Managment and Analysis of Physics Dataset – 1
A.A. 2019-20

Digital Circuits - 1

Overview

G.Collazuol

- Introduction to Digital Electronics
- Transistors and Logic Levels
- Propagation of Logic Levels → fanout and delays

Introduction to Digital circuits

- Boolean algebra and its representation
- Gates and Combinatorial Logic
- Flip-Flops and Sequential Logic
  - Timing and Shift Registers
  - Memory devices
  - State machines
  - Artithmetic Units
- Asynchronous vs Synchronous systems

- Circuits and Architectures
  - Logic Families
  - Mixed CMOS circuits
  - VLSI circuits
  - FPGAs
  - Microcontrollers

- Data Transfer and Data Communication
  - Buses
  - Peripherals
  - Links

Introduction – ENIAC a “programmable“ machine

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Introduction - ENIAC

- A dataflow machine that could be *wired* (i.e. programmed) to perform calculations

- The architecture consists essentially of a cascade of adders and logic elements that are acting on accumulators and that can be started by the results becoming available on the previous unit

- Could perform relatively complex calculation with a cycle-time of about 5K operations/sec

Introduction – Electronics in the ENIAC

PATENT SPECIFICATION

Application Date: June 21, 1919. No. 10,259/19. **148,582**

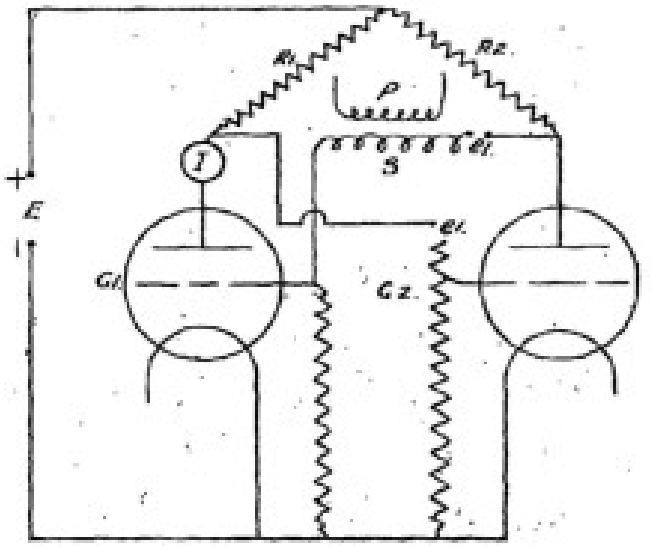
Complete Left: Feb. 18, 1920.

Complete Accepted: Aug. 5, 1920.

PROVISIONAL SPECIFICATION.

Improvements in Ionic Relays.

FIG. 2.



Introduction – Electronics in the ENIAC

Before the transistor

(i.e. the first electronic "switch")

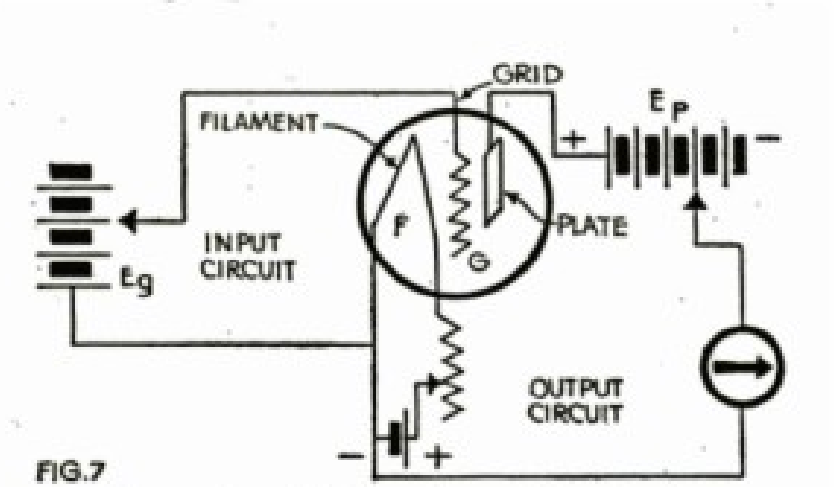
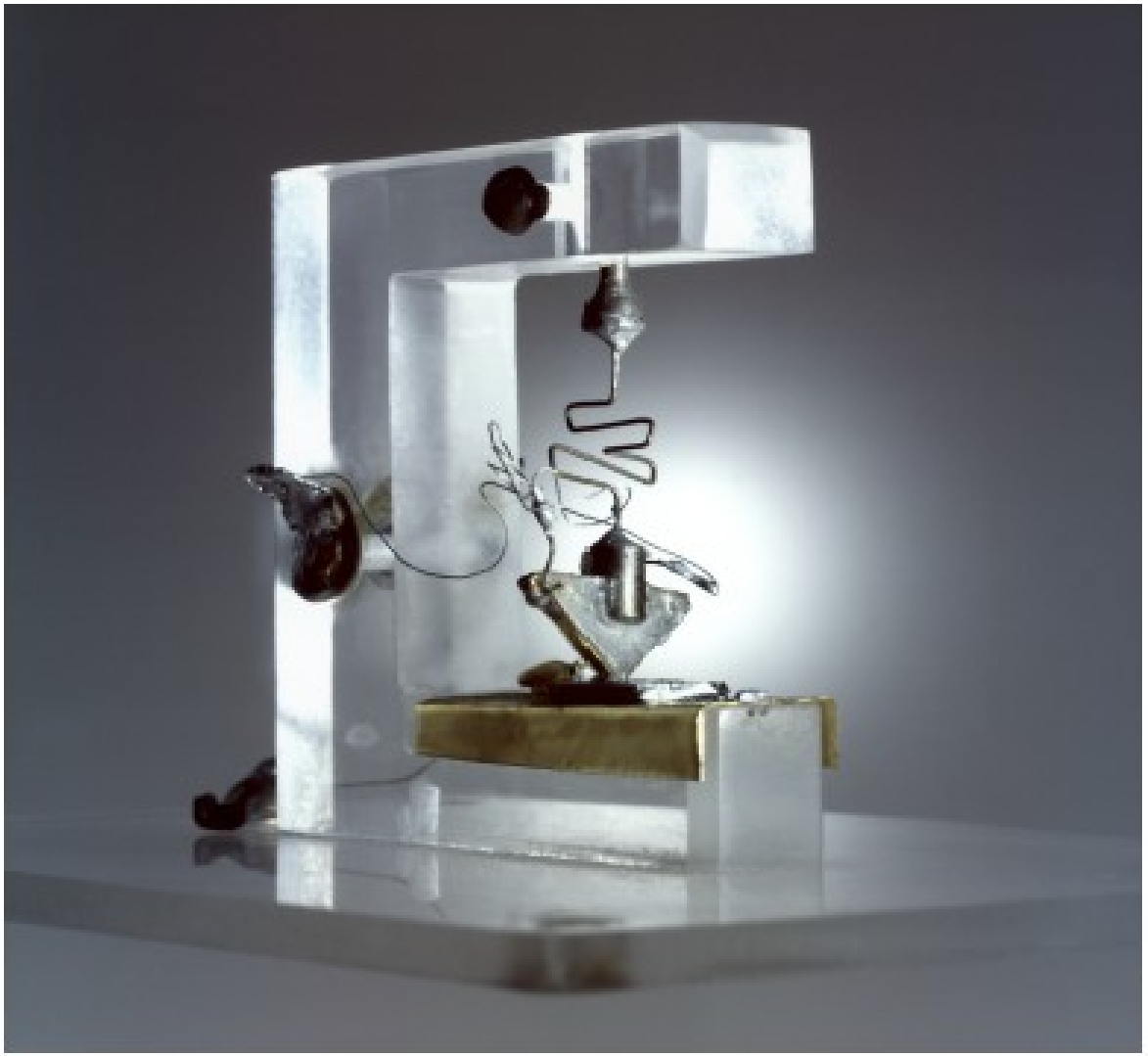
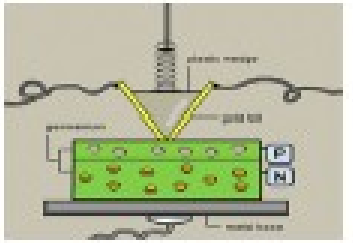


FIG.7

How to obtain the characteristics of the three-electrode vacuum valve. The apparatus used is simple

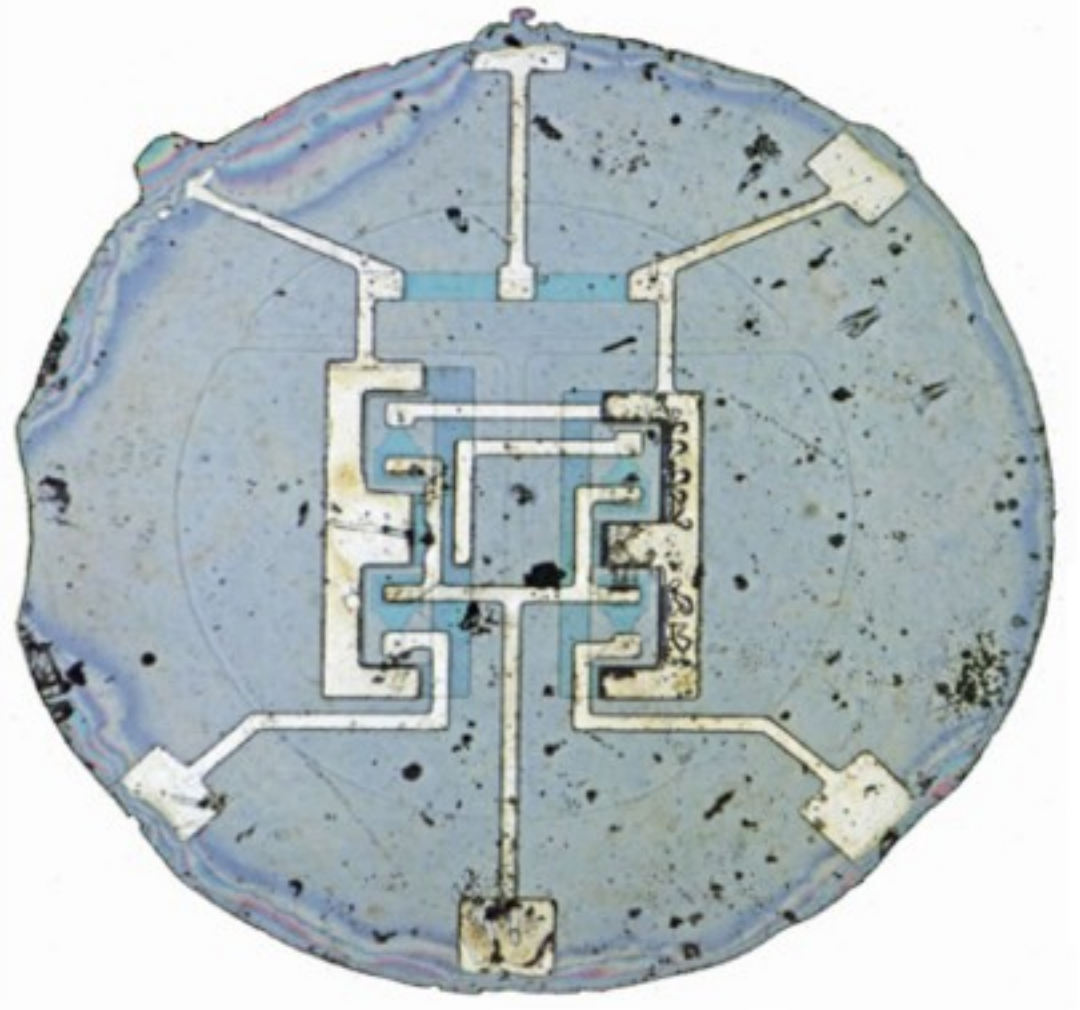
Introduction: the transistor revolution



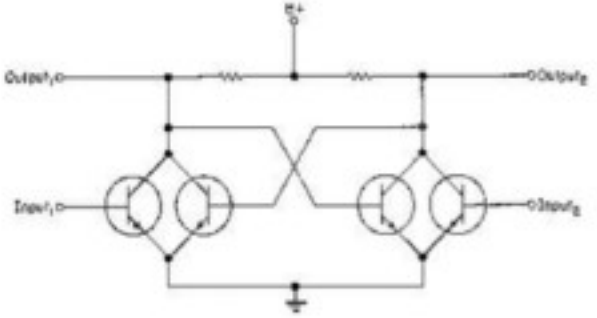


First Bipolar Transistor

Introduction: the first Integrated Circuit

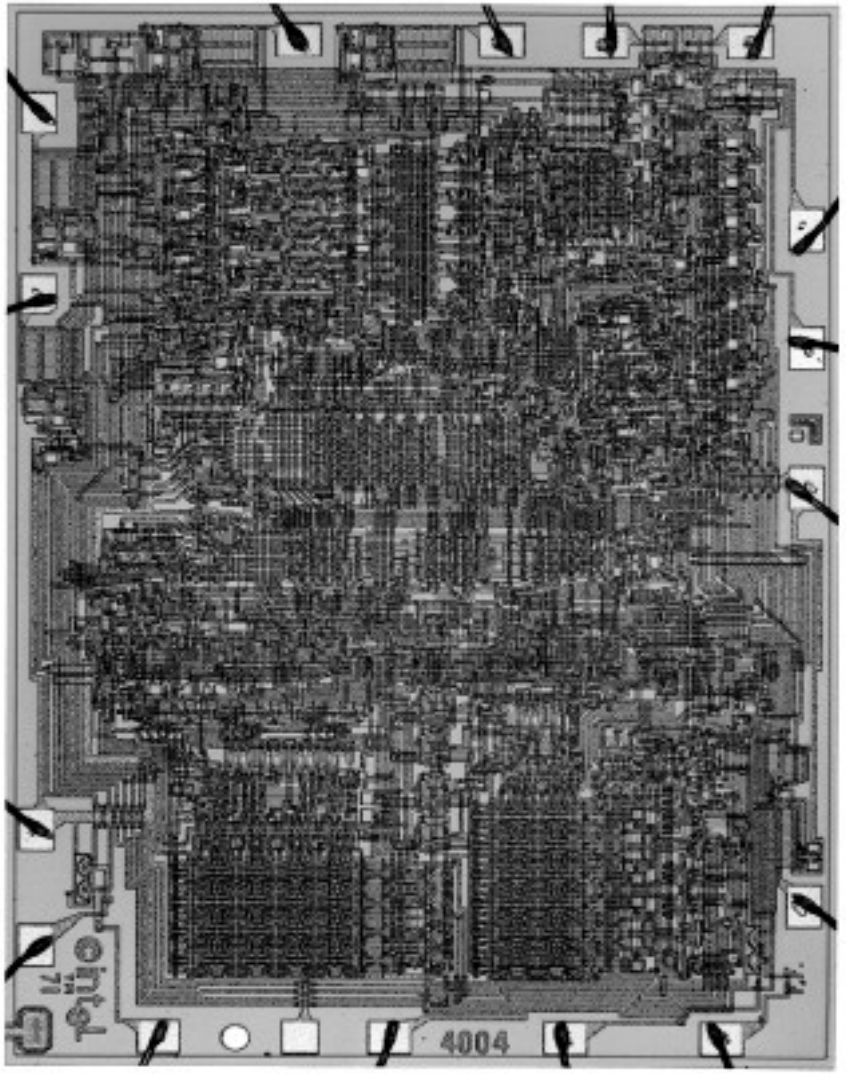


Fairchild
R-S Flip-Flop, 1960



Introduction

Intel 4004 Micro-Processor



1971
~1000 transistors
10μm tech
0.75 MHz operation

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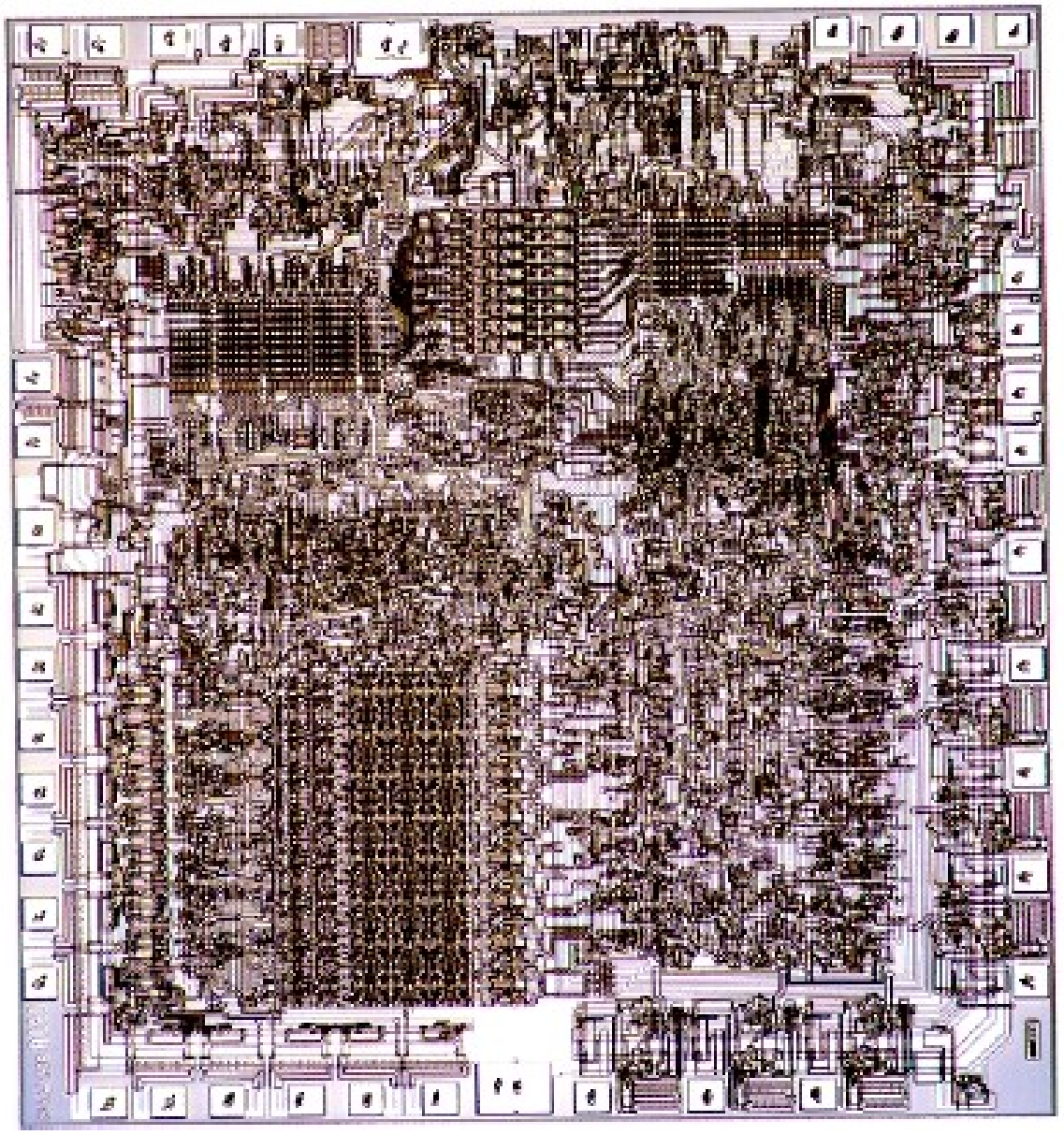
Introduction: 8080 Micro-Processor



Intel 1974,
6 micron N-channel
silicon gate MOS technology
4,500 transistors

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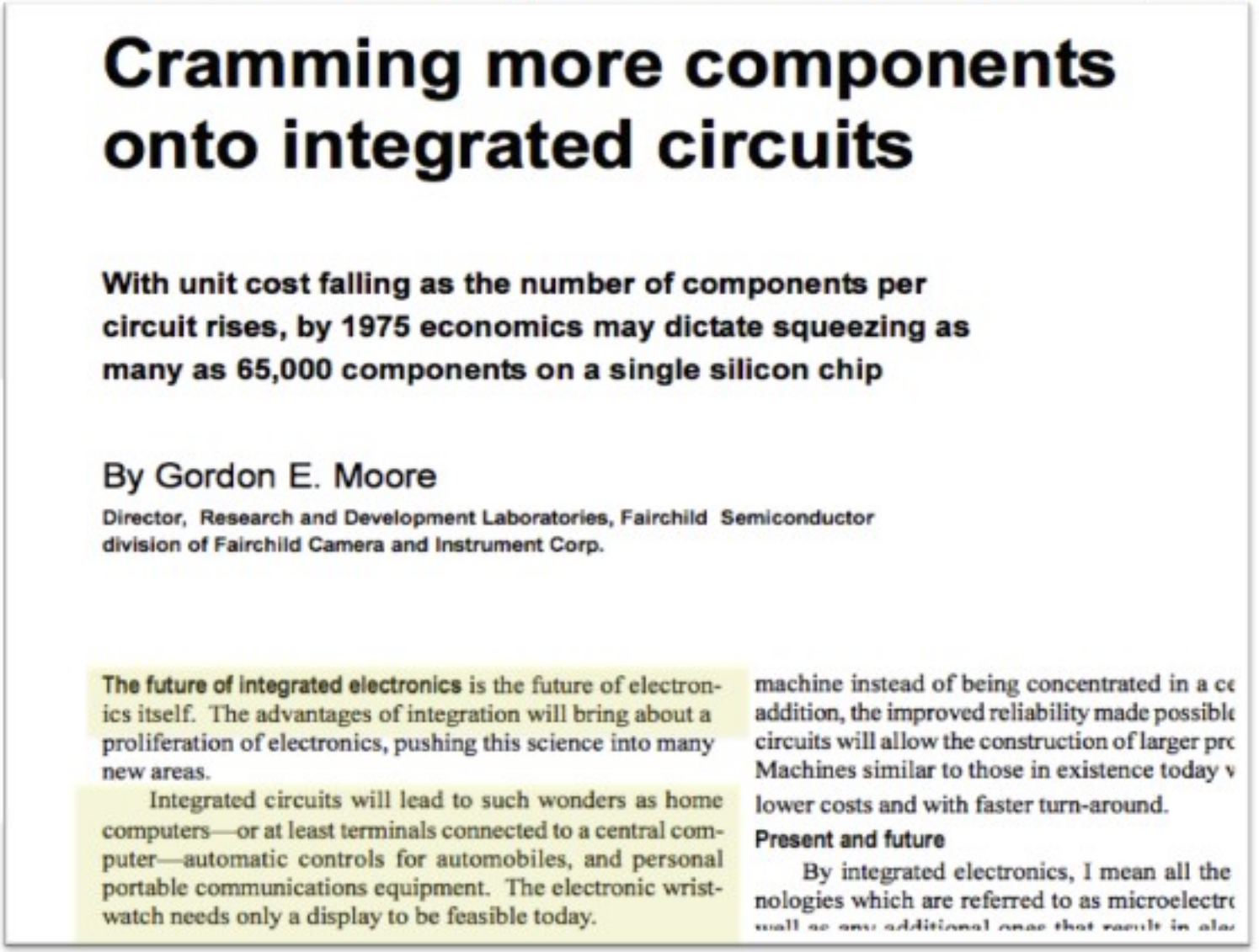
Introduction: transistors

50th anniversary of G. Moore's paper



Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

Electronics, Volume 38, Number 8, April 19, 1965

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

machine instead of being concentrated in a ce
addition, the improved reliability made possible
circuits will allow the construction of larger pro
Machines similar to those in existence today v
lower costs and with faster turn-around.

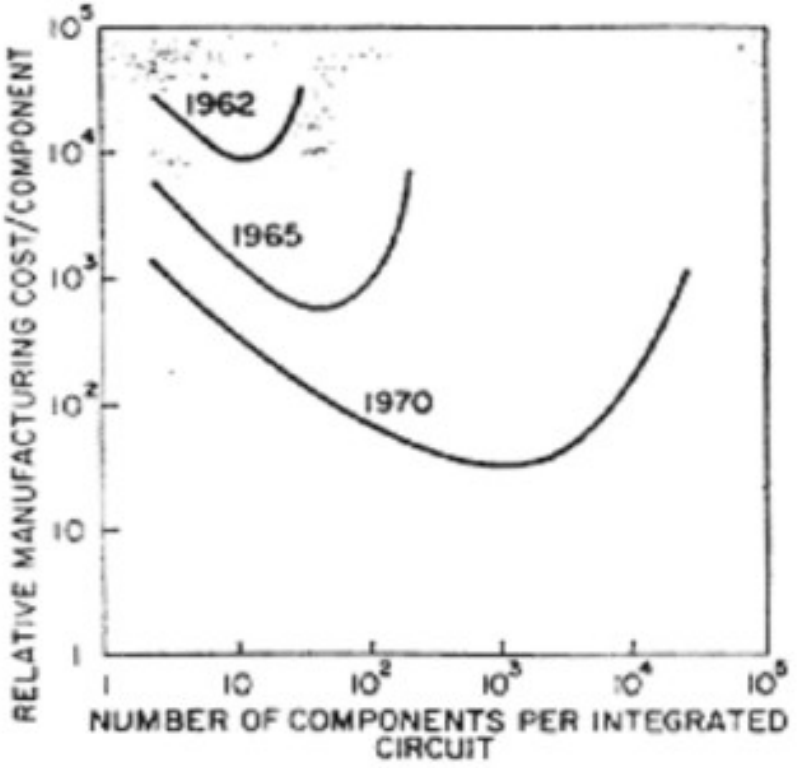
Present and future

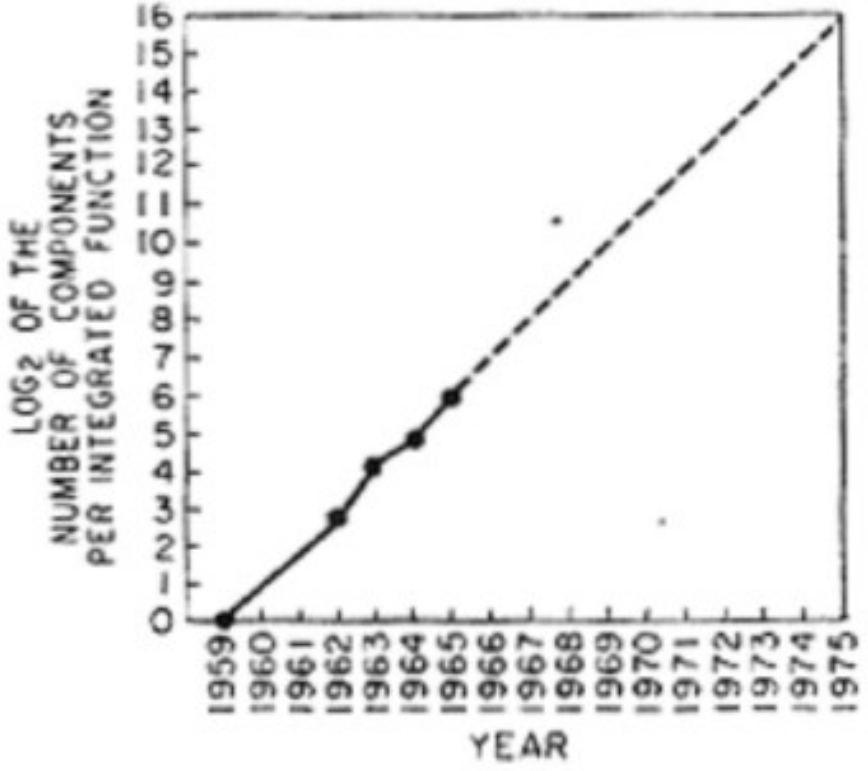
By integrated electronics, I mean all the
nologies which are referred to as microelectr

A. Marchioro / CERN

Introduction: transistors

50th anniversary of G. Moore's paper





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Present and future

By integrated electronics, I mean all the nologies which are referred to as microelectr

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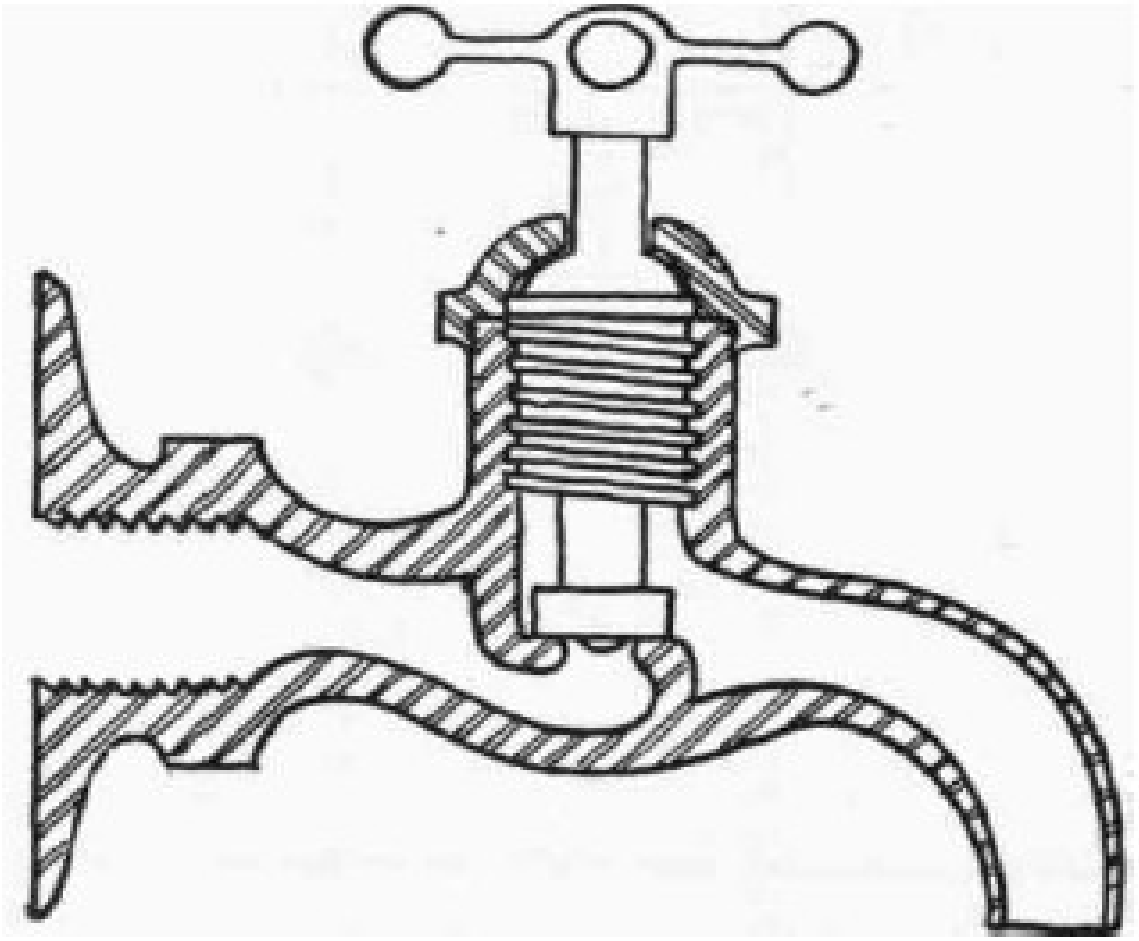
Introduction: what do we want from a transistor ?

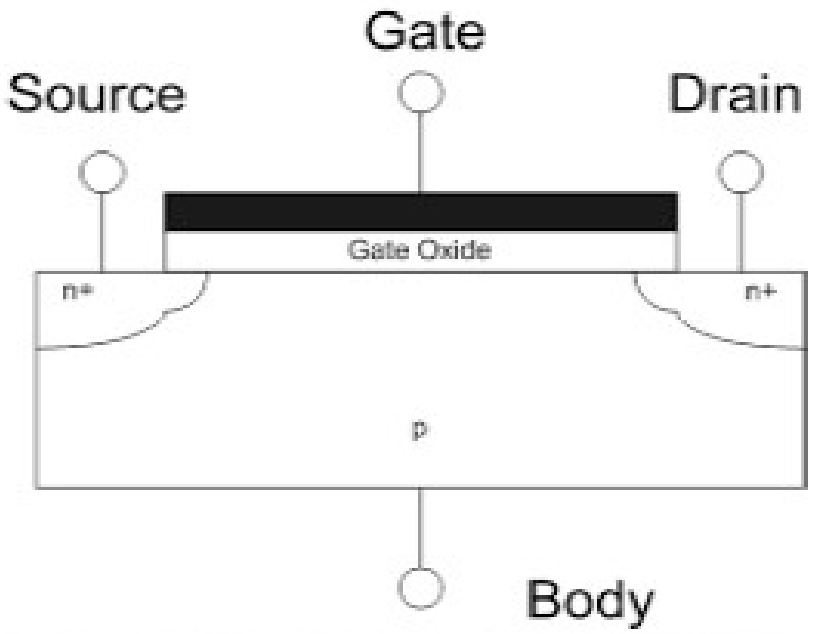
- A transistor (a digital transistor) is a device that "should" have the following characteristics:
  - to work as a switch (on or off)
  - have three terminals: an input, an output, a control
  - make a "sharp" transition between the two states (open or closed) in a time as short as possible
  - has no leakage current when off
  - has to deliver high current when on (to drive strongly the next stage).
    - Unfortunately this it is not uncorrelated from the previous requirement
  - make a transition between the two states with a voltage drive (Vg) as small as possible
  - control terminal should not be influenced by input/output terminal(s)
  - be physically small (otherwise other "parasitics" ruin the party)
  - Must have complementary type (i.e. a second type which is turned on when the first is turned off using the same "control").
- Good "analog" characteristics are desirable but by far not necessary or even important for the the majority of applications.

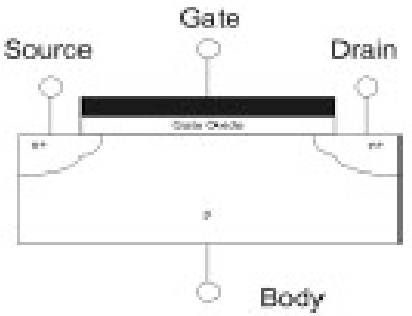
Introduction: what do we want from a transistor ?

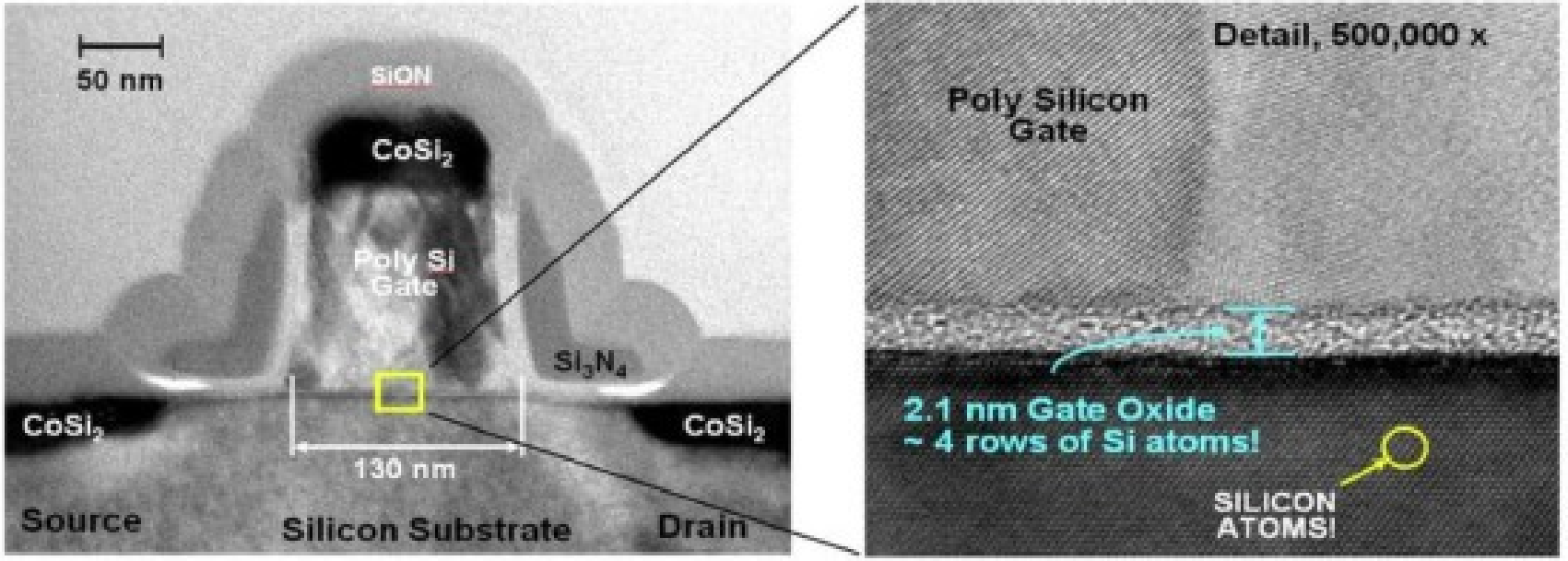
? !



Introduction: Field Effect Transistor

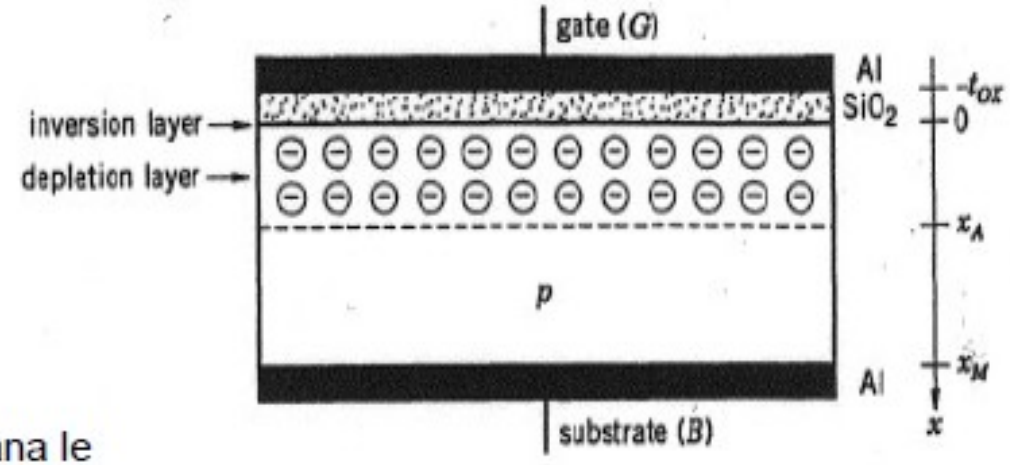






Condensatore MOS

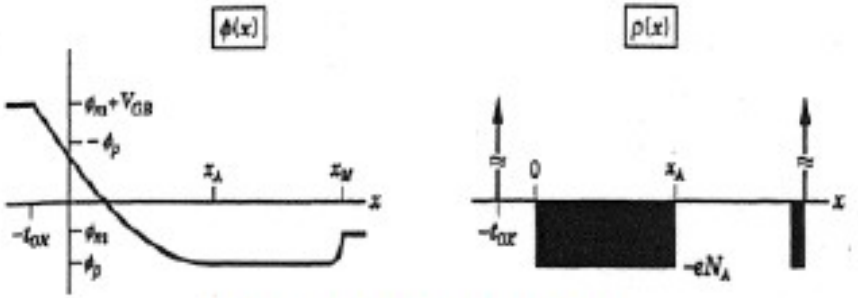
Dispositivo a due terminali:
"Gate" e "Substrato" o "Body"
Utile per spiegare principio dei transistor MOSFET:



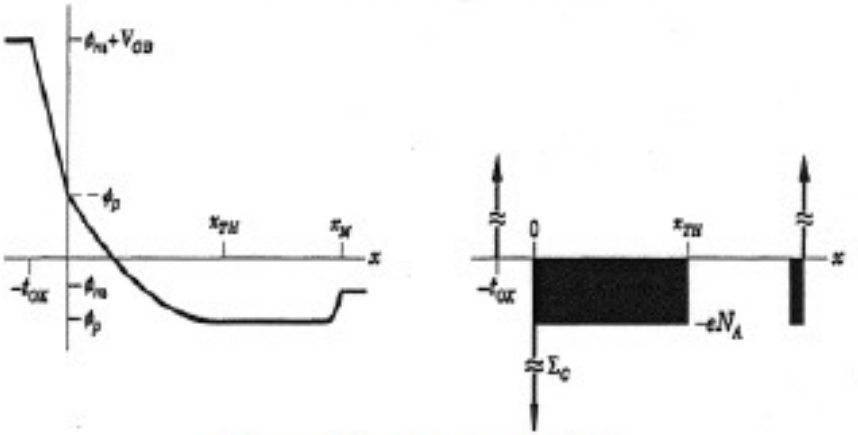
- All'aumentare di $V_{GB} > 0$ il substrato (p-type in figura) inizia a svuotarsi: il campo elettrico allontana le lacune (maggioritari) ed attrae verso l'ossido gli elettroni (minoritari) che si accumulano in uno strato spesso nanometri

- Si osserva che esiste una **soglia (V_{th}) per V_{GB}** oltre la quale gli elettroni sono accumulati con una densita` pari a quella dei maggioritari:
→ **strato di inversione ("canale") conduttivo**
→ tensione **V_{GB} regola la densita` dei portatori** minoritari nel canale

Nota: impiantando un opportuno strato superficiale di carica fissa (positiva) all'interfaccia Ossido-Semicondutture e` possibile rendere la tensione di soglia negativa: in tal caso il canale e` presente gia` con $V_{BG}=0$

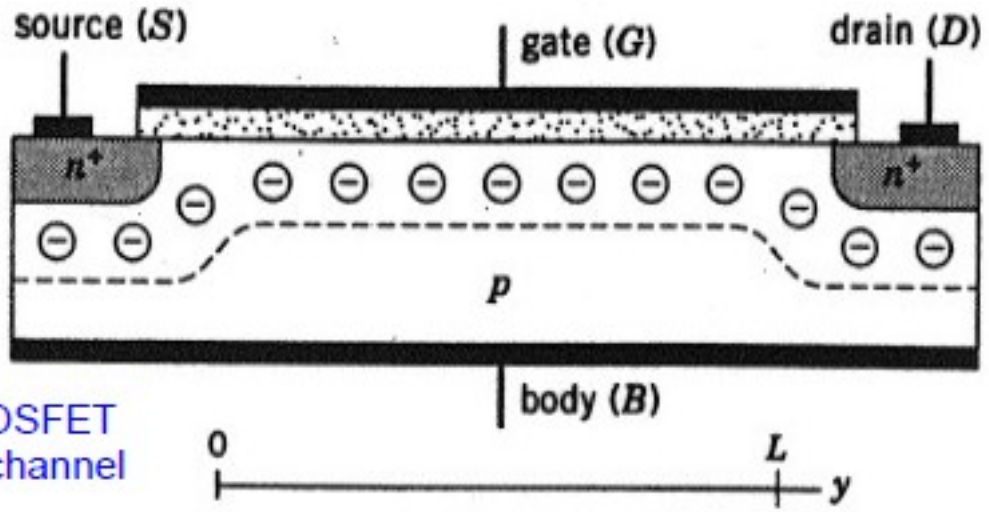


$V_{GB} < V_{th}$ sotto soglia

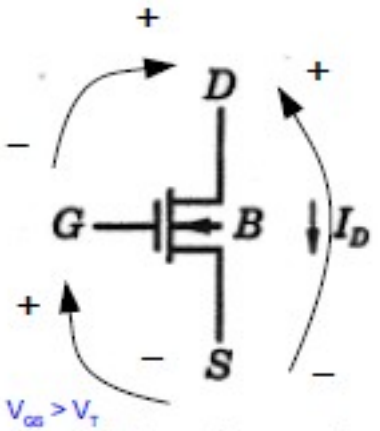


$V_{GB} > V_{th}$ sopra soglia

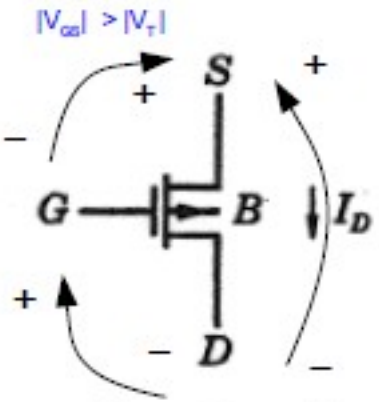
Introduction: MOS FET transistor



MOSFET
n-channel



(a) *n*-channel

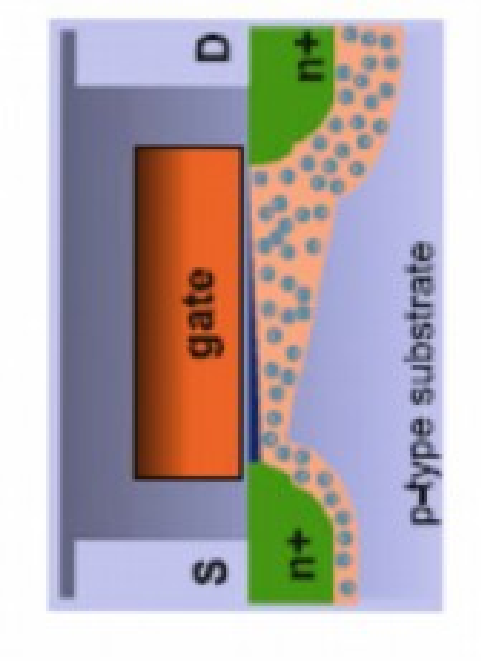


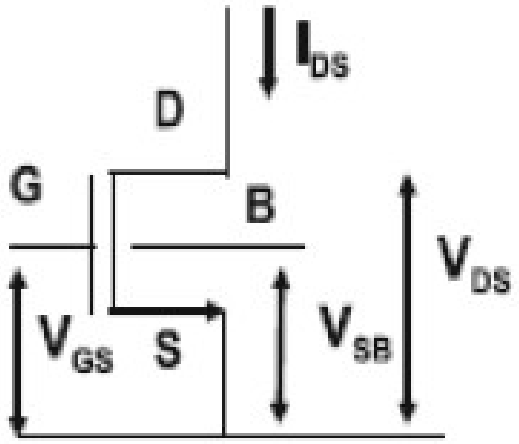
(b) *p*-channel

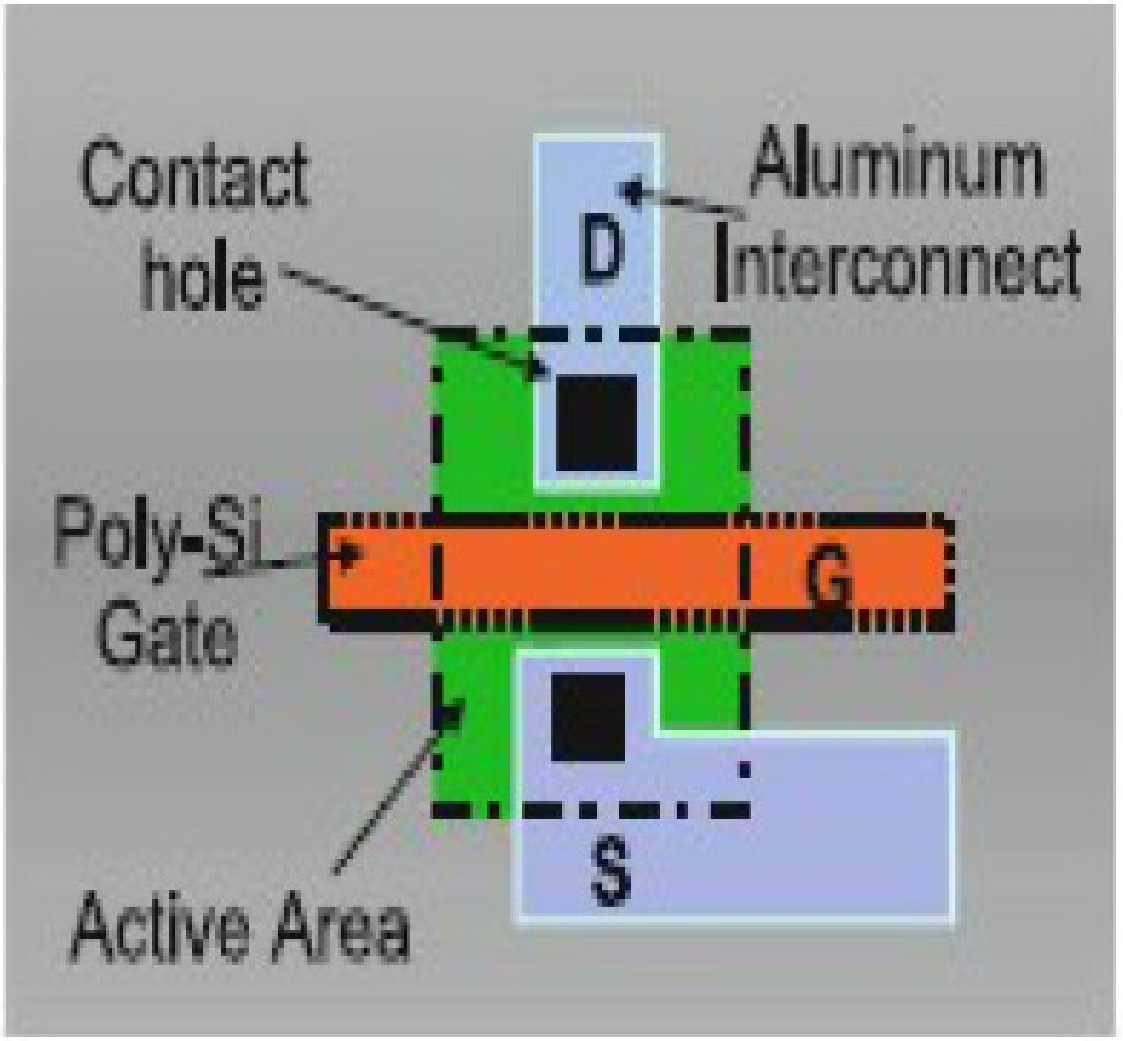
Il dispositivo sfrutta il canale (strato di inversione) che si forma sotto l'ossido polarizzando positivamente il Gate rispetto a Body (connesso a Source) e permette il passaggio di corrente tra Source a Drain.
Il potenziale del Gate V_{GS} permette di controllare tale corrente agendo sulla densita` dei minoritari nel canale grazie al campo elettrico prodotto (da cui il nome "Field Effect Transistor" o "FET")

Nota: il dispositivo ha 4 terminali; il Body deve essere posto alla tensione piu` bassa (alta) in n-channel (p-channel) per evitare di polarizzare forward il substrato; questo spesso si realizza connettendo Body con Source
(ma non sempre e` possibile)

Introduction: MOS FET transistor

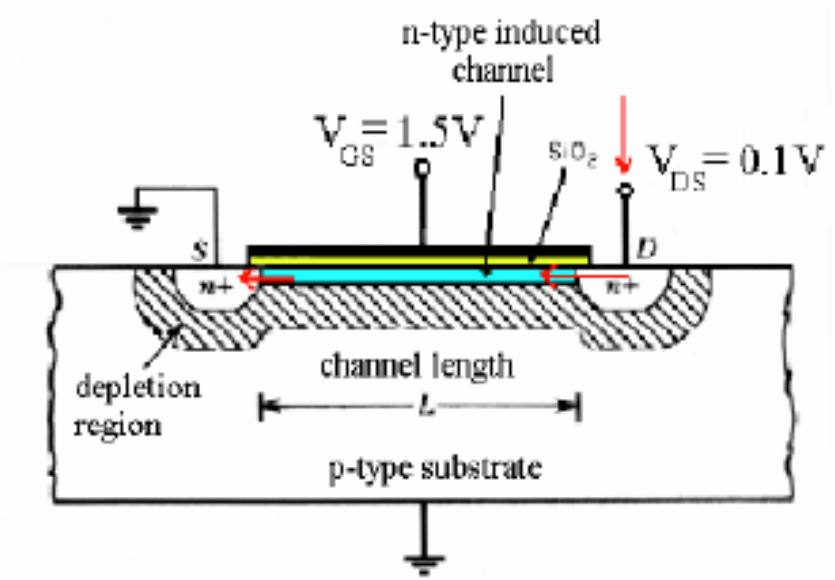


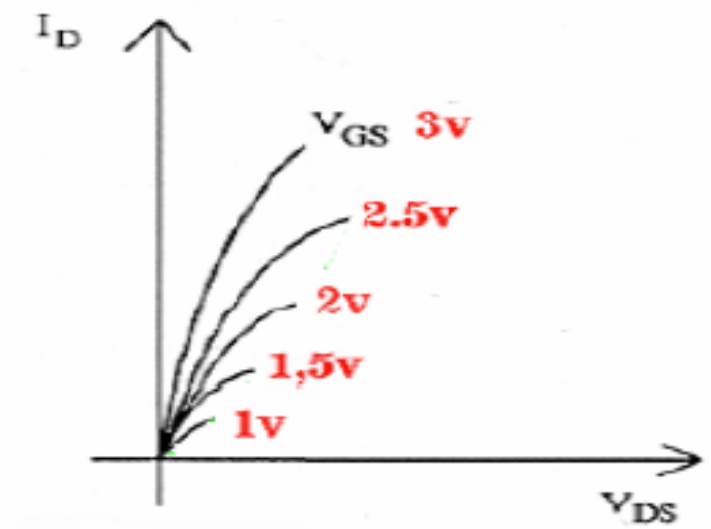




MOSFET – Regime ohmico

In prima approssimazione...





resistenza di canale tra Source e Drain

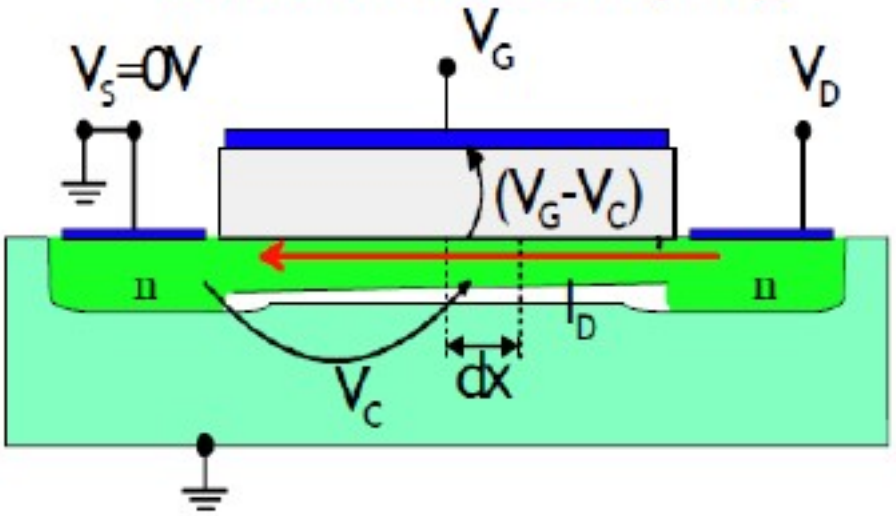
$$R_{ch} \propto \frac{1}{(V_{GS} - V_T)}$$

Se $V_{GS} > V_{th}$ (sopra soglia) si ha che per piccole tensioni V_{DS} la conducibilita` e` costante lungo il canale e la corrente nel canale cresce linearmente: in questo regime
→ **MOSFET e` resistenza controllata (in tensione)**

Aumentando V_{DS} l'incremento della corrente e` meno che lineare: la caduta di potenziale lungo il canale determinata dal passaggio della corrente fa diminuire la tensione ai capi dell'ossido man mano che ci si sposta verso il Drain
→ la carica diminuisce → **conduciblita` diminuisce lungo canale** (da S verso D)
→ all'aumentare di V_{DS} la resistenza (media) del canale aumenta

MOSFET – Regime ohmico → triodo

…piu` precisamente:
cerchiamo relazione tra I_D e V_{DS}



Legge di Ohm

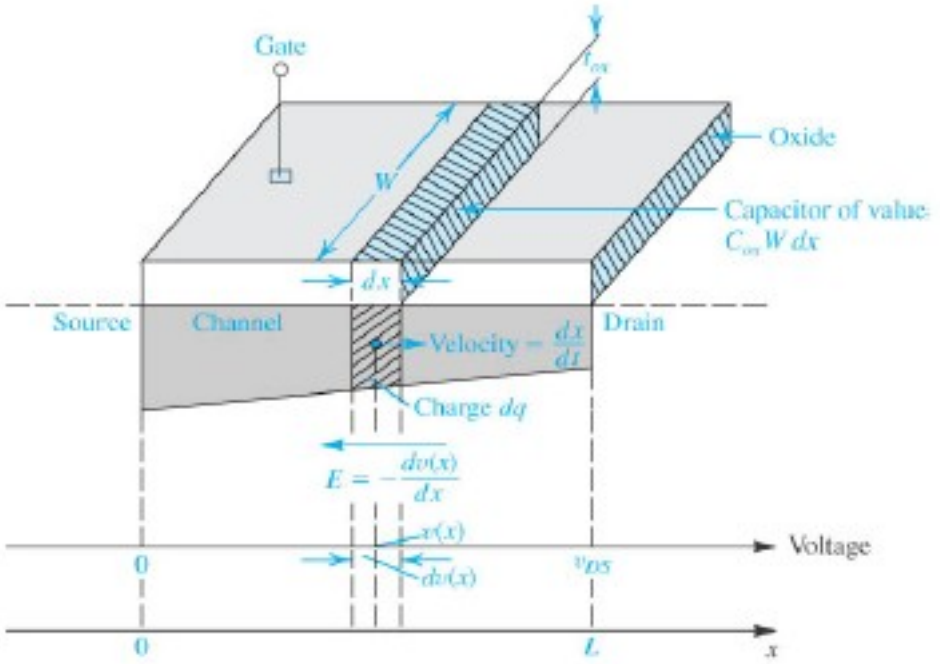
$$dV_C = I_{DS} \cdot dR$$

con $dR = \dfrac{dx}{\mu Q_n' W}$

$$dV_C = I_{DS} \cdot \frac{dx}{\mu C_{ox}'(V_G - V_C - V_T)W}$$

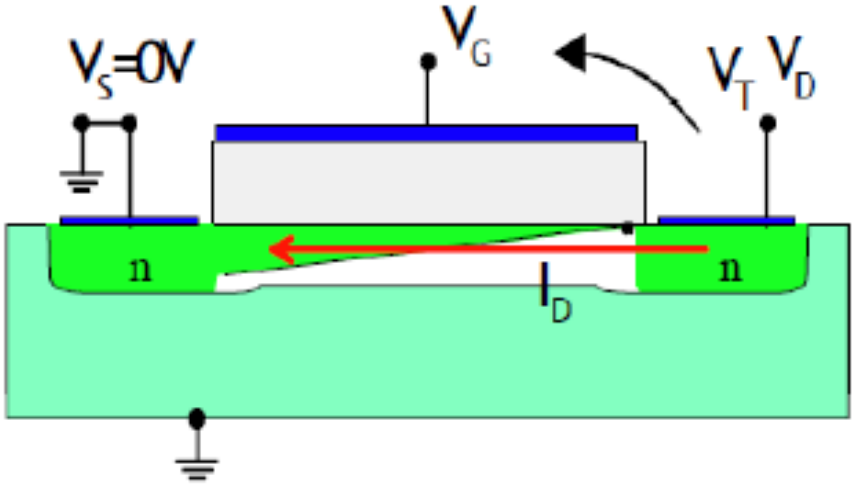
da cui $$\mu C_{ox}' \int_0^{V_{DS}} (V_G - V_C - V_T)\, dV_C = I_{DS} \cdot \frac{1}{W}\int_0^L dx$$

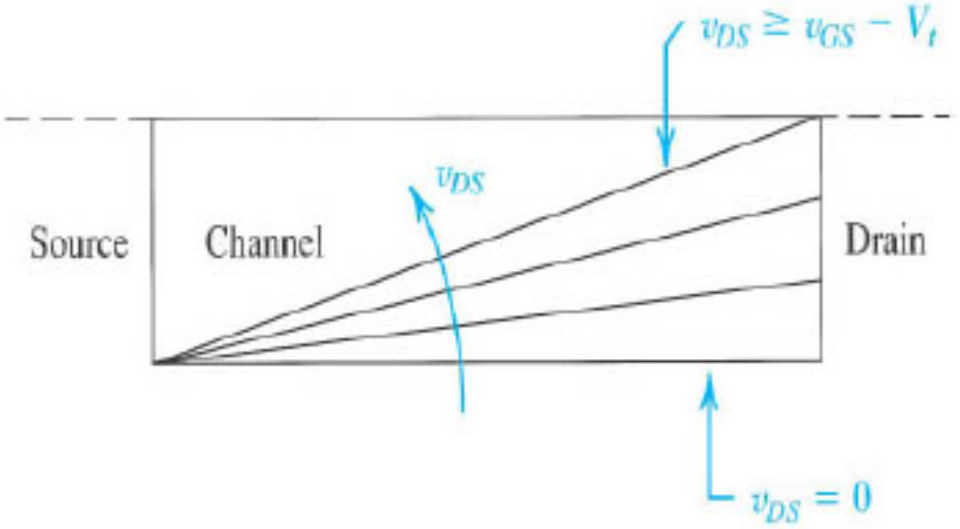
$$I_{DS} = \mu C_{ox}' \frac{W}{L}\left[(V_G - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$



(W e` la profondita` del canale;
direzione normale a piano figura)

MOSFET – Regime di Saturazione





$$V_{DS}^{sat} = (V_{GS} - V_T)$$

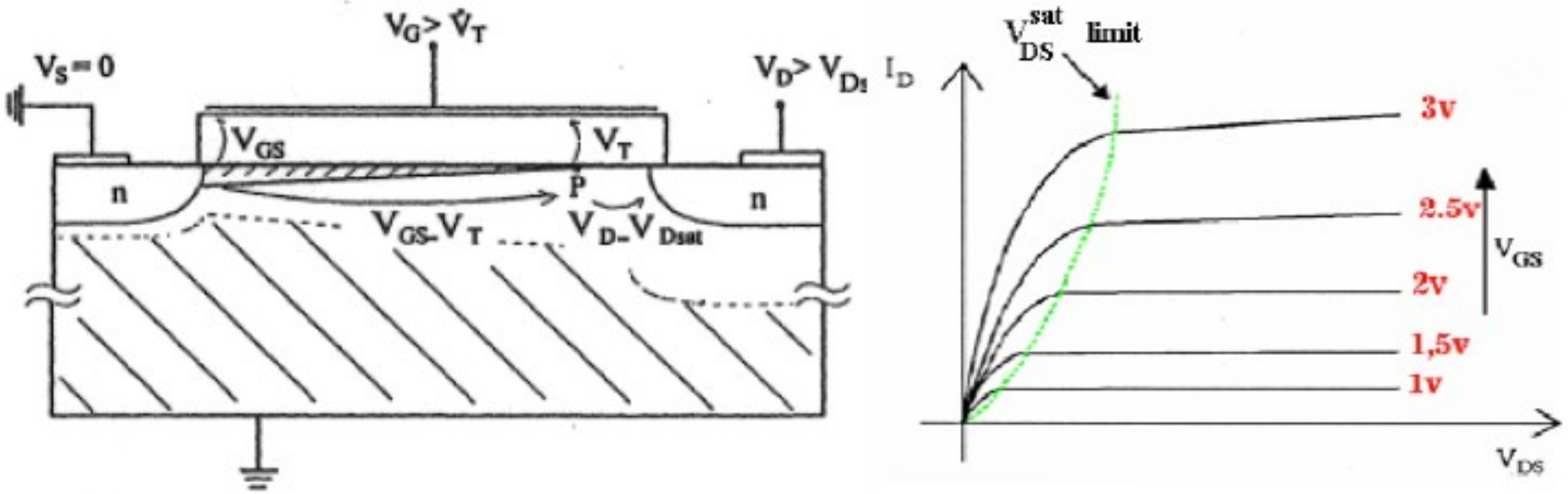
$$I_{DS} \propto \frac{(V_{GS} - V_T)}{R_{ch}} \approx (V_{GS} - V_T)^2$$

Aumentando ancora V_{DS} si arriva alla situazione in cui il potenziale V_{GD} non basta piu`per avere canale conduttivo esteso fino all'estremo del Drain ("*pinch-off*" o "strozzamento"). Cio' accade quando la caduta di potenziale ai capi dell'ossido al Drain e`pari a V_{th} ovvero V_G-V_D=V_{th}

In tale situazione la tensione ai capi del canale conduttivo vale V_{GS}-V_{th} ≡V_{DSat} (tensione di saturazione del canale) ed e` il rapporto tra $V_{GS}$-$V_{th}$ e la resistenza del canale $R_{ch}$ a determinare la corrente $I_D$ che fluisce tra Source e Drain (invece $V_D$ non conta piu` !)

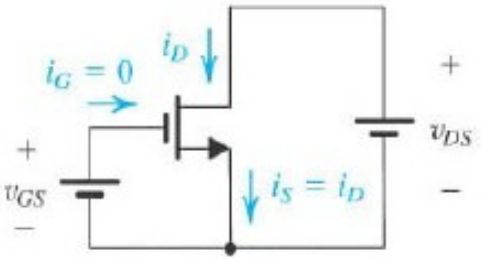
Nota: il *pinch-off* del canale conduttivo (nel punto P) non impedisce il passaggio della corrente. Infatti gli elettroni che giungono nel punto P continuano ad essere accelerati verso il Drain da una differenza di potenziale (pari a V_{DS}-V_{DSat})

Introduction: MOS FET Characteristic

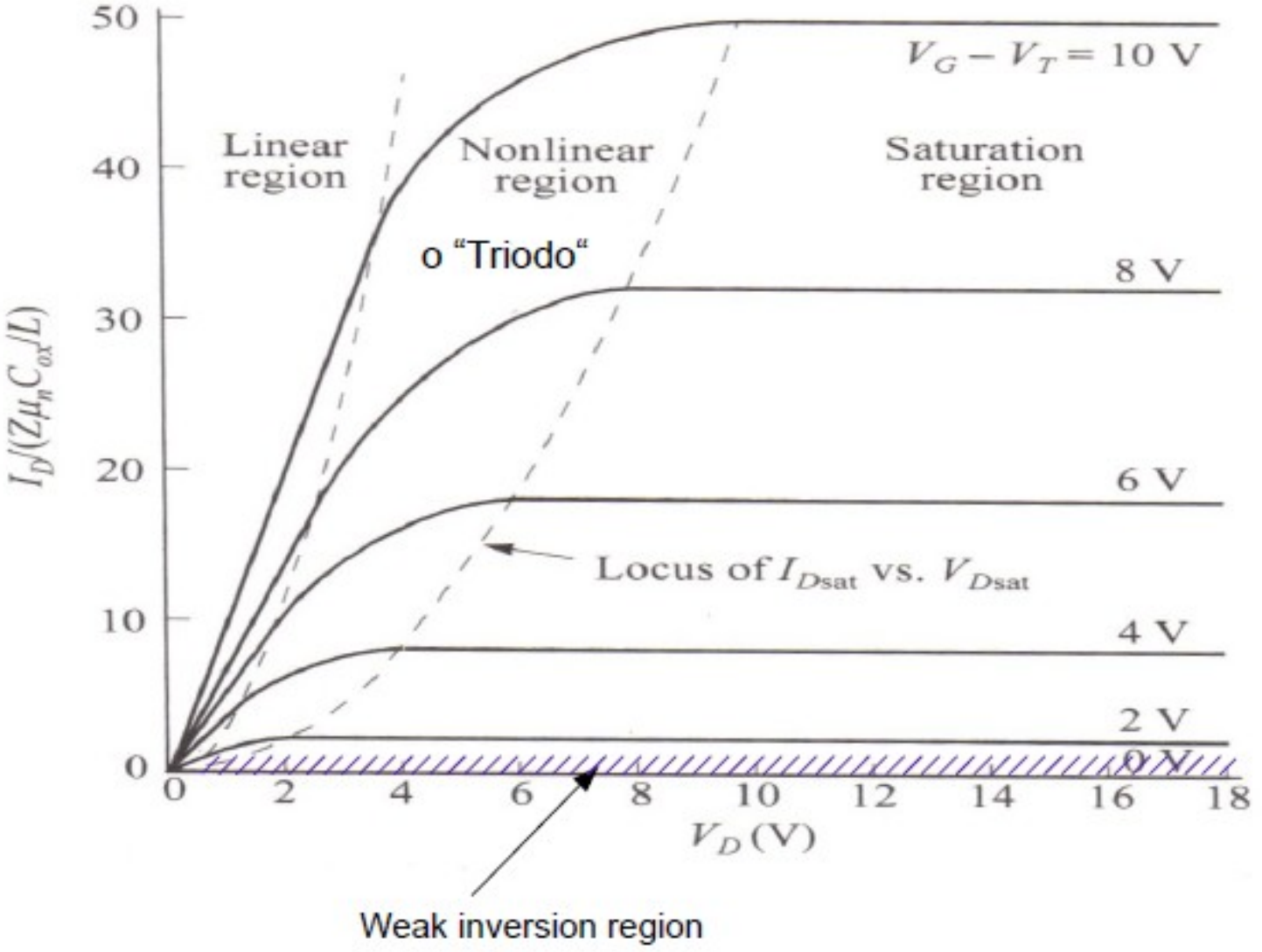


All'aumentare di V_{DS} (> V_{DSsat}) ai capi del canale conduttivo (ridotto ora al tratto tra Source ed il punto P) si ha sempre la caduta fissa di tensione esattamente pari a V_{GS}-V_{th} (minima ai capi dell'ossido per invertire il canale), mentre la tensione di Drain in eccesso V_{DS} - V_{DSat} va a cadere tra il punto P ed il Drain (determinando un allargamento locale della regione svuotata). La corrente I_D rimane quindi ~ costante all'aumentare di V_{DS} e data dal rapporto tra (V_{GS}-V_{th}) e la resistenza di canale (entrambi ~costanti)

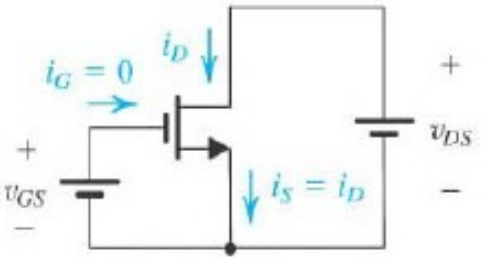
Introduction: MOS FET Characteristic



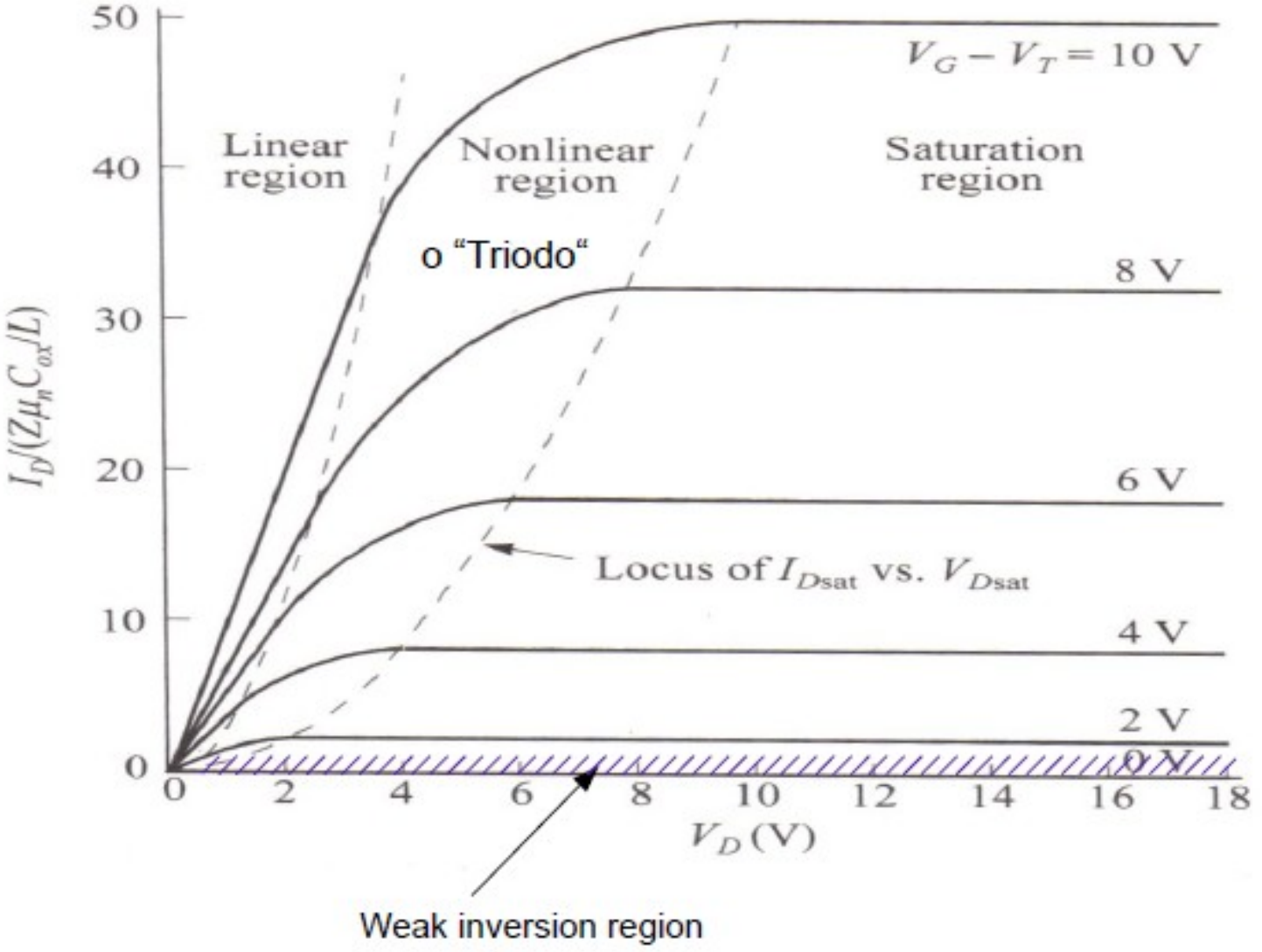
MOSFET n-channel



Introduction: MOS FET Characteristic



MOSFET n-channel



Why is Digital so good ?

Analog Adder (summing amplifier)

June 11, 1946. K. D. SWARTZEL, JR

SUMMING AMPLIFIER

Filed May 1, 1941

Patented June 11, 1946 2,401,779

UNITED STATES PATENT OFFICE

2,401,779

SUMMING AMPLIFIER

Karl D. Swartzel, Jr., Teaneck, N. J., assignor to Bell Telephone Laboratories, Incorporated, New York, N. Y., a corporation of New York

Application May 1, 1941, Serial No. 391,331

11 Claims. (Cl. 179—171)

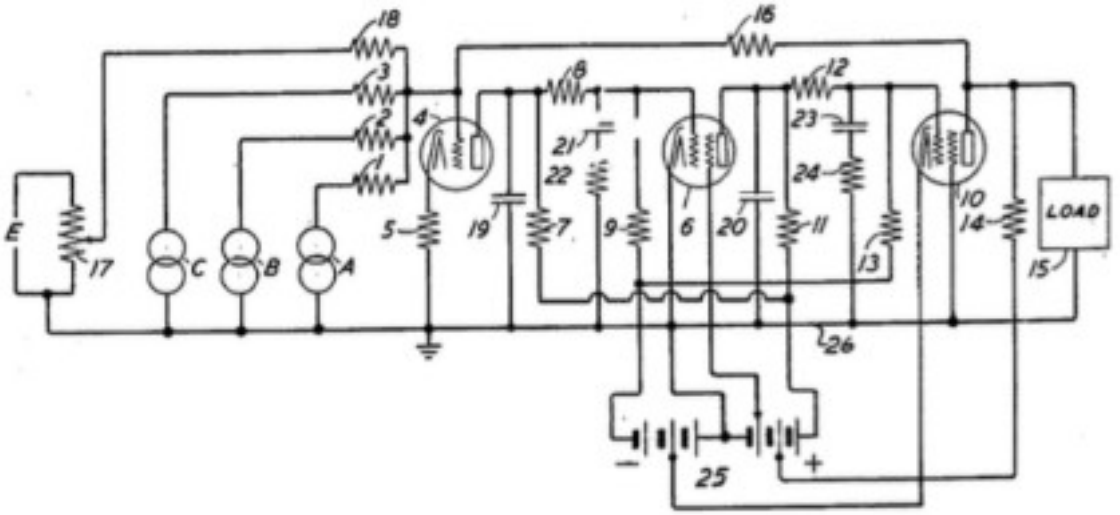
1

This invention relates to electrical calculating devices and particularly to a device for obtaining the sum of a plurality of electrical voltages.

The object of the invention is to obtain the sum of a number of electrical voltages, one pole of each of the voltages being grounded.

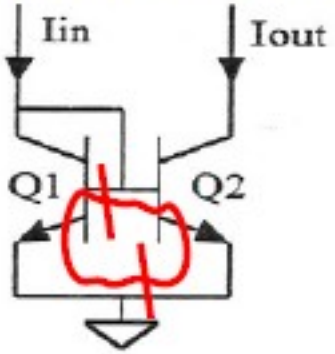
2

In the drawing the generators A, B, and C, diagrammatically symbolizing three sources of voltages to be added, are respectively connected in serial relationship with one of the impedances 1, 2, 3, each having a relatively high impedance compared to the effective input imped-



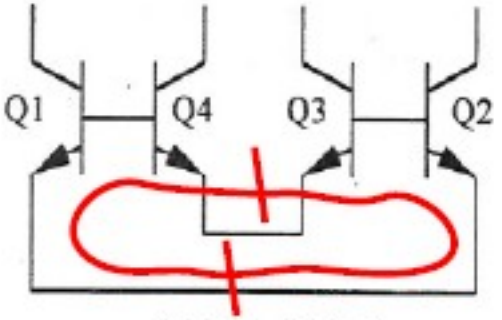
Analog Multiplier (Gilber cells)

Specchio di corrente



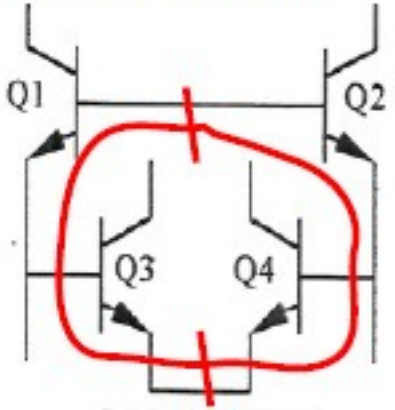
Ic1 = Ic2

Celle di Gilbert... mixer e ampli di corrente



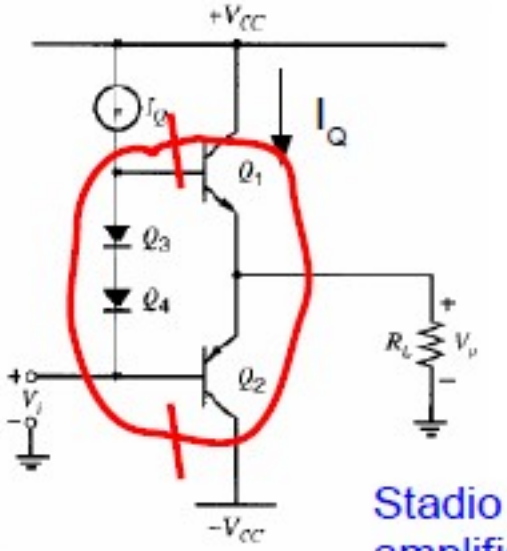
Ic1 Ic3 = Ic2 Ic4

Type A Cell (Alternating)



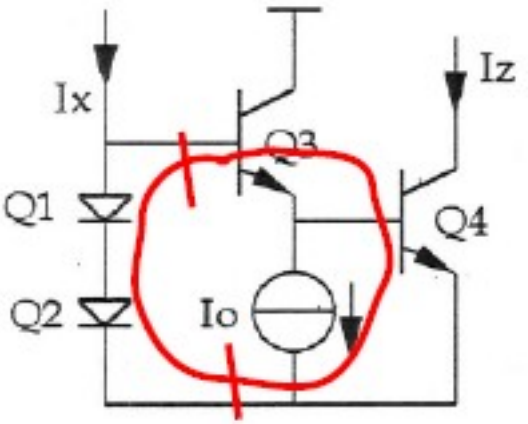
Ic1 Ic3 = Ic2 Ic4

Type B Cell (Balanced)



Stadio uscita di amplificatore

Stadio quadratore (1 quadrante)



$Iz = Ix^2/Io$

“Operational“ Amplifier

Analysis of Problems in Dynamics by Electronic Circuits*

JOHN R. RAGAZZINI†, MEMBER, I.R.E., ROBERT H. RANDALL‡, AND FREDERICK A. RUSSELL§, MEMBER, I.R.E.

Summary—This paper describes a method for obtaining an engineering solution for integrodifferential equations of physical systems using an electronic system. The components consist of standard plug-in feed-back amplifier units. As the interconnections are wires, resistors, and capacitors, no complicated mechanical layout problem is involved and a generally flexible analyzer need not be set up, for it is a simple matter to assemble the particular circuit for any system of equations for which solutions are desired. The system should, therefore, be of interest to those involved in a study of the dynamics of physical systems.

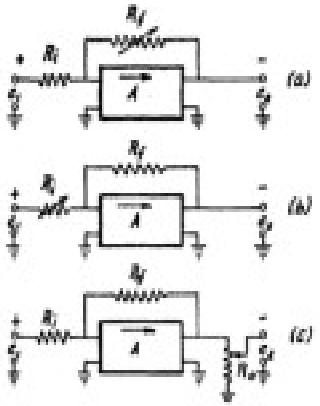


Fig. 3—Three methods for obtaining variable changes in scale or gain.

II. Operational Amplifiers

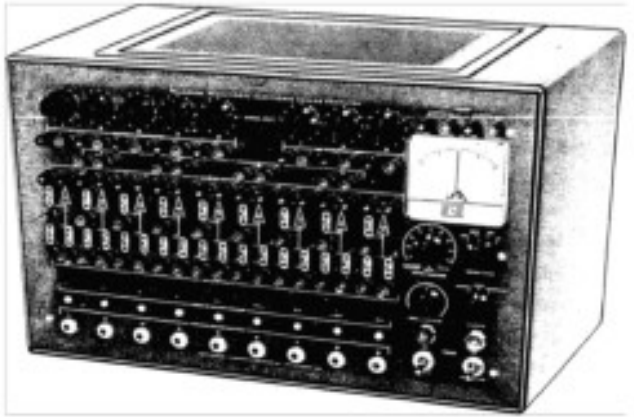
The term "operational amplifier" is a generic term applied to amplifiers whose gain functions are such as to enable them to perform certain useful operations such as summation, integration, differentiation, or a combination of such operations. In view of the fact that

Proceedings of the IRE, 1946

Analog Computer

Heathkit EC1 (circa 1960)

OPERATIONAL MANUAL FOR THE HEATH
EDUCATIONAL ANALOG COMPUTER
MODEL EC-1



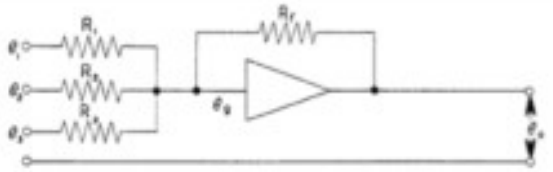


Figure 5 AMPLIFIER AS ADDER

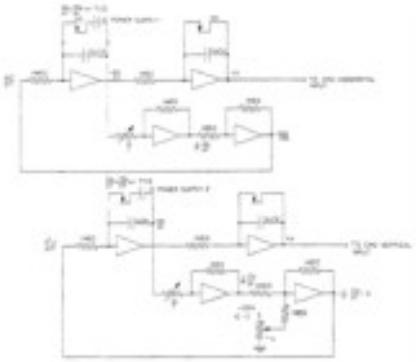


Figure 34

COMPUTER SETUP FOR PROJECTILE PROBLEM

The components of the initial velocity are controlled by IC-1 and IC-2, while the acceleration due to gravity, g, is controlled by IC-3. Air resistance is controlled by the controls m/c. The solution is shown in Figure 35.

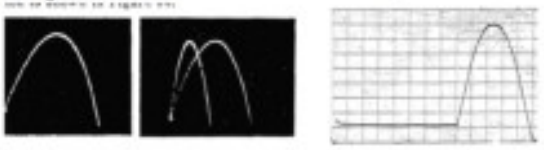


Figure 35 A

Figure 35 B

SOLUTION OF PROJECTILE PROBLEM

A. Marchioro / CERN

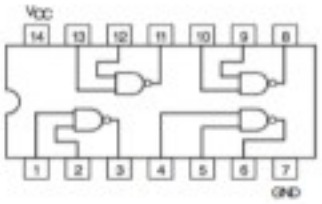
Why are analog computers out of fashion?

- Components cannot (easily) be fabricated all equal and are subject to degradation with aging
  - Mismatch of components causes errors or non-consistent results
- Components characteristics are almost always temperature dependent
  - E.g.: Resistivity is $\rho(T) = \rho_0[1 + \alpha(T - T_0)]$
  - Gain of transistors (through mobility) depends on T
- Behavior (i.e. "function") of circuits depends (almost always) on power supply variation and noise
  - References must be kept stable
  - Supply must be noiseless
- Transmission of "analog" information is badly subject to noise
- Noise is always "additive" and cannot be removed

On/Off → Off/On

MOTOROLA

QUAD 2-INPUT NAND GATE



MC54/74F00

QUAD 2-INPUT NAND GATE
FAST™ SCHOTTKY TTL

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

MC54/74F00

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

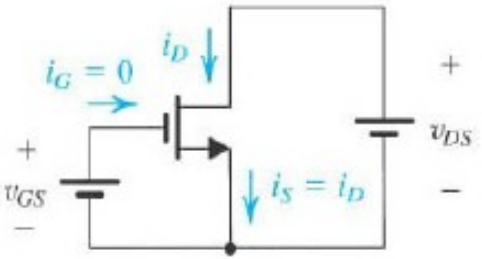
Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage					V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74				V	I_{OH} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current					μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				2.8	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				10.2	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

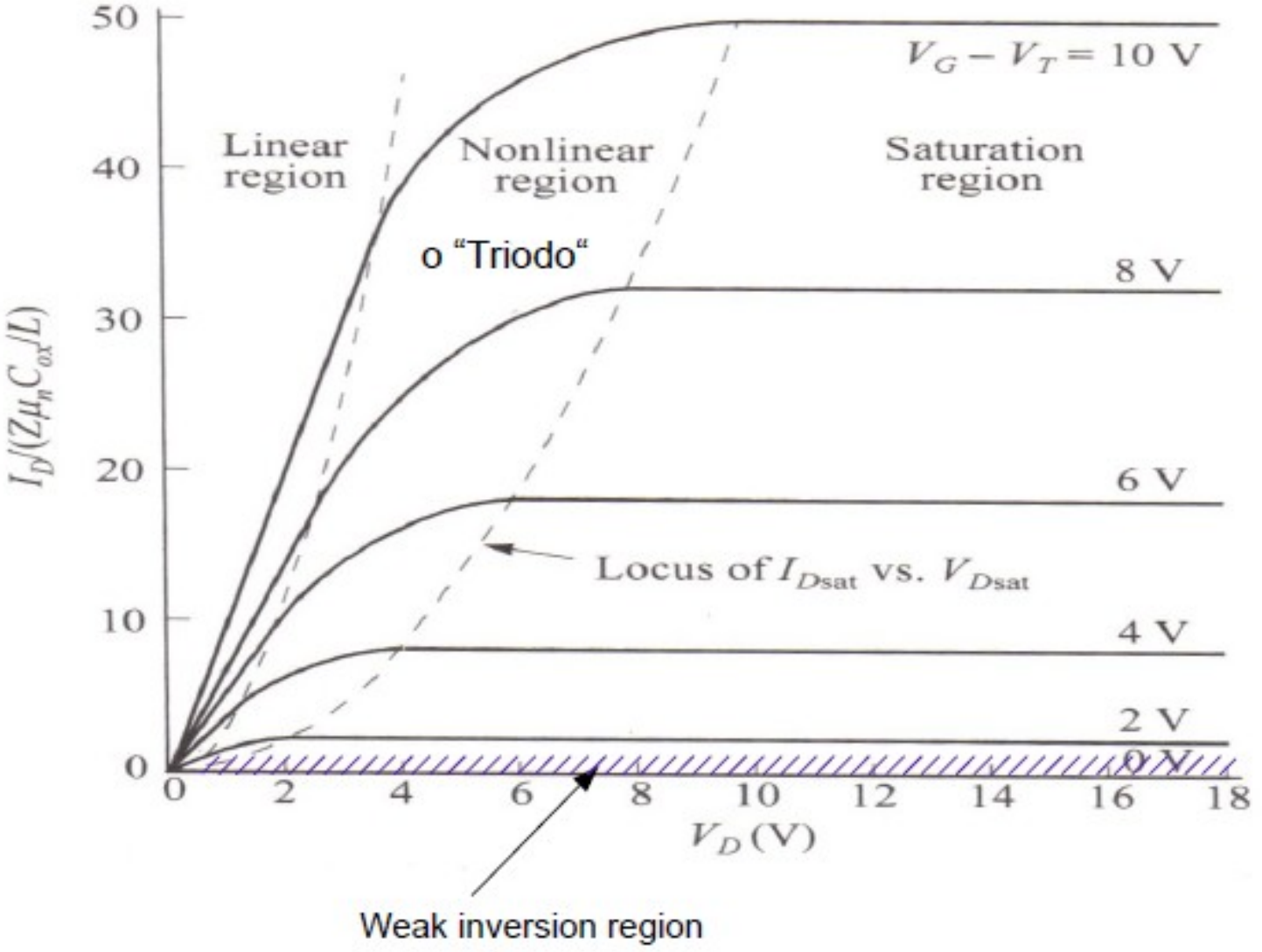
AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF Min	Max	54F T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF Min	Max	74F T_A = 0°C to 70°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF Min	Max	Unit
t_{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t_{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns

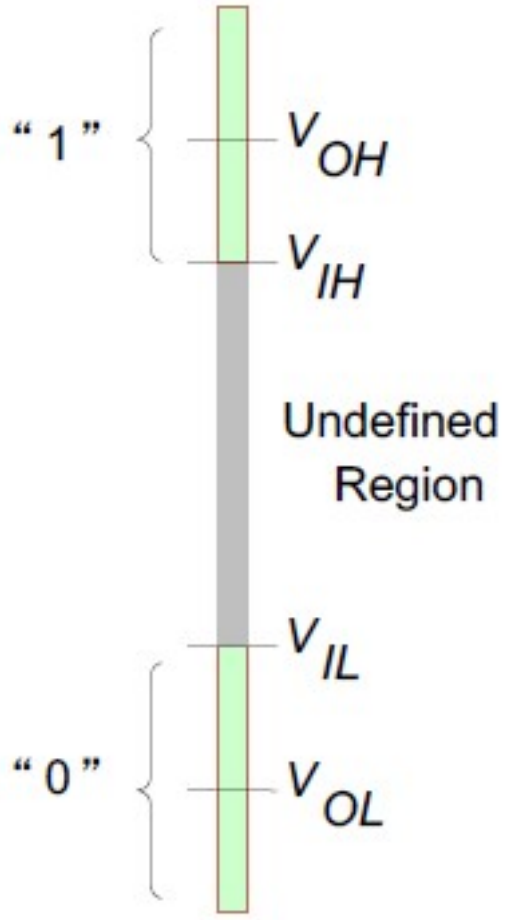
Introduction: MOS FET Characteristic

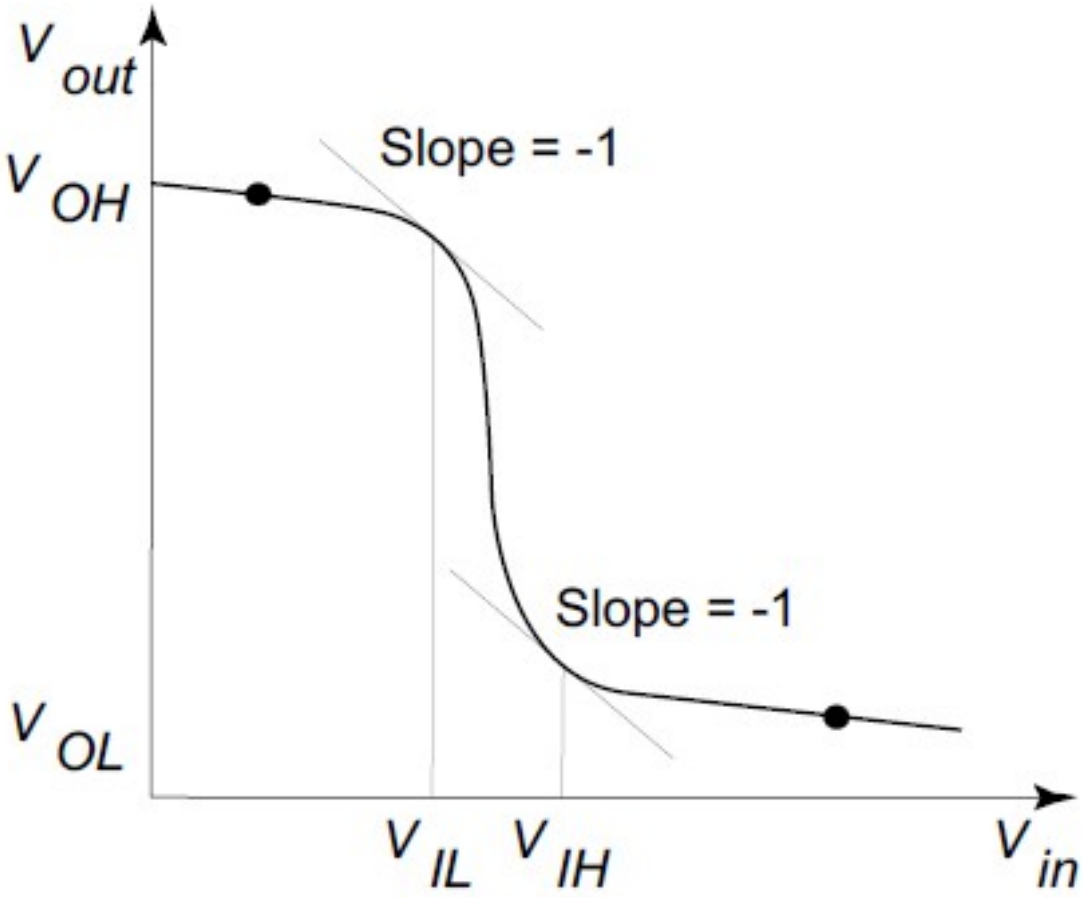


MOSFET n-channel

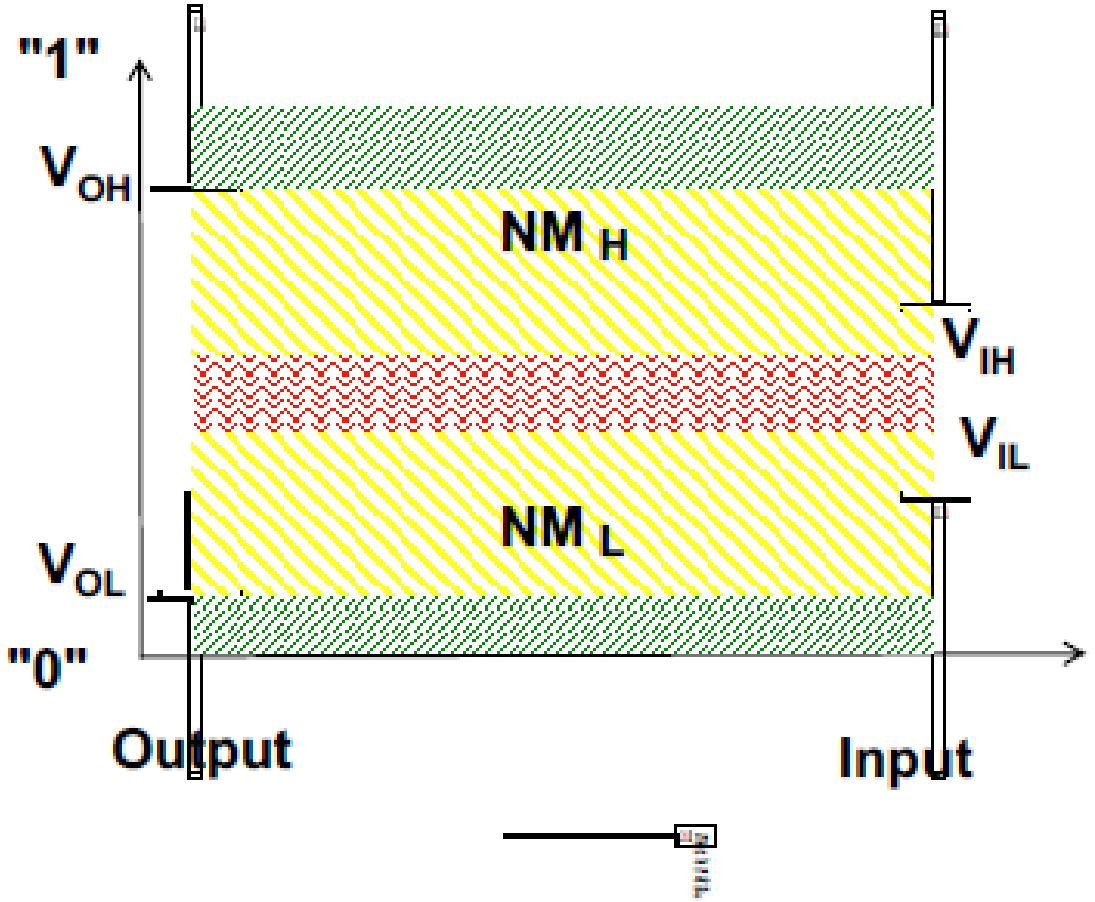


Mapping between Analog and Digital signals





Noise Margin



Noise margin high

Noise margin low

Introduction: CMOS Technology

MOS technology integrates both n-channel and p-channel transistors on the same chip.
If the substrate of the circuit is p-doped, the n-channel transistors sit directly on the substrate, whereas the p-channel devices need a well. This is a diffused layer with complementary doping compared to the substrate. The well is also called tub, while the technology is termed n-well technology.

For a n-type substrate the arrangement is complementary: the p-channel transistors are made in the substrate and the n-channel transistors sit inside the p-well. For the p-channel device the terms 'substrate' and 'bulk' have distinct meanings: 'substrate' refers to the whole slab supporting all devices, while 'bulk' refers to the n-well

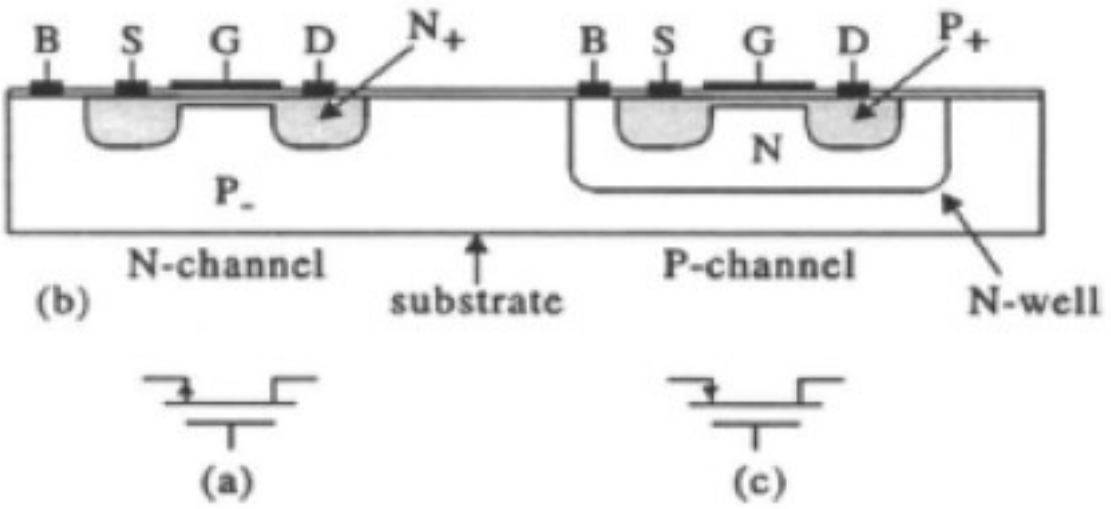
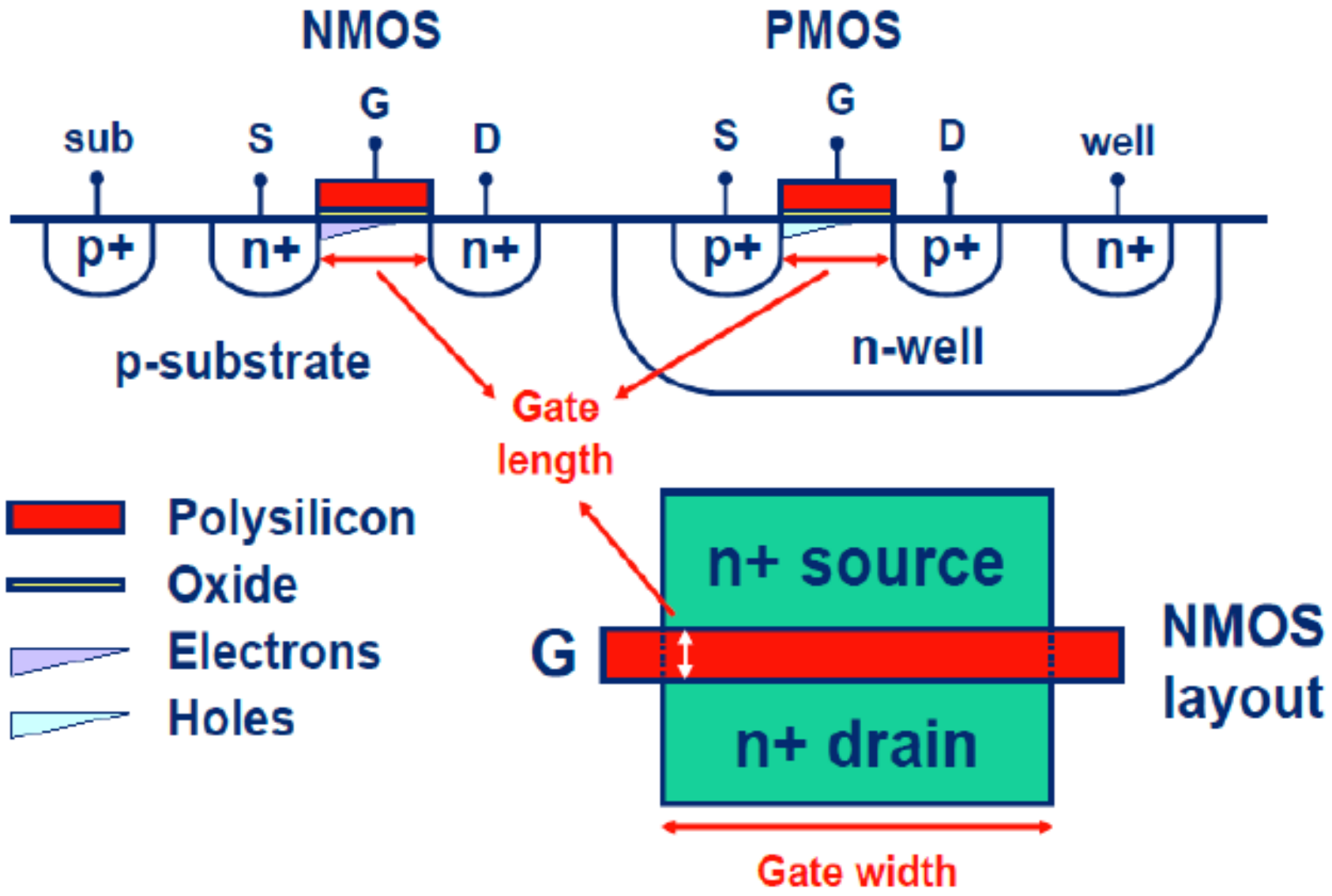


Fig. 8.3(b) CMOS N-well technology.
P_-: light P-channel doping $\approx 2 \times 10^{21}/m^3$.
N: moderate N-Channel doping $\approx 1.5 \times 10^{22}/m^3$.
N_+, P_+: heavy doping $> 10^{25}/m^3$
(a,c) Circuit symbols.

Introduction: CMOS Technology



Introduction: CMOS Technology

Cross section of a typical CMOS technology in figure. The substrate is *p*-type (often the substrate consists of a epitaxial layer (*p*-epi) grown on a *Si* substrate)

The *p*-well and the *n*-well are achieved with complementary mask using a phosphorous and boron implant respectively followed by a drive-in diffusion. The active area defines the region where transistors are located.

On the top of the active area we have a thin oxide (for 0.5μm technology it is *9-12nm* for a shorter channel-length the oxide is thinner; with a 0.35μm technology it is *5-7 nm*)

Around the active area there are structures made by highly doped region → achieve the so-called channel stop to avoid lateral current leakage.

Over the thin oxide there is the silicon gate that also separates the source and drain. Because of the lateral diffusions the source and the drain extend under the silicon gate leading to an overlap between the source (and the drain) and the silicon gate. In addition, the effective channel length is shorter than the designed length by a given extent

Fig. also shows a poly-poly capacitor.

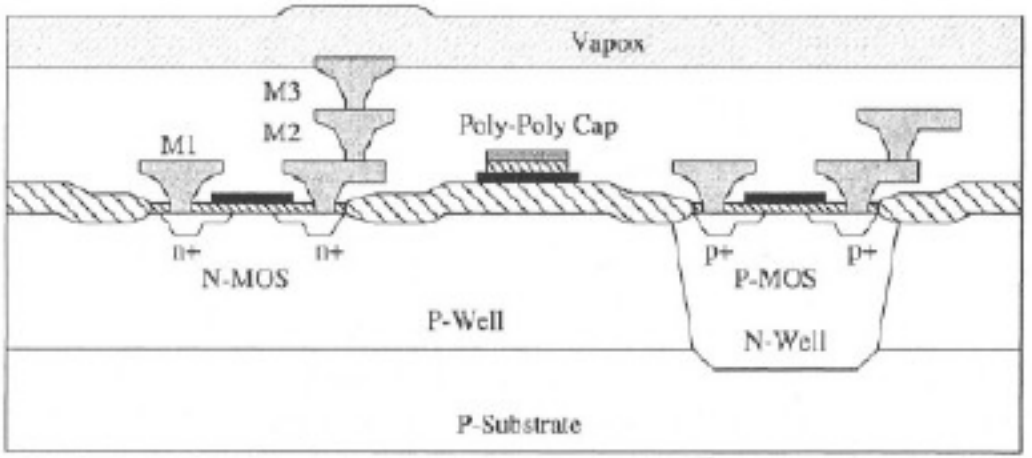
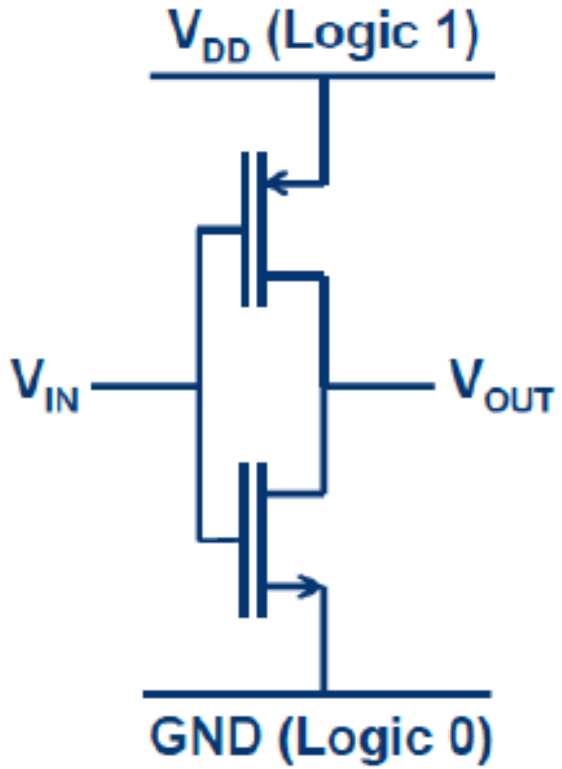


Fig. 1.10 - Cross section of a CMOS p-well circuit conteining an n-channel and a p-channel transistor

Introduction: why CMOS ? many reasons !

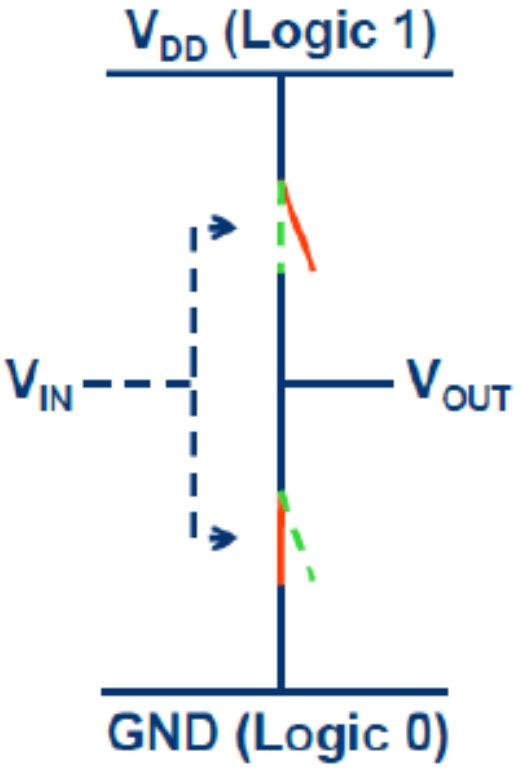


THE INVERTER

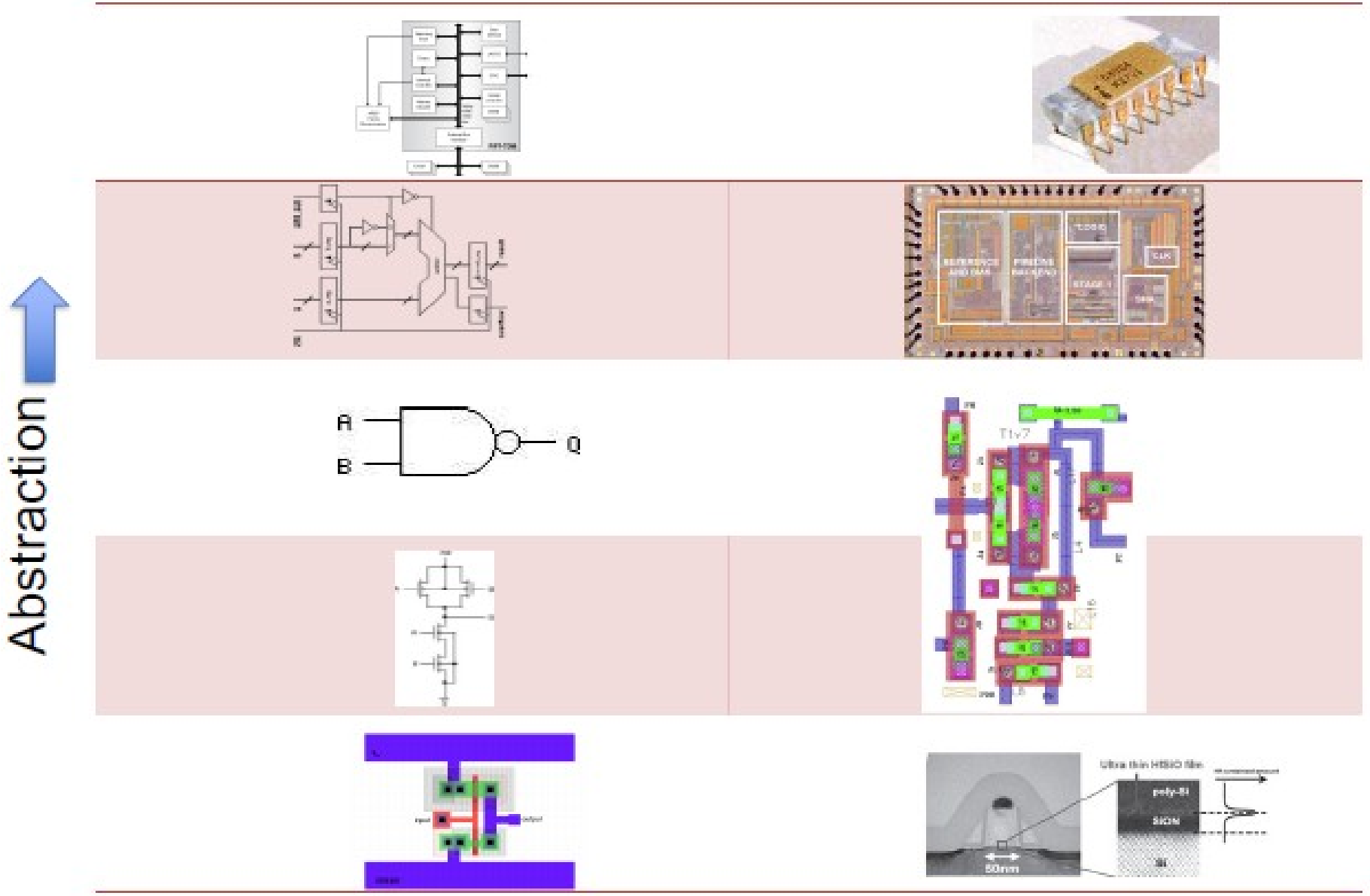
Truth table

IN	OUT
0	1
1	0

! low power consumption



Digital systems - Design Levels



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