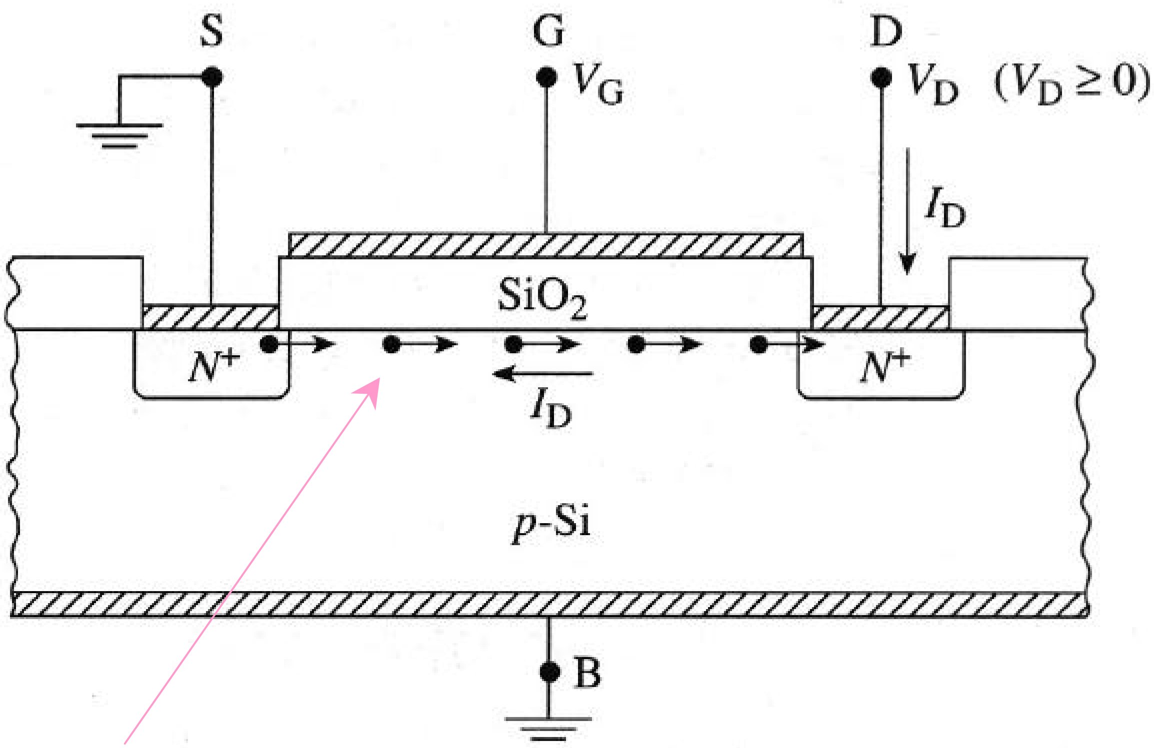
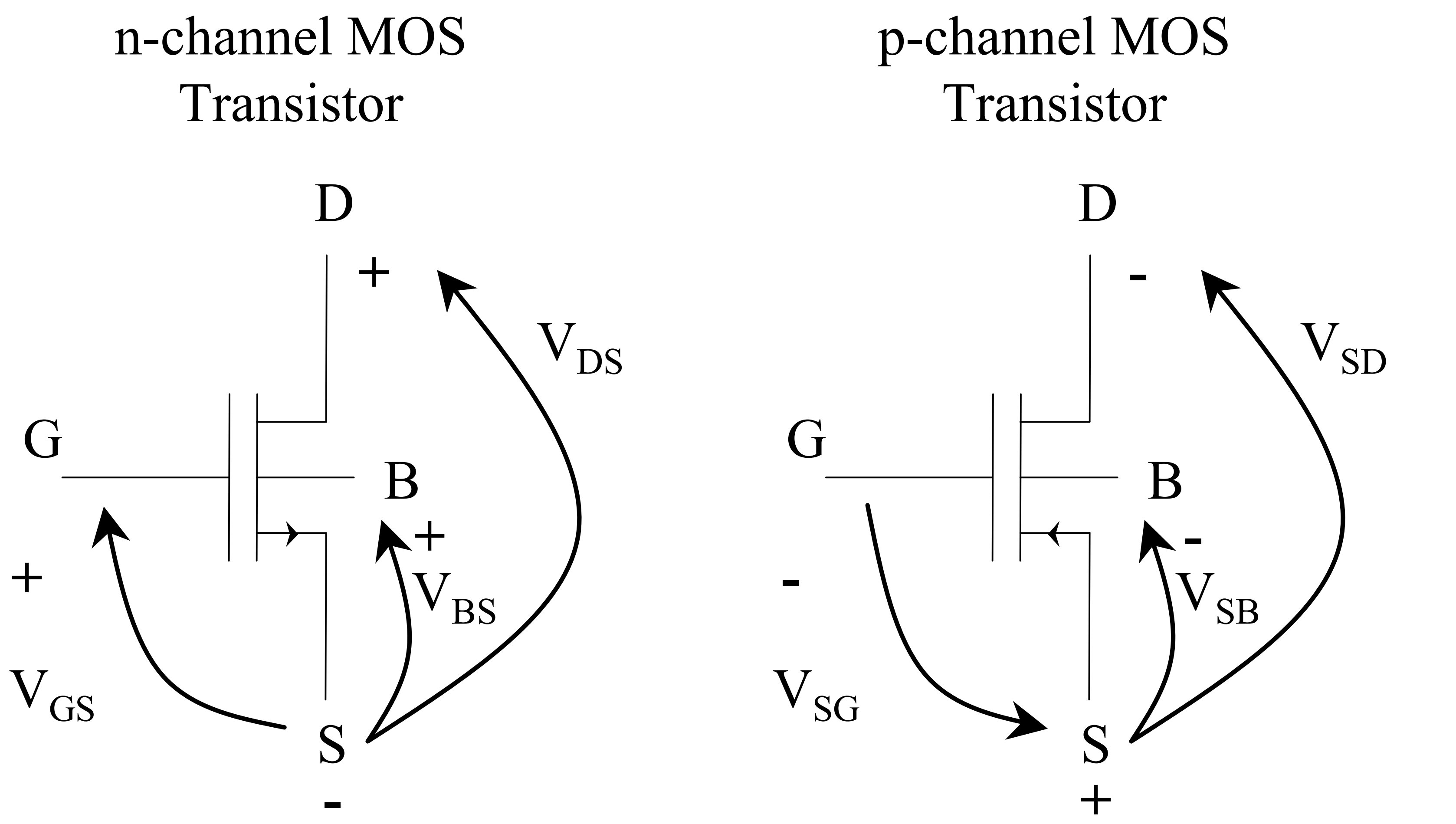
MOS Transistor
Qualitative Description

Flow of current from "Source" to "Drain" is controlled by the "Gate" voltage.



Control by the Gate voltage is achieved by modulating the conductivity of the semiconductor region just below the gate. This region is known as the channel

MOS Transistor
Qualitative Description



Note: All voltages are shown in their "positive " direction.
Obviously, $V_{YX}=-V_{XY}$ for any voltage

G=Gate, D=Drain, S=Source, B=Body (substrate, but to avoid confusion with substrate, B is used)

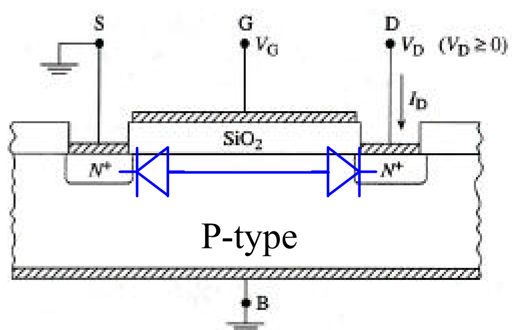
MOS Transistor

Qualitative Description

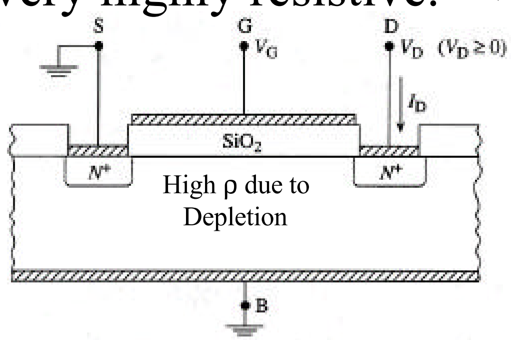
Assume an n-channel (receives it's name from the "type" of channel present when current is flowing) device with its source and substrate grounded (i. e., $V_S=V_B=0$ V).

For any value of V_{DS}:

•when $V_{GS}<0$ (accumulation), the source to drain path consists of two back to back diodes. One of these diodes is always reverse biased regardless of the drain voltage polarity.



•when $V_{GS}<V_T$ (depletion), there is a deficit of electrons and holes making the channel very highly resistive. => No Drain current can flow.

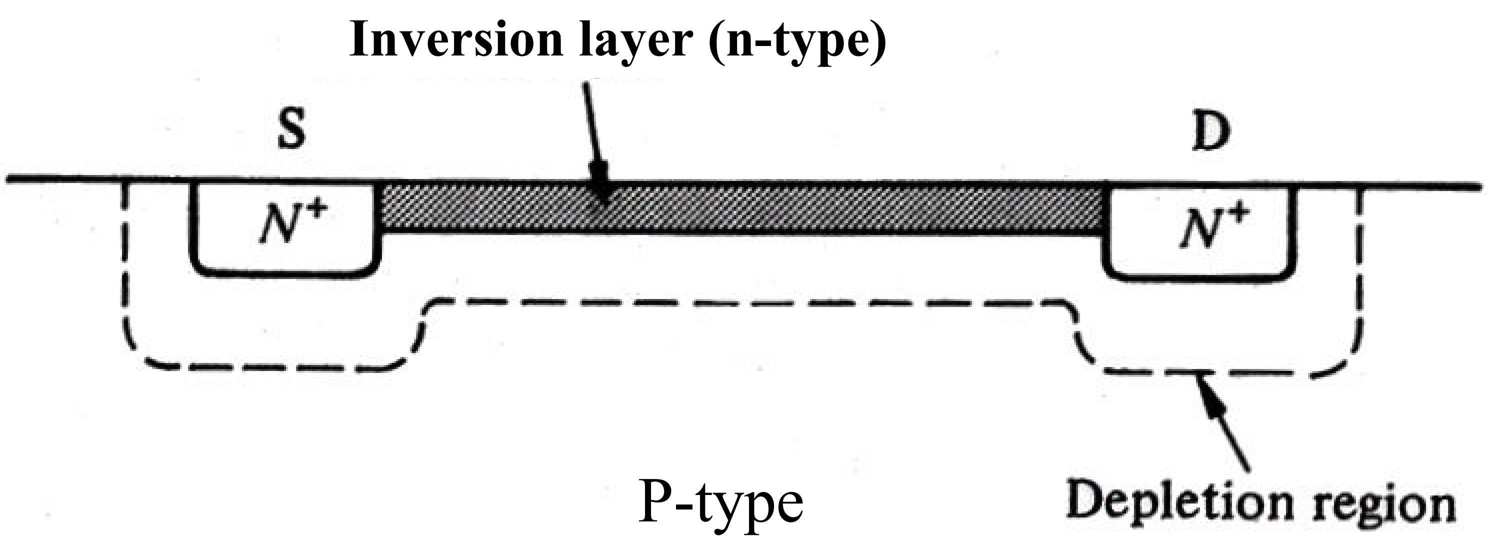


MOS Transistor
Qualitative Description

Consider now the Inversion case:

First, $V_{DS} = 0$:

- when $V_{GS} > V_T$, an induced n- type region, an "inversion layer", forms in the channel and "electrically connects" the source and drain.

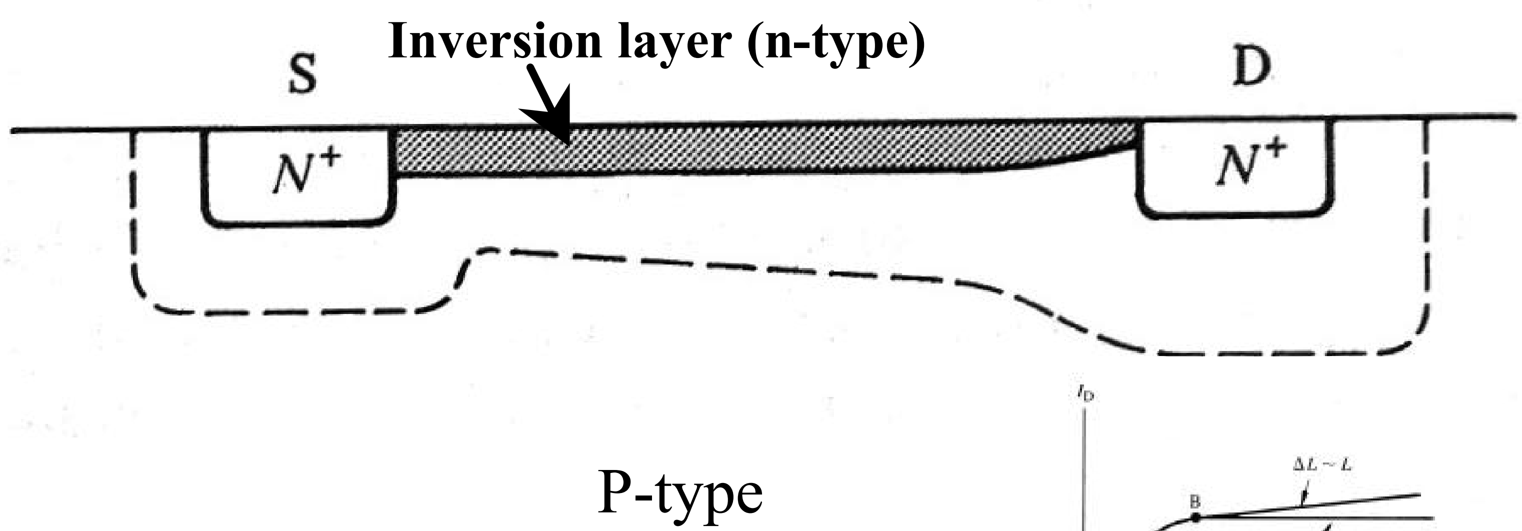


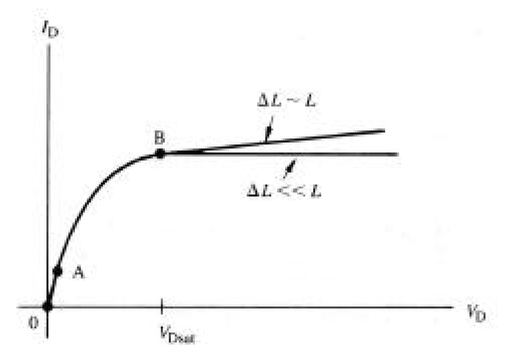
MOS Transistor

Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

When V_{DS} >0 , the induced n- type region allows current to flow between the source and drain. The induced channel ast like a simple resistor. Thus, this current, I_D, depends linearly on the Drain voltage V_D. This mode of operation is called the linear or "triode"* region.



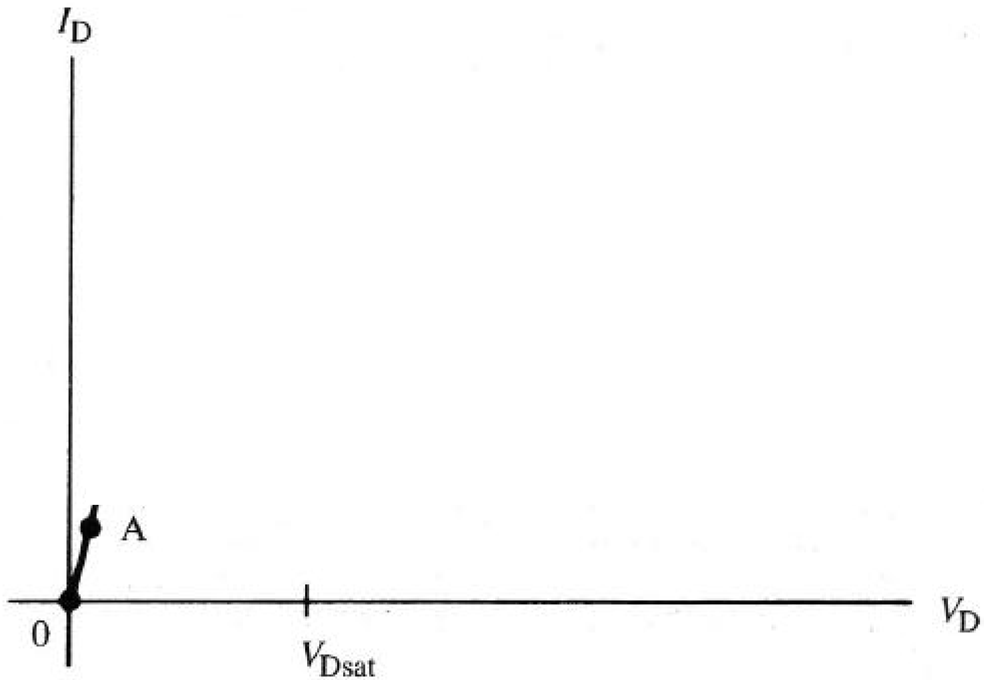


* "Triode" is a historical term from vacuum tube technology.

MOS Transistor
Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

Drain current verses drain voltage when in the linear or "triode"* region.



MOS Transistor

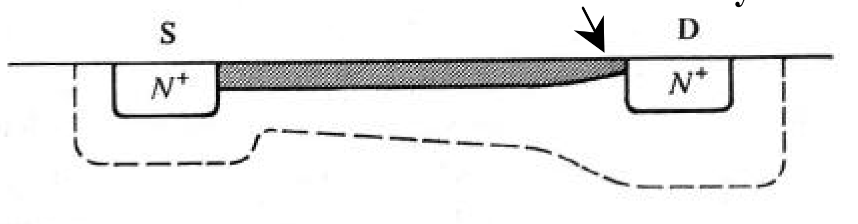
Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

When V_{DS} increases a few tenths of a volt (>0):

- The depletion region near the drain widens (N+ drain is positively biased – I.e. reverse biased with respect to the substrate).
- The electron concentration in the inversion layer near the drain decreases as they are "sucked out" by the Drain voltage.
- Channel conductance decreases resulting in adrop in the slop of the I_D-V_D curve.

Reduced electron concentration in the Inversion layer bear the drain



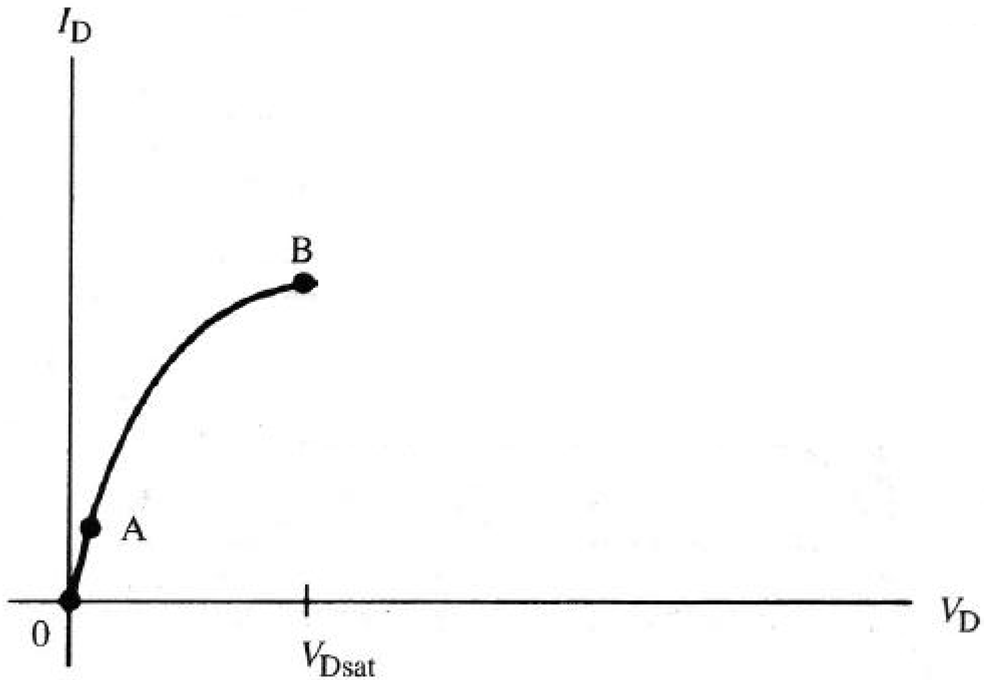
P-type

MOS Transistor

Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

Drain current verses drain voltage for increasing V_{DS} (still in the "linear" or triode region).

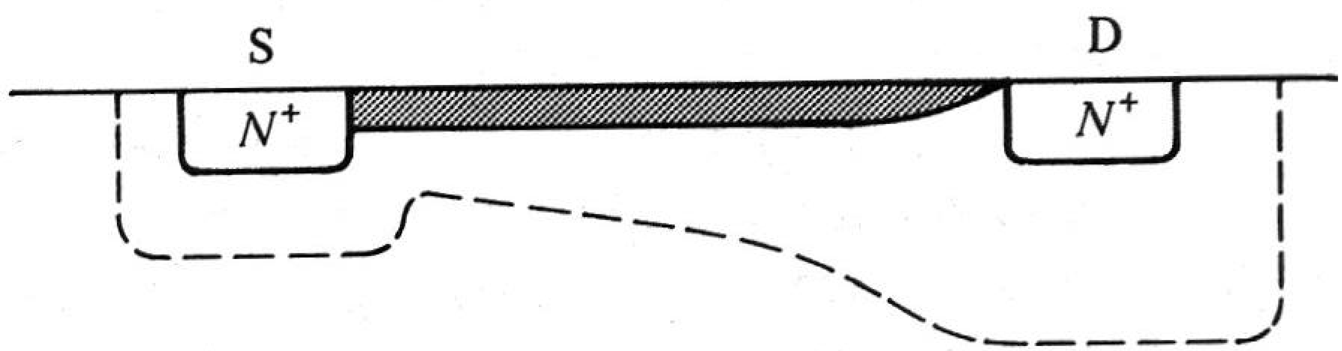


MOS Transistor
Qualitative Description

Inversion case, $V_{GS} > V_{T(\text{continued})}$:

The inversion layer eventually vanishes near the drain end of the channel.

This is called "Pinch-Off" and results in a Flat I_D-V_{DS} curve



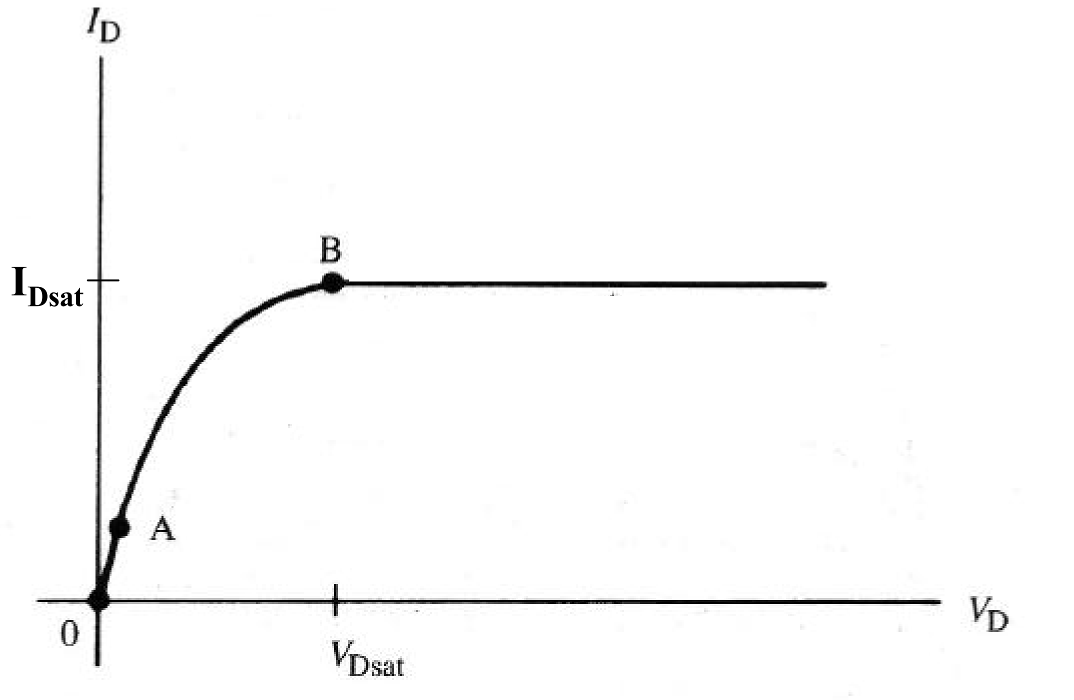
MOS Transistor

Qualitative Description

Inversion case, $V_{GS} > V_{T}$(continued):

I_D-V_{DS} curve for the "Saturation Region"

The drain-source voltage, V_{DS}, at which this occurs is called the saturation voltage, V_{sat} while the current is called the saturation current, I_{Dsat}.

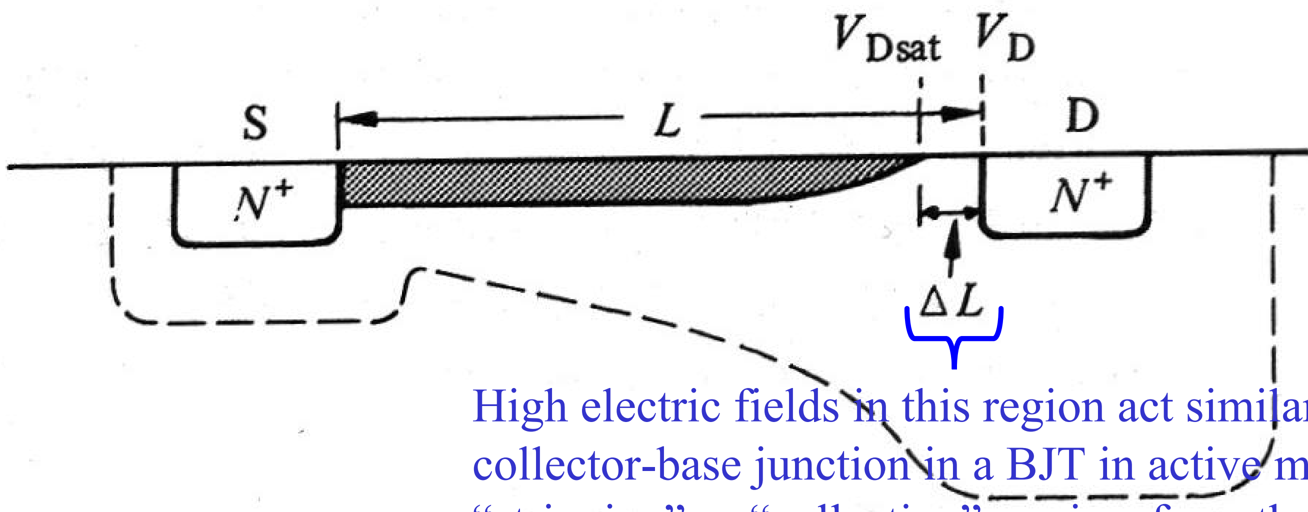


MOS Transistor
Qualitative Description

Inversion case, $V_{GS} > V_{T(continued)}$:

For $V_{DS}>V_{sat}$ the channel length, L, effectively changes by a value ΔL.

The region of the channel, ΔL is depleted and thus, is high resistivity. Accordingly, almost all voltage increases in $V_{DS}>V_{sat}$ are "dropped across" this portion of the channel.



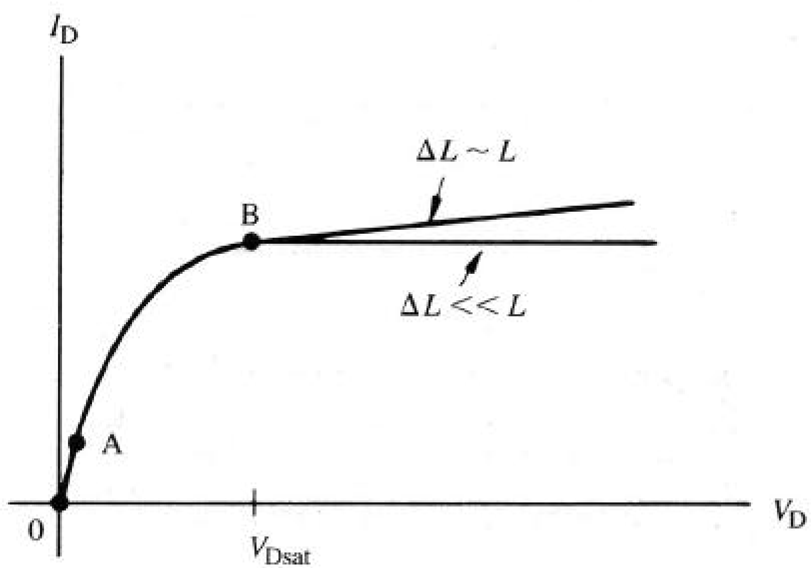
High electric fields in this region act similarly to the collector-base junction in a BJT in active mode, "stripping" or "collecting" carriers from the channel.

MOS Transistor
Qualitative Description

Inversion case, $V_{GS} > V_{T(\text{continued})}$:

If $\Delta L << L$, the voltage at the end of the channel will be constant (V_{sat}) for all $V_{DS} > V_{sat}$. I_D will be constant.

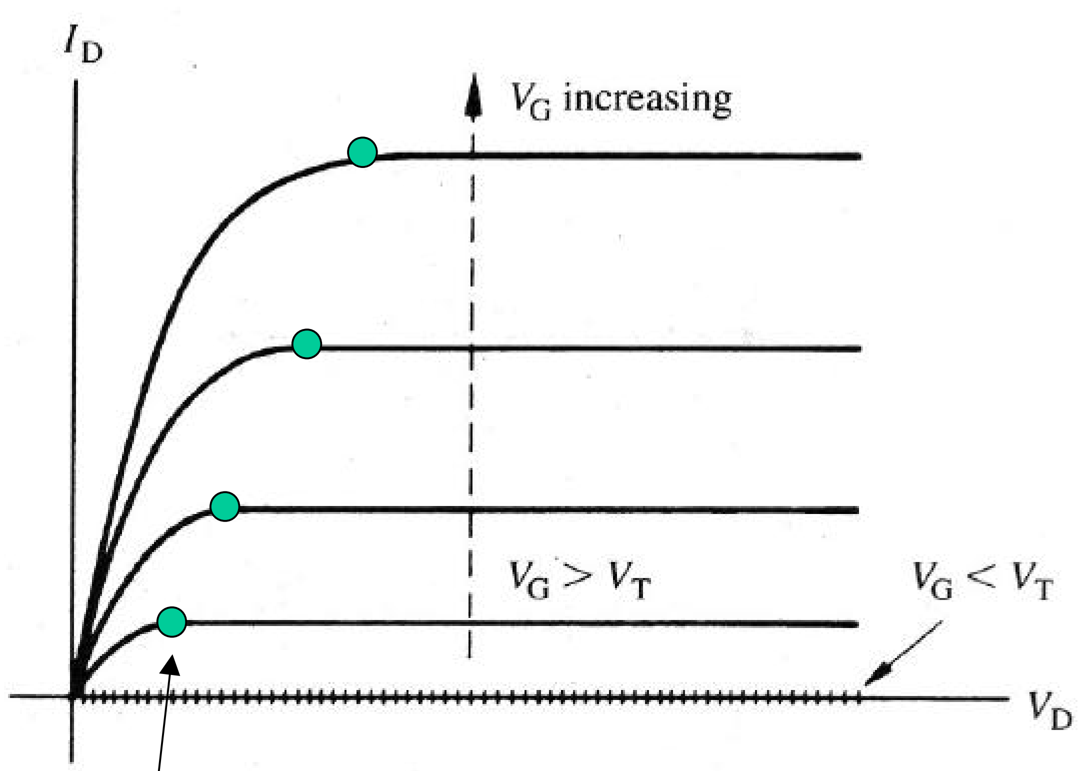
If $\Delta L \sim L$, the voltage dropped across the the channel (V_{SAT}) varies greatly with V_{DS} due to large modulations in the electric field across the pinched off region ($E=[V_{DS}-V_{SAT}]/[\Delta L]$). In this case, I_D increases slightly with V_{DS}.



MOS Transistor
Qualitative Description

Finally,

I_D-V_{DS} curves for various V_{GS}:



V_{Dsat} depends on V_G