School of Energy System

Master`s Program in Electrical Engineering

BL30A1321 - Modelling and Control of Power Electronic Converters

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Simulation Of A Power Electronic Converter

Modelling And Control of A Three-Phase Grid Connected Converter

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ABSTRACT

Firstly, a three-phase grid-connected inverter is modelled in Simulink, the Park’s transformation is applied to its voltage and current measurements and the angle reference for the transformation is computed by a PLL. Then the current and DC-link voltage control is implemented and tuned and the control parameters are tested in a simulation in the Simulink environment under different operating conditions. In the end, the modelling of an unbalanced system is explained and tested by simulating a SLG fault.

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Converter Modelling

Inverter, RL Filter And Network Modelling

A three-phase inverter is a power device able to convert an input DC voltage into an AC voltage at a particular frequency and it's currently used for a wide range of applications, in particular those regarding the integration of renewable energy sources in the electric system. In fact it's usually placed as an interface between the renewable source, such as in PV-farms or in wind farms, and the grid to synchronize the unit outputs with the network: in this case a grid-connected inverter is studied, so the selected output frequency is the grid frequency equal to $f_{grid} = 50$ Hz.

In the circuit model in Simulink, the converter is modelled by using ideal switches that are controlled with the signal of a 2-level PWM generator as shown in *Figure 1*. The selected switching frequency is $f_s = 2500$ Hz.

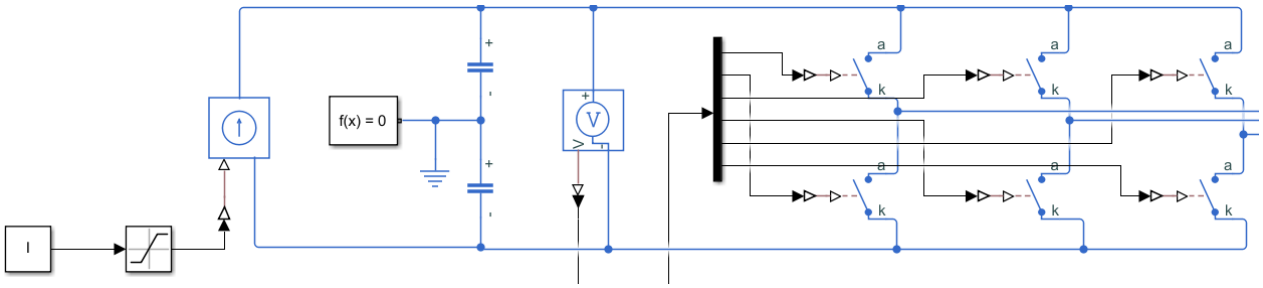


Figure 1 - Inverter model

The DC voltage is given by a two capacitors of capacitance $C_{dc} = 10$ mF placed in series between phase and neutral on the DC side of the converter. They can be seen as an equivalent element of capacitance equal to $C_{dc}/2 = 5$ mF and each of them is initialized with a voltage value of $V_{dc}/2$, in such a way that at time $t = 0$, the DC-link voltage is equal to 690 V as shown in *Figure 2*.

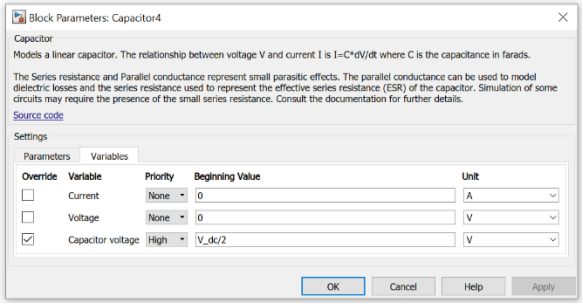


Figure 2 - DC-link initialization

In normal operating condition, current flows from the source on the DC side, which is modelled as a current-controlled current source, to the grid on the AC side without flowing into the capacitor, meaning that $P_{dc} = P_{inv}$ and in particular $i_{dc} = i_{inv}$ with $i_C = 0$. Since the inverter has a maximum power of $A_{inv} = 50$ kVA, the maximum DC current that is allowed to flow through the inverter is equal to $A_{inv}/V_{dc} = 72$ A: in fact as it's possible to observe again in *Figure 1*, a saturation block is placed to limit it.

The three-phase inverter is connected to a RLC low-pass filter, shown in *Figure 3*, which is used to filter the voltage and current output: in fact the converter causes interference on the signal, leading to a higher frequency content in the outputs, and this phenomena increases with the switching frequency. Since the network needs to guarantee a suitable level of voltage quality for technical reasons, for example due to the fact that electrical devices are designed to work on a specific voltage and they are able to handle just little variations of that, the output variables needs to be cleared from higher frequency harmonics.

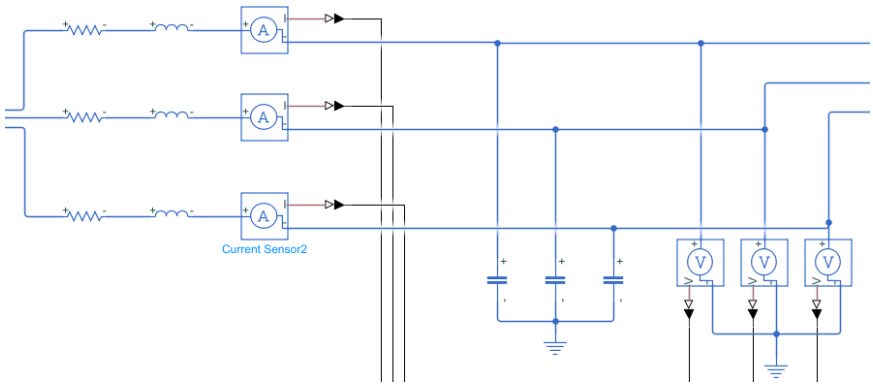


Figure 3 - RLC filter

The filter parameters are selected in order to achieve a cut-off frequency of the RL filter equal to the grid frequency: consequently $R = 0.314\ \Omega$ and $L = 1$ mH are the chosen parameters since the transfer function is the one written below in (1) and its frequency behaviour in shown in *Figure 4*. Then, in parallel between the phases and the ground, a capacitor equal to $C = 6$ mF is added: the transfer function of the RLC filter has a resonance near the grid frequency, as it's possible to see from *Figure 5* that represent the frequency behaviour of the RLC filter, but it's amplitude is small, so it shouldn't cause any problem.

$$RL(s) = \frac{1}{sL + R} \tag{1}$$

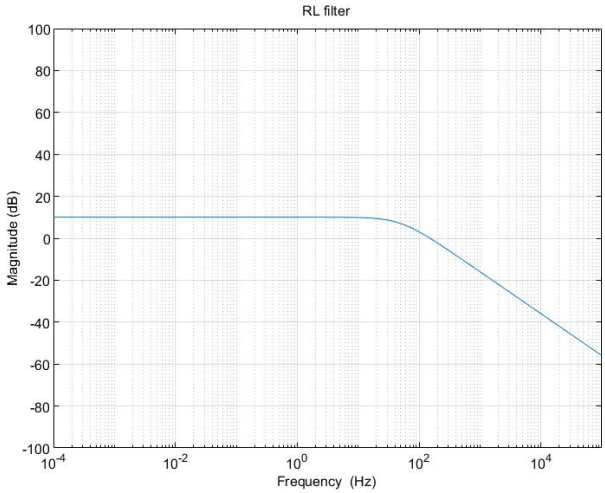


Figure 4 - Frequency behaviour of the RL filter

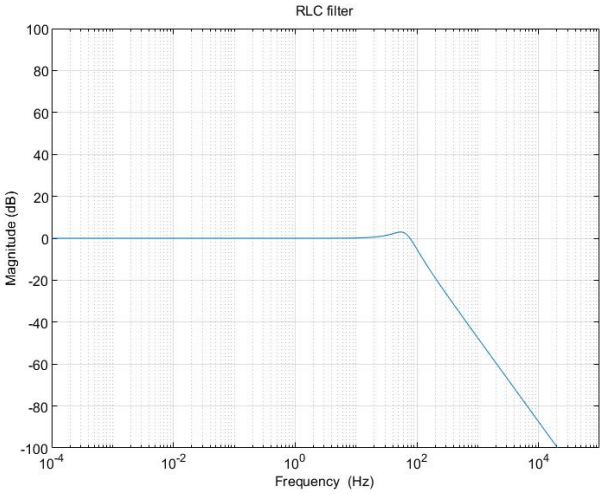


Figure 5 - Frequency behaviour of the RLC filter

Then the converter is connected to the grid which is modelled as an ideal and symmetrical three-phase voltage source: all the phases have the same phase-to-phase RMS voltage magnitude equal to $V_a = V_b = V_c = 400$ V and phase b and phase c are respectively shifted of $\phi_b = -2/3\pi$ and $\phi_c = -4/3\pi$ with respect to phase a which is initialized to $\phi_a = 0$.

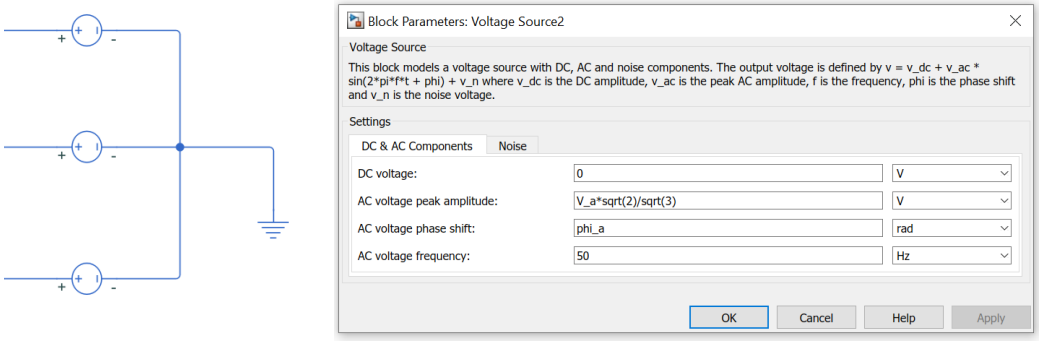
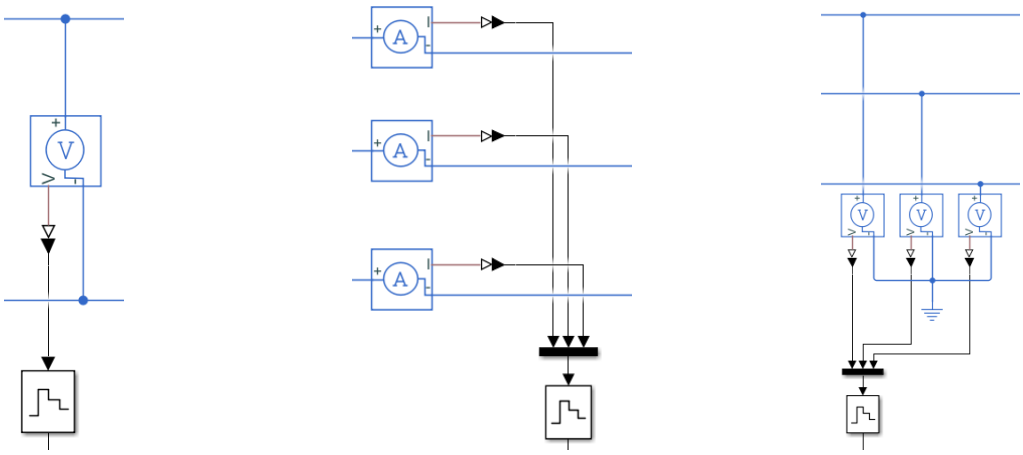


Figure 6 - Grid model and parameters

Synchronous Reference Frame And PLL

Output currents and voltages are measured through a current or voltage sensors, then a Zero-Order Holder (ZOH) is used to re-build the continuous-time signal from the samples. A sampling frequency equal to $f_{sampling} = 2f_s = 5000$ Hz is chosen.



(a) DC-Link (b) Line currents (a) Phase voltages

Figure 7 - Current and voltage measurements and sampling

These variables are then transformed into a synchronous reference frame: firstly, a Clarke's transformation is performed and the three-phase *abc* variables are modified into another three-phase $\alpha\beta 0$ variables in which the α and β components are shifted of 90° between each other. Then those components are transformed again into another three-phase $dq0$ variables in a reference that is synchronised with the phase voltage. The zero-component is neglected since in this case it isn't relevant.

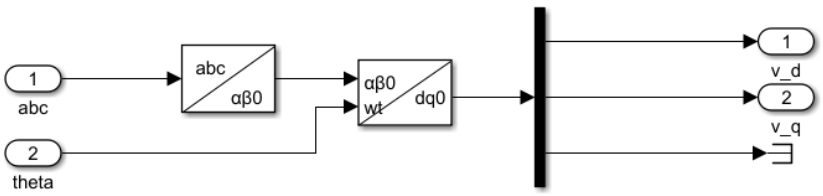


Figure 8 - Alpha-beta-0 and d-q-0 transformations

For the sake of simplicity, the full transformation just for voltage variables is shown below in (2) (Clarke's transformation) and (3) ($\alpha\beta$-dq transformation), but it's applied to both voltages and currents.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3}$$

This methodology is used to achieve a control signal that is stable at steady-state in order to improve the performance of the converter control system: in fact, in case of a symmetrical three-phase system, the d-component is constant and the q-component should be equal to zero.

The angle θ that is used to synchronise the reference frame with the grid voltage is computed by a Phase-Locked Loop (PLL) that uses the voltage q-component as a signal error for a feedback control system to adjust the frequency, so the phase. It's composed by:

- A Phase Detector, which is in this case incorporated in dq-transform since the q-components is used as signal error, that represents the phase difference between two signals. Since the q-component is zero in a symmetric three-phase system, that means that the phase difference should be null.
- A Loop Filter which is used to remove the high frequency content from the error signal. Its transfer function is the one written below in (4).

$$LF(s) = \frac{k_P T_I s + k_P}{T_I s} \tag{4}$$

- A Voltage-Controlled Oscillator (VCO) which produces the output controlled signal frequency that is then integrated to produce the angle reference for the frame.

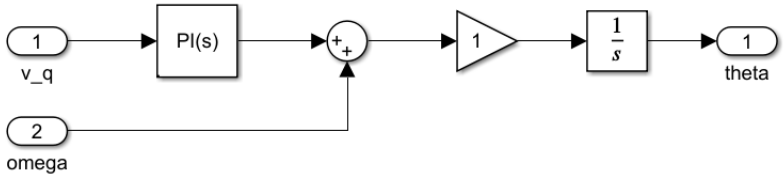


Figure 9 - PLL

Converter Control

Current Control

The current control loop is characterized by the transfer function of a PI controller, of the PWM and of the RL filter: the PI controller takes the signal error between the current reference and the current measurement as input (the proportional gain k_P takes into account the current value of the error, while the integral gain k_I consider the value assumed by the error in the previous step), then this signal is sent to the PWM which provides the switching signal for the opening/closing of the switches and in the end the current is measured again after the RL filter to compute this loop once more. In this simulation, this feedback control is applied to both current d and q-components.

The current reference for the q-component is set equal to zero, while the reference of the d-component is the output of the DC voltage control that is going to be explained later on.

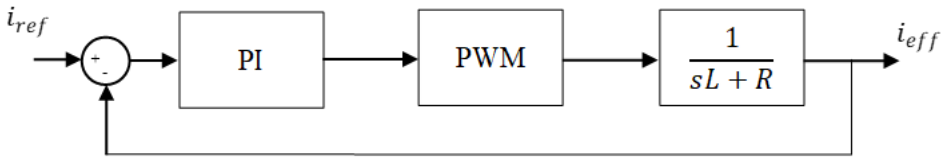


Figure 10 - Current control loop

The PWM is modelled as a delay of $T = 1.5T_s$ as expressed in (6) in which T_s is the sampling period:

$$T_s = \frac{1}{f_{sampling}} = \frac{1}{2f_s} = 0.2\ ms \tag{5}$$

$$PWM(s) = \frac{2 - Ts}{2 + Ts} \tag{6}$$

Therefore, the open-loop transfer function of the current control is the following expression:

$$G_{co}(s) = \frac{k_{Pc}s + k_{Ic}}{s} * \frac{2 - Ts}{2 + Ts} * \frac{1}{sL + R} \tag{7}$$

While the closed-loop transfer function becomes:

$$G_{cc}(s) = \frac{G_{co}(s)}{1 + G_{co}(s)} \tag{8}$$

In Simulink, the current control loop is implemented as shown in *Figure 11*.

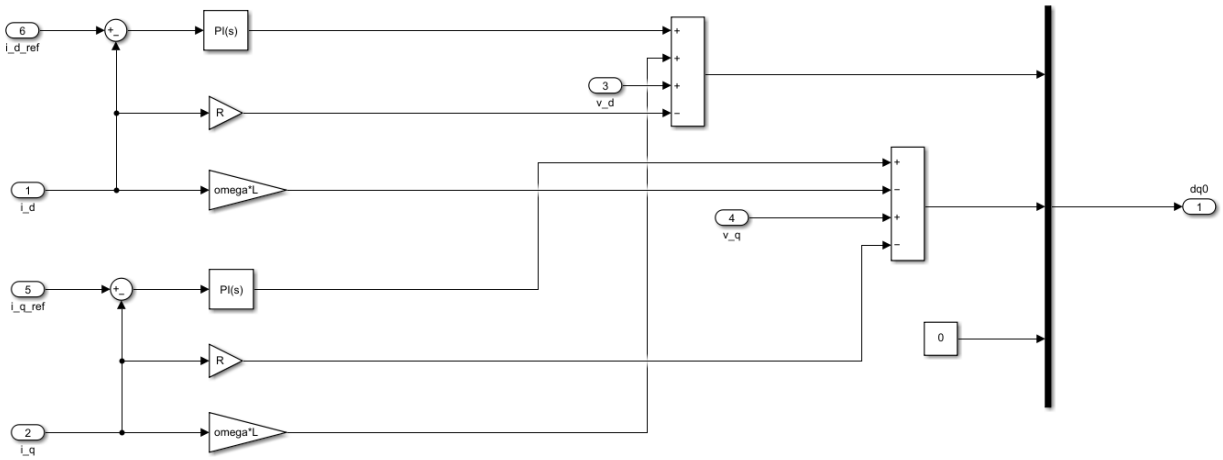


Figure 11 - Current control loop

Tuning Of The Current PI Controller

The current PI controller is tuned with an approach called Internal Model Control (IMC). First of all the bandwidth α of the controller is computed, according to the current rise time that in this simulation has been chosen as $t_{rise} = 3$ ms. The corresponding bandwidth is equal to:

$$\alpha = \frac{ln(9)}{t_{rise}} = 732.408 \tag{9}$$

Then the parameters of the PI controller can be selected as:

$$k_{Pc} = \alpha L = 0.732 \tag{10}$$

$$k_{Ic} = \alpha R = 229.976 \tag{11}$$

The stability of the closed-loop can be tested with the Nyquist criterium by plotting the Nyquist diagram of the open-loop transfer function. As it's possible to observe from *Figure 12*, the diagram doesn't spin around the critical point (-1,0) and, since the transfer function doesn't have either poles with positive real parts, the criterium is satisfied, meaning that the closed-loop system with these control parameters is stable.

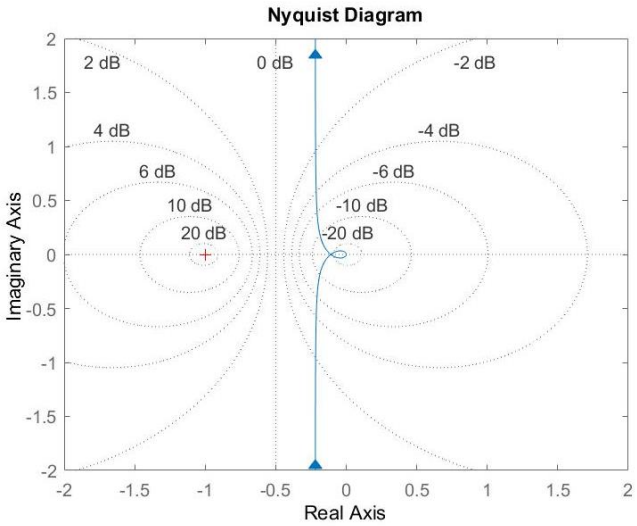


Figure 12 - Current Nyquist diagram

Those shown below in *Figure 13* represent the sensitivity functions of the current control loop: the closed-loop transfer function has a low-pass behaviour and its speed is proportional to the width of the bandwidth: the higher the gain, the greater the velocity of the control, but if it's too high it can lead to stability problems, even if this doesn't happen in this case.

Moreover, the noise sensitivity presents a bigger gain at higher frequencies than the lower ones, but anyway it's still lower than 0 dB. The load sensitivity instead has a magnitude peak close to the grid frequency but, also in this case, the value always remains lower than 0 dB, meaning that at most the noise will pass unaltered ($1 = 0$ dB), but it won't be amplified.

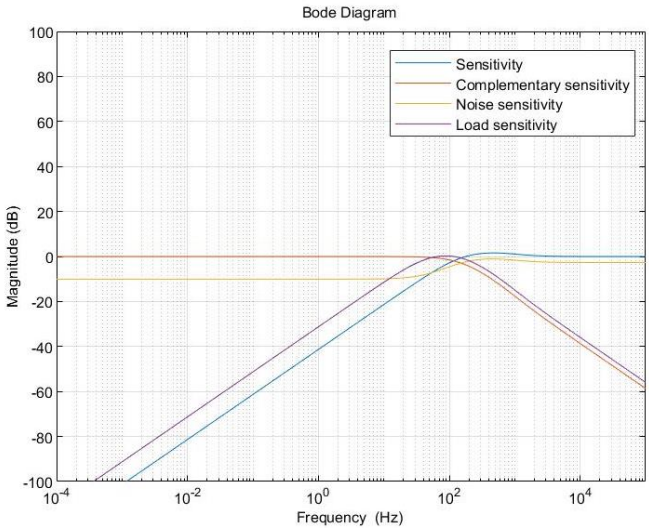
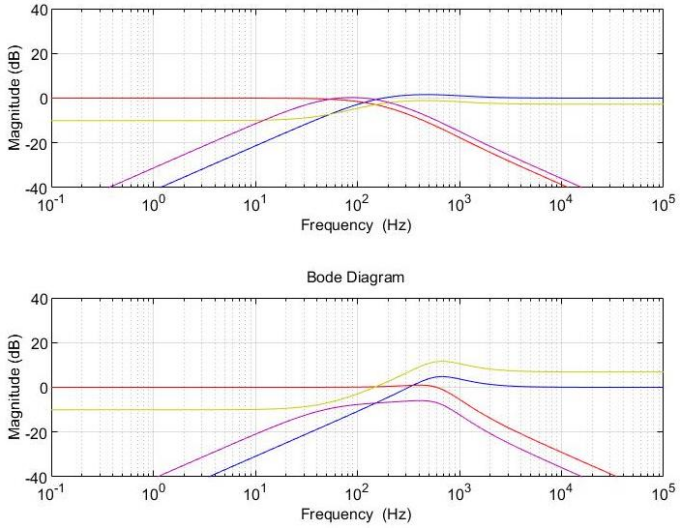


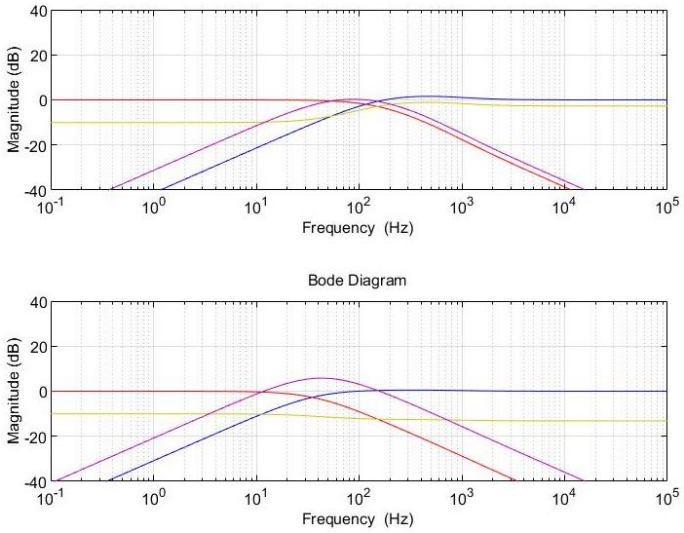
Figure 13 - Current sensitivity functions

As highlighted in *Figure 14*, changing the rise time has an effect on the bandwidth of the controller:

- If a rise time equal to 1 ms is chosen, the bandwidth α increases, so the cut-off frequency is shifted to the right of the Bode diagram, but the noise sensitivity increases at higher frequencies, while the load sensitivity decreases near the grid frequency.
- If a rise time of 10 ms is selected, the bandwidth α decreases and the cut-off frequency is shifted to the left, while the noise sensitivity decreases at higher frequencies and the load sensitivity increases near the grid frequency.



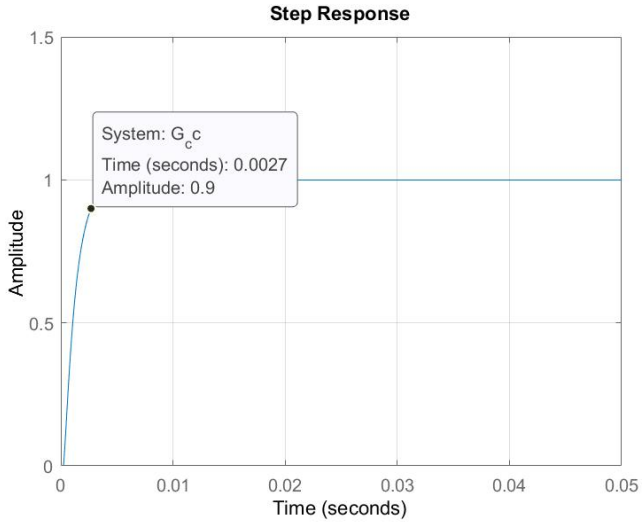
(a) Sensitivity functions with $t_{rise} = 1$ ms



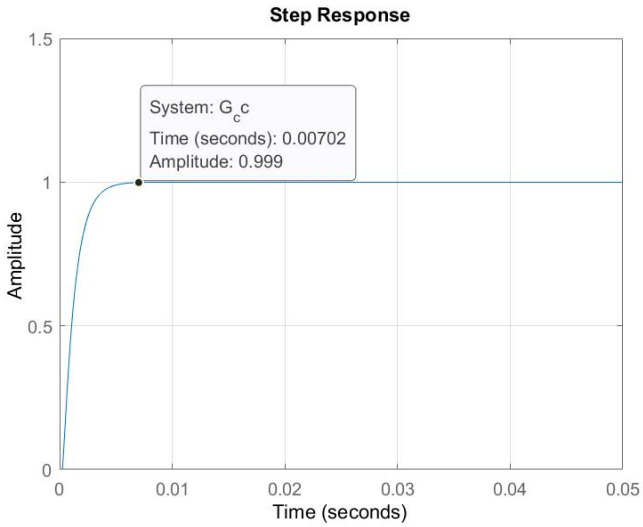
(a) Sensitivity functions with $t_{rise} = 10$ ms

Figure 14 - Comparison between sensitivity functions

The current rise time is then tested by plotting the step response of the closed-loop transfer function that is provided in *Figure 15*. As it's possible to point out, the current reaches 90% of its final value after 2.7 ms and the steady-state in about 7 ms. The IMC tuning approach doesn't take into account the delay caused by the PWM and the sampling, so it's normal that the simulated rise time doesn't match with the set one.



(a) Current rise time



(b) Current steady-state

Figure 15 - Current step response

Voltage Control

The voltage control loop consists of the transfer functions of the PI controller, the closed-loop current control and the DC-link. In this case, the PI controller takes the signal error between the DC voltage reference and the DC measured voltage as input, then this signal is processed by the current control which provides the opening/closing signal for the switches in order to adjust the output voltage and in the end the DC voltage is measured again to compute this loop once more. In the simulation, this approach is applied just to the d-component in order to create the reference for the d-current, since the reference for the q-current is set at priori equal to zero.

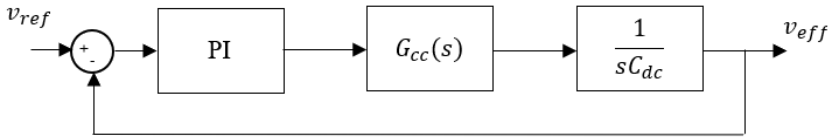


Figure 16 - Voltage control loop

Therefore, the open-loop transfer function of the voltage control is the following:

$$G_{vo}(s) = \frac{k_{Pv}s + k_{Iv}}{s} * G_{cc}(s) * \frac{1}{sC_{dc}} \tag{12}$$

While the closed-loop transfer function becomes:

$$G_{vc}(s) = \frac{G_{vo}(s)}{1 + G_{vo}(s)} \tag{13}$$

In Simulink, the current control loop is implemented as shown in *Figure 17*.

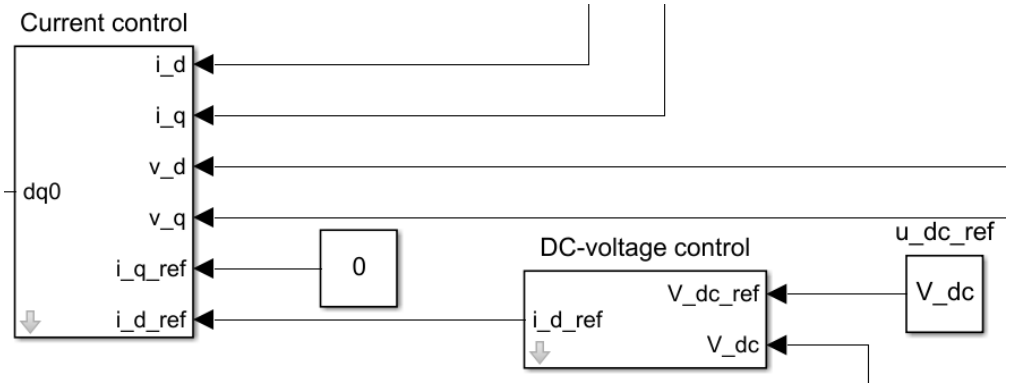


Figure 17 – DC-link voltage control loop

Tuning Of The Voltage PI Controller

The PI controller of the voltage loop can be tuned looking at the root locus: since the current control loop can be approximated with its dominant pole α as shown in (14) and it has a time-constant $T_\alpha = 1.4$ ms, the integrator time T_{Iv} of the voltage PI controller is chosen equal to $a^2 T_\alpha = 12.3$ ms in which $a = 3$ is assumed, in such a way that the voltage control loop is slower than the inner current loop.

$$G_{cc(app)} = \frac{\alpha}{s + \alpha} \tag{14}$$

$$T_\alpha = \frac{1}{\alpha} \tag{15}$$

By plotting the root locos of the open-loop transfer function shown in *Figure 18* when $k_{Pv} = 1$, it's possible to observe that its behaviour is dominated by the pole near the zero. So a proportional gain $k_{Pv} = 1.29$ is selected in order to have pole with frequency of 161 rad/s, so a time constant of 6.2 ms should be present.

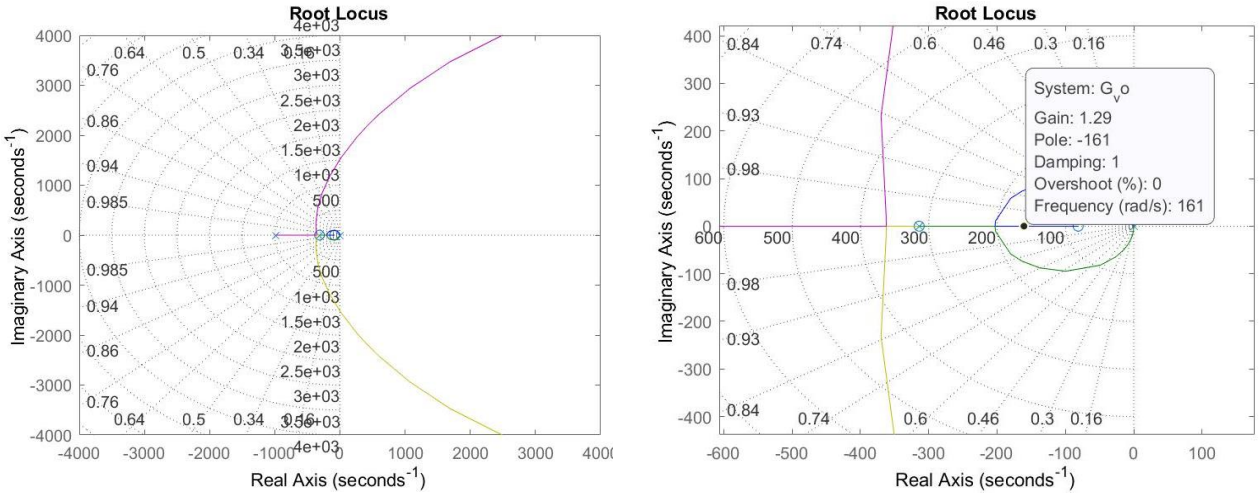


Figure 18 - Voltage root locus

This choice leads to the parameters express in (16) and (17) for the voltage PI controller:

$$k_{Pv} = 1.29 \tag{16}$$

$$k_{Iv} = \frac{k_{Pv}}{T_{Iv}} = 81.379 \tag{17}$$

The stability of the closed-loop can be tested with the Nyquist criterium by plotting the Nyquist diagram of the open-loop transfer function. As it's possible to observe from *Figure 19*, the diagram doesn't spin around the critical point (-1,0) and, since the transfer function doesn't have either poles with positive real parts, the criterium is satisfied, meaning that the closed-loop system with these control parameters is stable.

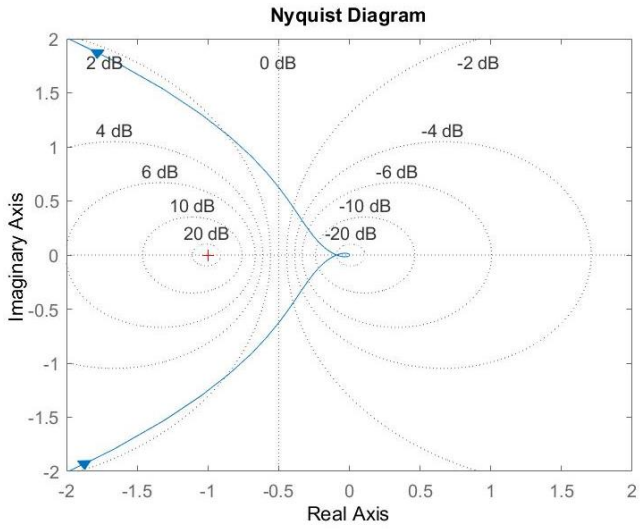


Figure 19 - Voltage Nyquist diagram

Those shown below in *Figure 20* represent the sensitivity functions of the voltage control loop: the closed-loop transfer function has a low-pass behaviour as well as the closed-loop transfer function of the current control, but also in this case the gain isn't too high to cause stability problems.

The noise sensitivity has a bigger gain at higher frequencies, as it happens before for the current control loop, and in this case it's a bit higher than 0 dB. Moreover, the load sensitivity is damped at lower frequencies, but it has a magnitude peak near the grid frequency as in the previous case.

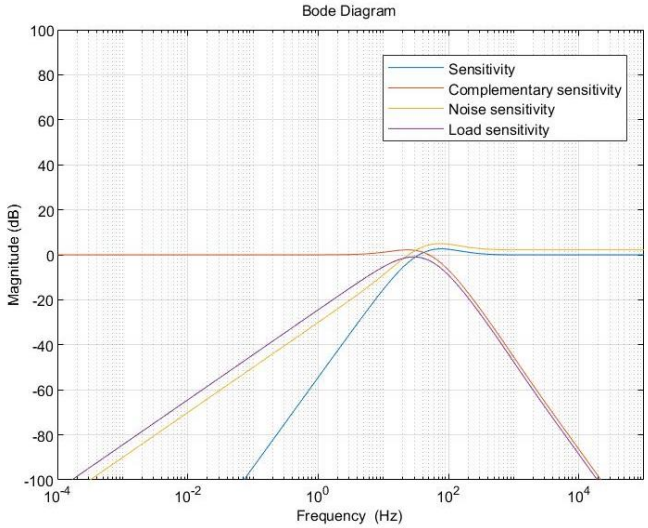


Figure 20 - Voltage sensitivity functions

The voltage behaviour is then tested by plotting the step response of the closed-loop transfer function that is provided in *Figure 21*. As it's possible to point out, the voltage reaches the steady-state in about 50 ms whit an overshoot of 26%.

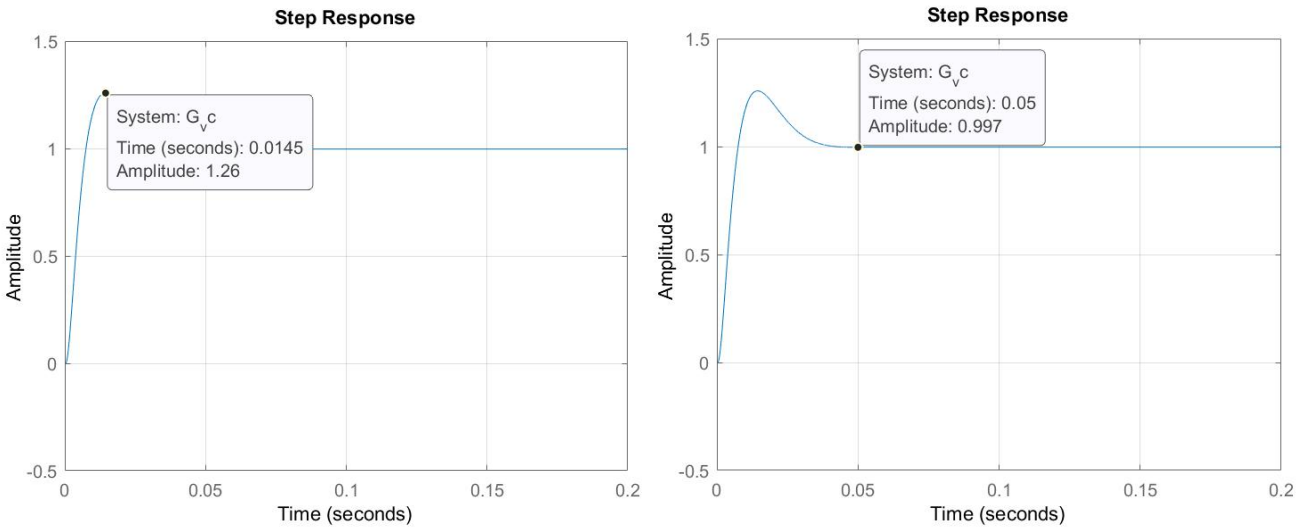


Figure 21 - Voltage step response

PLL Tuning

In the PLL, the Loop Filter should be tuned and its transfer function is shown below in (18): a damping $\zeta = 1$ and a settling time equal to $t_{settling} = 1$ s has been chosen in order to compute the gain k_P and the integrator time T_I as highlight in (19) and (20).

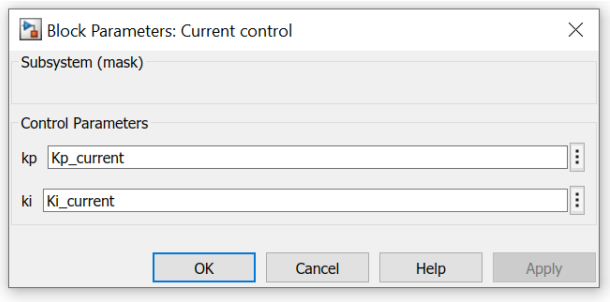
$$LF(s) = \frac{k_P T_I s + k_P}{T_I s} \tag{18}$$

$$k_P = \frac{9.2}{t_{settling}} = 9.2 \tag{19}$$

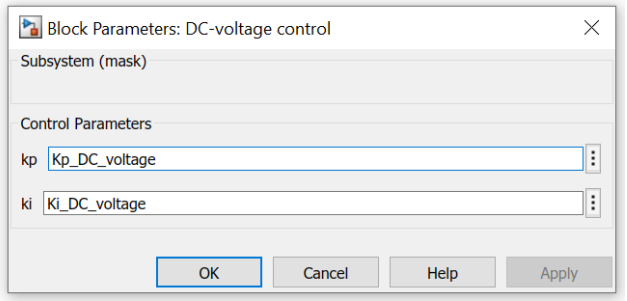
$$T_I = \frac{t_{settling}\zeta^2}{2.3} = 0.435 \tag{20}$$

Simulation Results

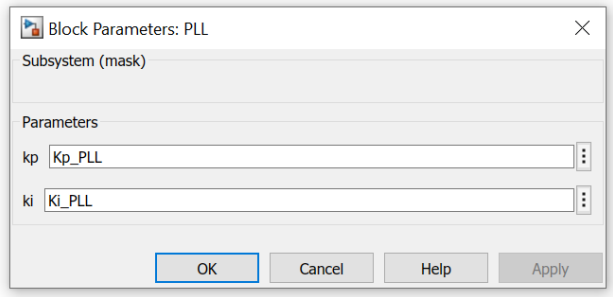
The selected control parameters are then tested in a simulation in the Simulink environmental. Each control parameters are already placed in the correct position in each mask, but first it's necessary to run the MatLab file *grid_connected_inverter_tuning*: at the beginning of the file, all the circuit parameters are defined, then the system transfer functions are computed, such as those regarding the RL filter or the PWM, then the current control loop and the voltage control loop are tuned. In case it may be necessary to apply any changes, such as to the control or circuit parameters, just this file should be modified and run again to ensure that the new selected values are in agreement with everything explained before. Even the inverter current value must be modified just in this file and not directly in the Simulink model since everything is initialized to work correctly according to the values in the Matlab workspace.



(a) Current control mask



(b) DC-link voltage control mask



(c) PLL mask

Figure 22 - Control masks

Then the simulation is started: the simulated time is 0.2 s which is largely enough for the following applications.

No-Load Operation

Firstly, the source current is set equal to zero: in this case no current flows from the inverter to the grid. As shown in *Figure 23*, the line currents have a transient at the beginning, but then they settle on the constant value of 0 A as it should be. The same can be observe from the dq-components of the current in *Figure 24* which settle to zero as well.

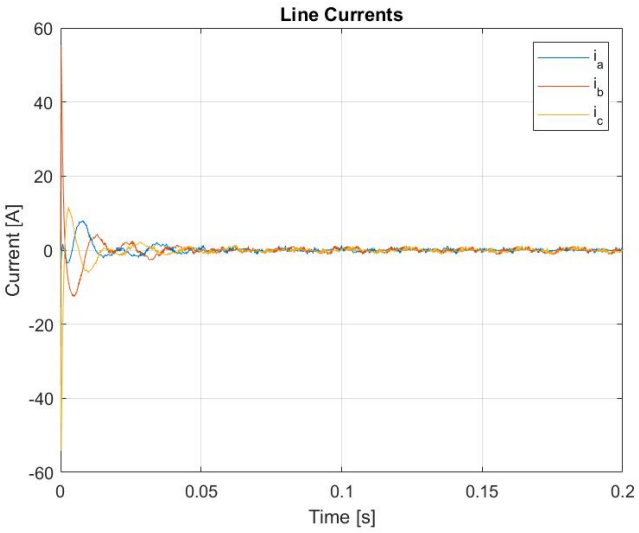


Figure 23 - Line currents in no-load conditions

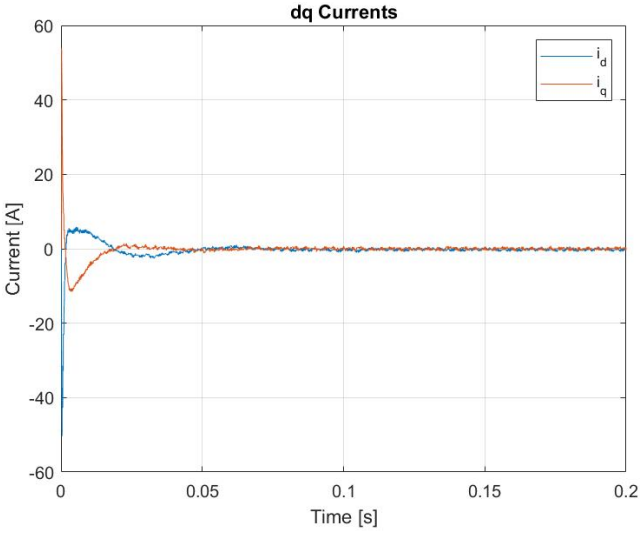


Figure 24 - dq-currents in no-load conditions

Also the DC voltage has a transient in the first instants as it's possible to observe in *Figure 25* but, after about 100 ms, it settles to the nominal value of 690 V. The reached peak is near 695 V which is quite similar to the nominal value, so its dynamic can be assumed acceptable. The time constant is a bit higher than the one forecasted in the MatLab simulation, but this is quite normal since in the Simulink model all the delays that aren't keep into account in the MatLab model are instead considered.

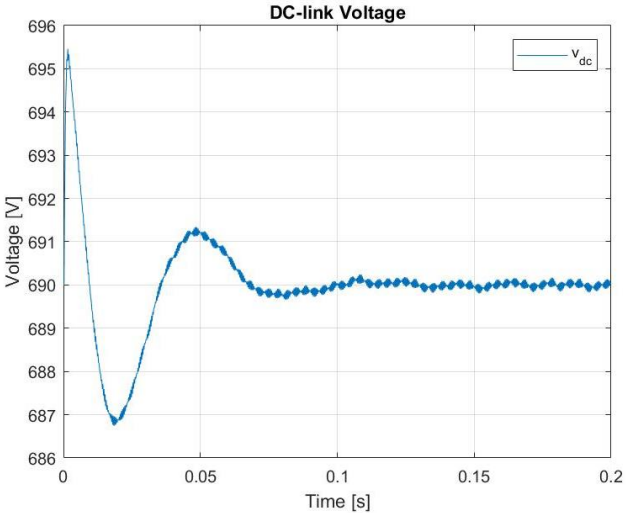


Figure 25 - DC-link voltage in no-load conditions

On the phases, a sinusoidal three-phase voltage is present since it's induced by the grid. As it's possible to highlight from *Figure 27*, the d-voltage has a transient at the beginning, but then it remains constant at steady state, while the q-voltage oscillates with a ripple near the zero.

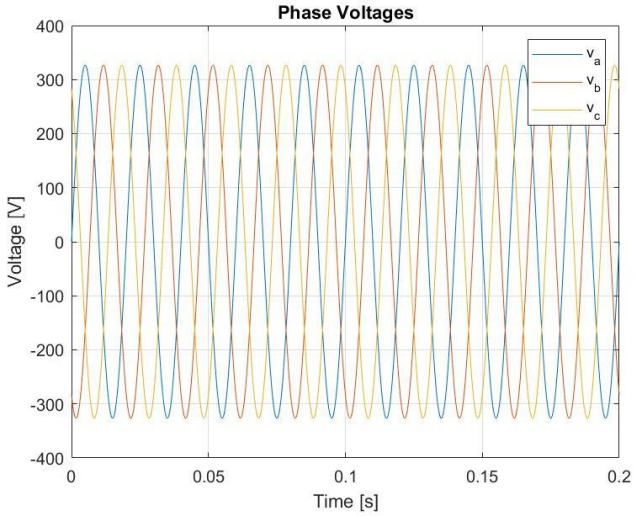


Figure 26 - Phase voltages on no-load conditions

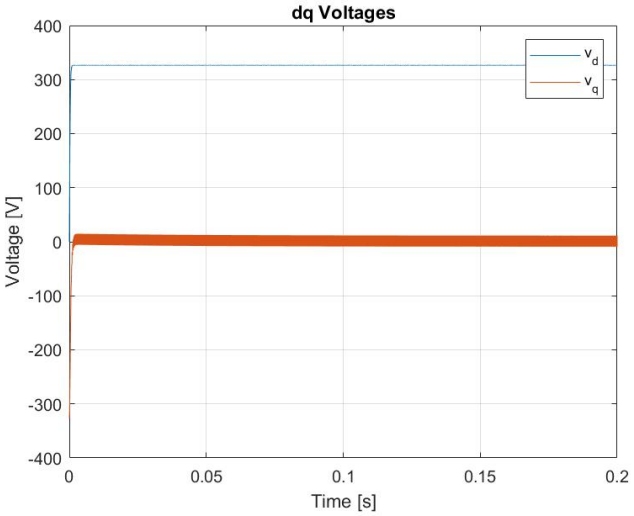


Figure 27 - dq-voltages in no-load conditions

Operation Under Load

Now a current equal to 50 A should be placed on the DC side of the converter. In this case, a current is flown on the grid as shown in *Figure 28*, meaning that the dq-components of the current wouldn't be zero anymore. In fact the d-component of the current settles to a constant value at steady-state, while the q-component reaches the zero, both of them after a transient as it's possible to observe from *Figure 29*. The current reaches its steady-state in about 50 ms.

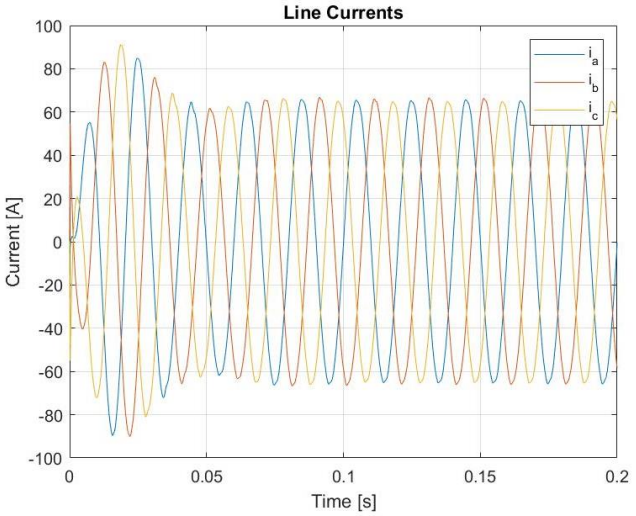


Figure 28 - Line currents on under-load conditions

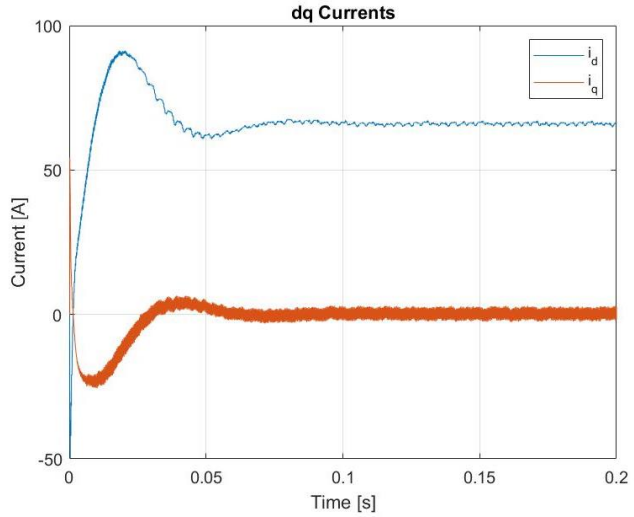


Figure 29 - dq-currents on under-load conditions

Regarding the DC-link voltage represents in *Figure 30*, it presents a behaviour similar to the previous case, but now the overshoot reaches the higher value of 740 V. The steady-state is once again made in 100 ms as in the previous case. Despite the bigger overshoot, it's possible to assume that the dynamic is acceptable in this case as well.

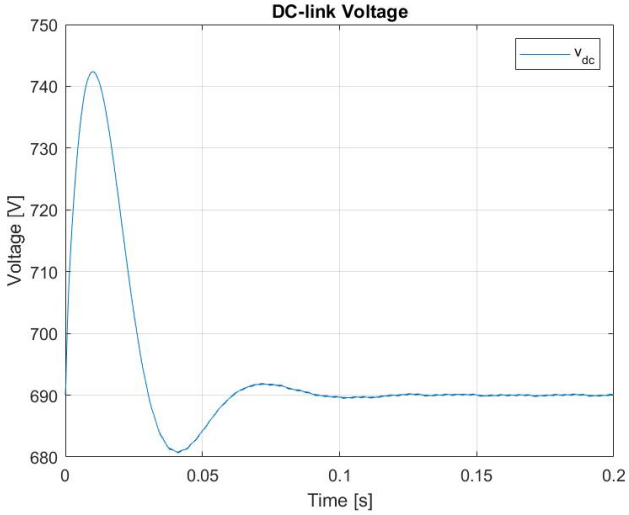


Figure 30 - DC-link voltage on under-load conditions

Once again, the phase voltage is sinusoidal at 50 Hz with an phase-to-phase RMS amplitude of 400 V and the dq-components of the voltage behave as in the previous case.

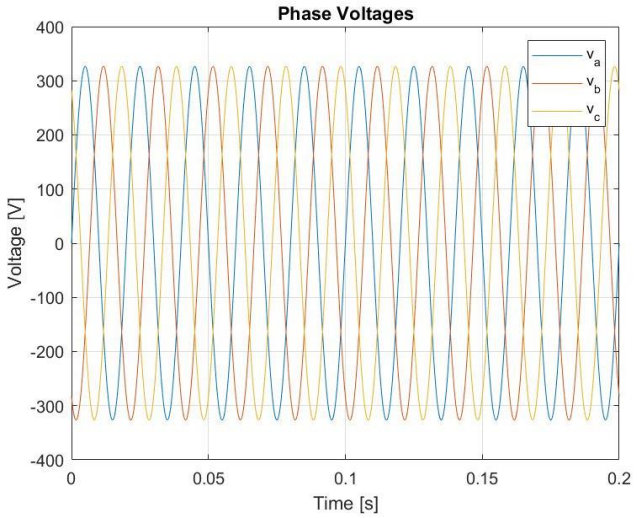


Figure 31 - Phase voltages on under-load conditions

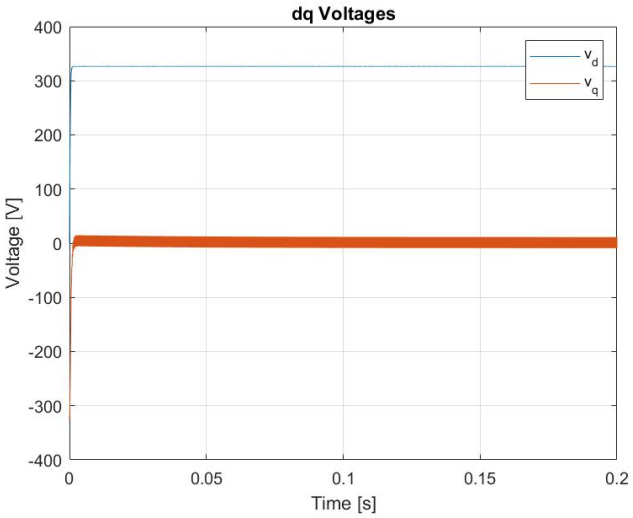


Figure 32 - dq-voltages on under-load conditions

Step Response

In the end, a step reference is applied to the source current in order to investigate how the system behaves in presence of a sudden change in the generation. The current is changed from zero to 50 A at time $t_{step} = 0.1$ s as shown in *Figure 33* in order to let the system arrive at steady-state before imposing the current change.

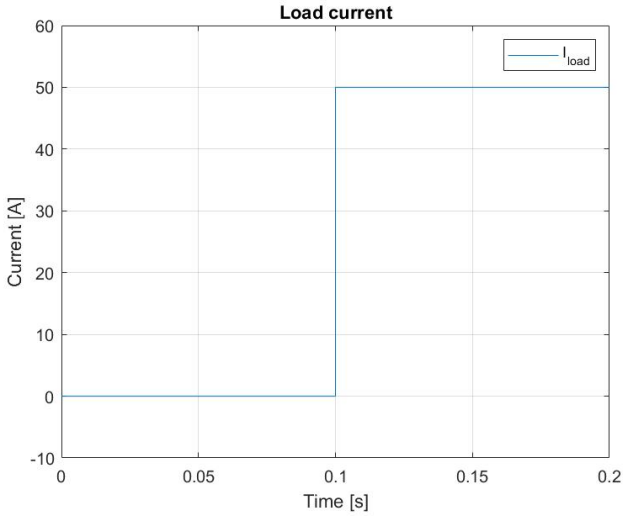


Figure 33 - Step current

Since at beginning the source current is zero, the system behaves as in the case with a generated current equal to zero, so there is a transient and then the variables assest to their steady-state values. At time 0.1 s, the step is applied: both the DC-link voltage and the line currents suddenly change and then reach the steady-state in 100 ms as well.

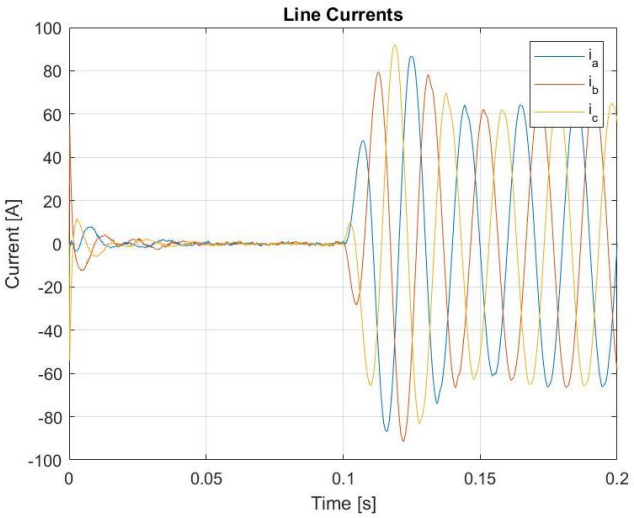


Figure 34 – Line currents with a step current

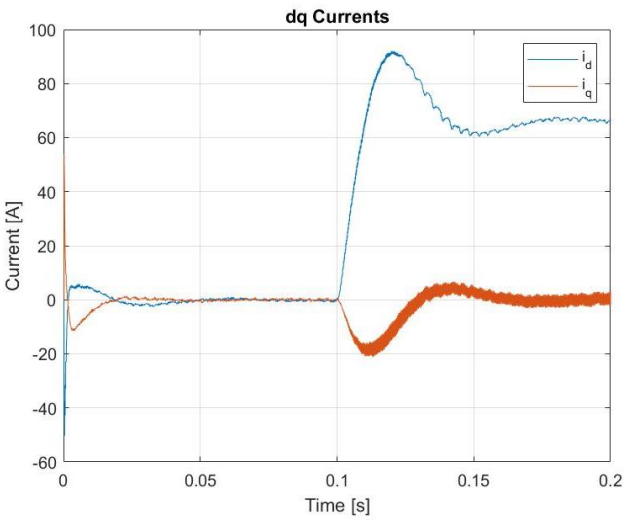


Figure 35 - dq-currents with a step current

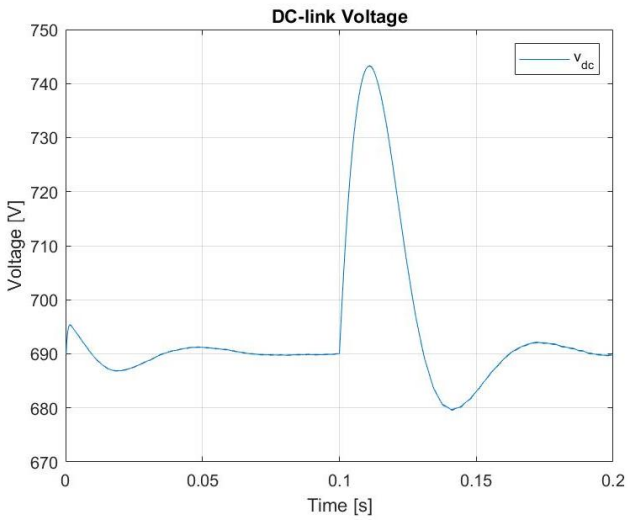


Figure 36 - DC-link voltage with a step current

Regarding the phase voltages, they aren't influenced by the source current as already observed in the previous cases since the voltage is imposed by the grid. This means that the voltage is still a symmetric three-phase system and the dq-voltage components remain constant at steady-state without undergoing changes due to the current change.

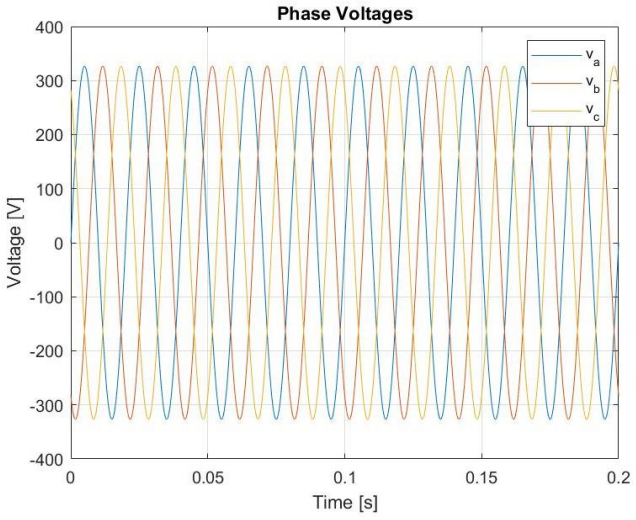


Figure 37 - Phase voltages with a step current

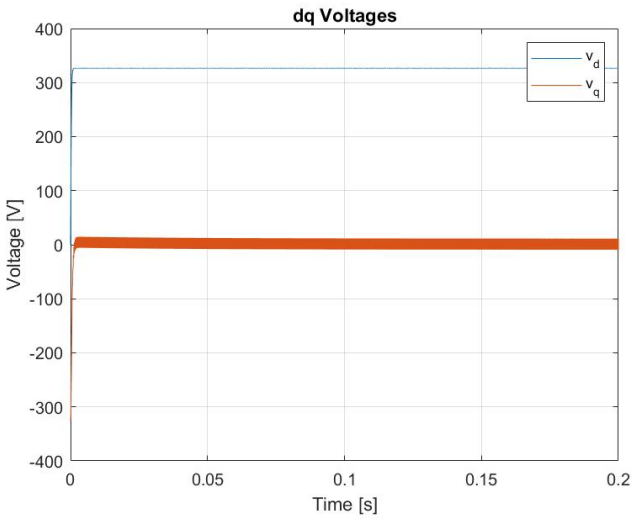


Figure 38 – dq-voltages with a step current

Unbalanced Systems

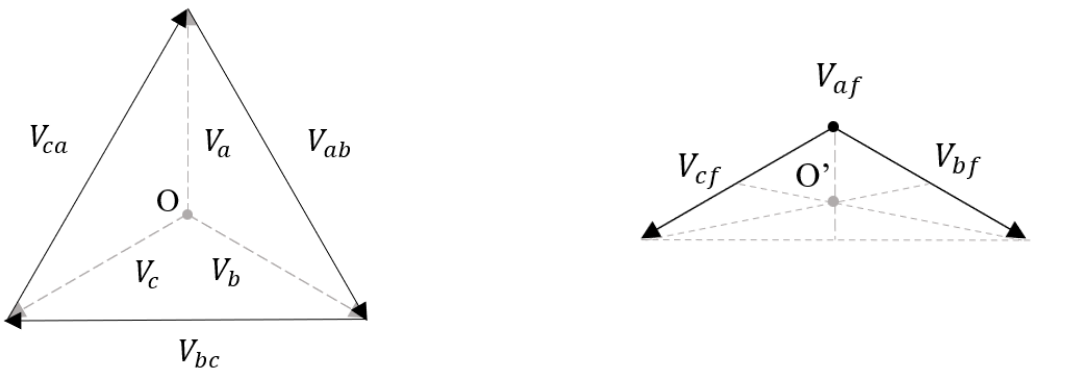
Usually it's possible to say that the real grid voltage behaves like a symmetrical three-phase source, but sometimes, for example during a fault, this approximation can't be considered true anymore. In these cases, also the control system should be implemented differently in such a way that the dq-components of voltages and currents remain constant at steady-state for a better performance of the controllers.

In the following sections, a Single Line to Ground (SLG) fault is assumed for phase *a*, starting from a no-load condition, but the same analysis can be implemented for any type of unsymmetrical fault. For the sake of simplicity, just the modelling of the converter in the faulted condition is explained, while the controlling isn't implemented.

Voltage Computation

As it's known, when a fault occurs in the network, the grid voltage is subjected to a transient: assuming that the network reaches the steady-state, it's possible to compute the grid voltage and the line currents in the fault condition.

The faulted phase voltage is set equal to zero and, since the system is assumed to be isolated from the ground, the other two phases suffer from an overvoltage because the theoretical centre of the voltage triangle is shifted by the homopolar voltage from O to O', due to the fact that the faulted phase voltage imploded in one point as shown in *Figure 39*.



(a) Three-phase voltages in unfaulted conditions (b) Three-phase voltages in SLG-faulted conditions

Figure 39 - Voltage triangle in unfaulted and faulted conditions

For these reasons, the phase voltages in the faulted condition can be assumed as shown in (21) and (22).

$$\begin{aligned} V_a &= 0 \\ V_b &= 400\sqrt{3} \\ V_c &= 400\sqrt{3} \end{aligned} \tag{21}$$

$$\begin{aligned} \phi_a &= 0 \\ \phi_b &= -\frac{5}{6}\pi \\ \phi_c &= \frac{5}{6}\pi \end{aligned} \tag{22}$$

SOGI-based PLL And PNSC

Since the system is asymmetric, the dq-components of the voltage and the current should be computed differently from the previous case.

Firstly, the phase variables are transformed into their $\alpha\beta$-components with a Clarke's Transformation as before. Then a Second Order Generalized Integrator (SOGI) is applied to compute two pairs of variables in quadrature (shifted of $\pi/2$ between each other), one for the α-component and one for the β-component. In this particular simulation, a rise time t_s equal to 0.1 s is assumed for the SOGI and its implementation for the α-voltage component is shown below in *Figure 40*.

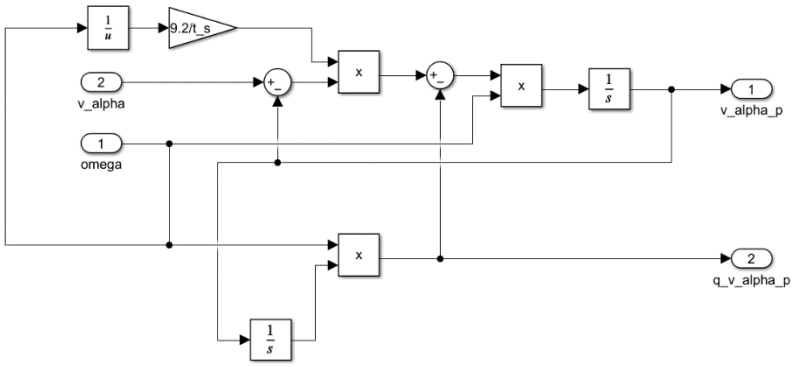


Figure 40 - Example of SOGI for the alpha-voltage component

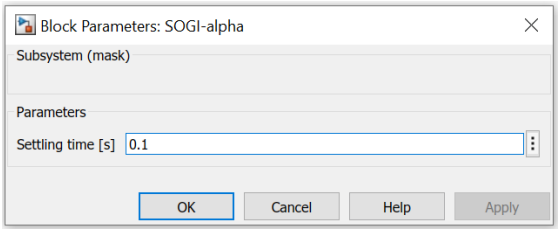


Figure 41 - SOGI mask with the selection of settling time parameter

In the end, these variables are decoupled in the PNSC shown in *Figure 42* to obtain two pairs of $\alpha\beta$-components, one for the positive sequence and one for the negative sequence.

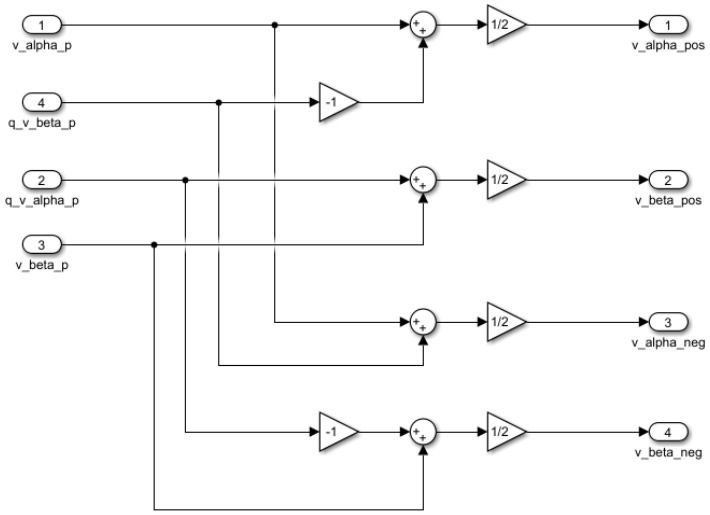


Figure 42 - PNSC

Then the dq-transformation is applied to the components of both sequence in order to compute two pairs of dq-component, one for the positive sequence and one for the negative sequence: the PLL is used again to determine the angle reference for the transformation, which is synchronized with the grid voltage, and it's calculated starting from the q-voltage component of the positive sequence, while the angle reference for the dq-transformation of the negative sequence is assumed equal to $-\theta_{pos}$. Also in this case the zero component is assumed equal to zero for the sake of simplicity and this process is applied to both voltages and currents.

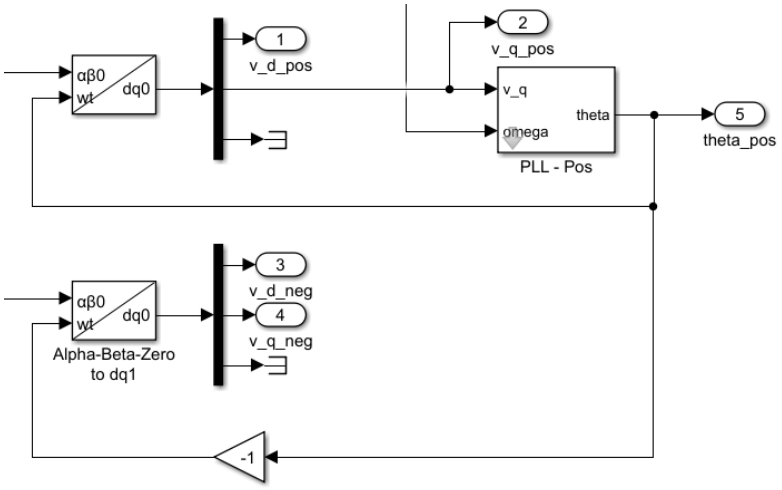
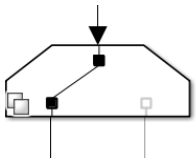


Figure 43 - PLL and computation of the positive and negative sequence dq-components of the voltage

Simulation Results

In order to simulate the presented scenario, it's necessary to apply one change in the model since it works for both balanced and unbalanced system. According to the situation that is studied, the phase variables are given as input to a different block, while the other one is neglected. As default, the block which refers to the balanced systems control is simulated.

First of all, the condition *fault==1* must be written in the switches, as shown in *Figure 44*, in order to define the condition that triggers the switching in the control system. It's important to write it every time the model is opened from scratch since it won't remain saved after the closure of the model.



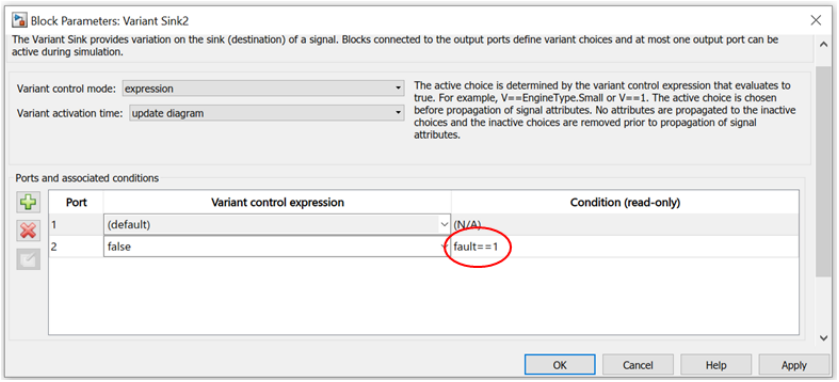


Figure 44 - Implementation of the switching condition

Then the fault is implemented also in the MatLab file *grid_connected_inverter_tuning*: by default, the variable fault is set to zero, so it's necessary to change it from 0 to 1 in order to apply the faulted conditions explained before. If another type of fault is wanted to be studied, the new faulted conditions should be written in the *if* structure instead of the ones present now which refers to a SLG fault. Since just the initial data have changed, it's possible to avoid running the whole file, but just running the first section by clicking on the bottom *Run and Advance* in the control bar.

```
20 -   fault=1;
21
22 -   if fault == 1
23 -       V_a=0;
24 -       V_b=sqrt(3)*400;
25 -       V_c=sqrt(3)*400;
26 -       phi_a=0;
27 -       phi_b=-5/6*pi;
28 -       phi_c=5/6*pi;
29 -   else
30 -       V_a=400;
31 -       V_b=400;
32 -       V_c=400;
33 -       phi_a=0;
34 -       phi_b=-2/3*pi;
35 -       phi_c=-4/3*pi;
36 -   end
```

Figure 45 - Faulted conditions in the MatLab file

Then the Simulink model is run again. The phase voltages are those shown in *Figure 46*: phase *a* is faulted, while the other two suffer from an overvoltage as explained in the previous section.

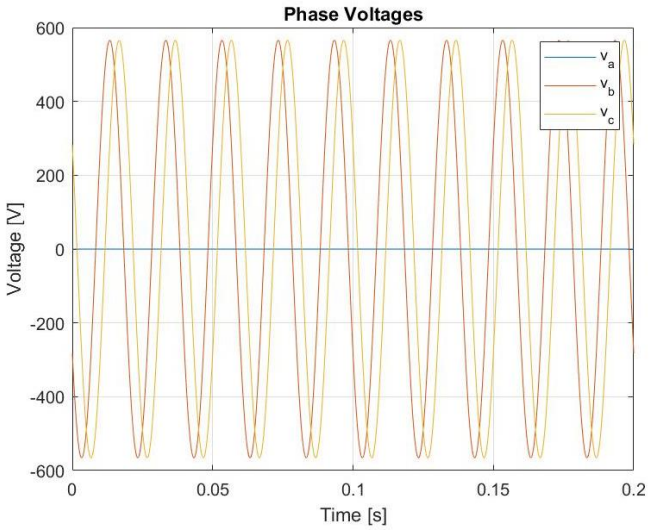


Figure 46 - Phase voltages in faulted conditions

The dq-voltage components of the positive and negative sequence are those shown below in *Figure 47* and *Figure 48*: as it's possible to observe, the system reaches the steady-state after a transient, so if the control system would have been implemented, the control signal would have been constant. Just the d-component of the positive sequence is non null at steady-state, while all the others reach the zero.

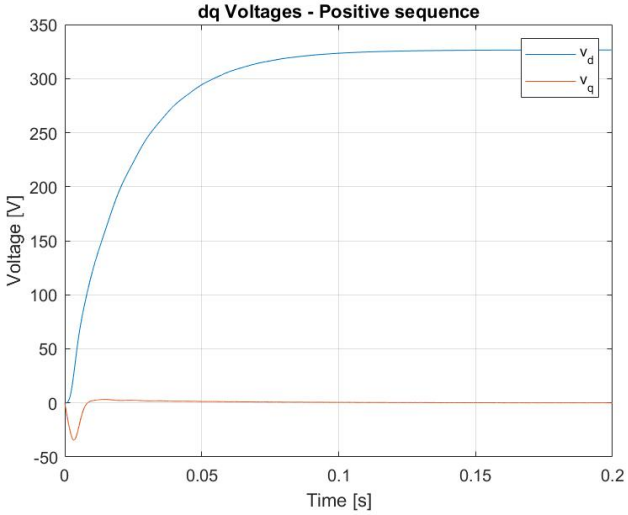


Figure 47 - dq-voltage components in faulted conditions for the positive sequence

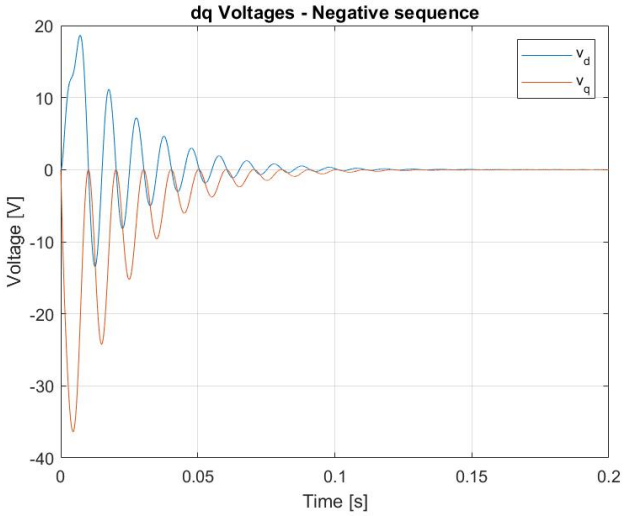


Figure 48 - dq-voltage components in faulted conditions for the negative sequence

Regarding the current components, those are shown below in *Figure 49* and *Figure 50*: even if the system is at no-load, so there shouldn't be any current flowing from the inverter to the grid, the grid voltage induces a line current anyway since the system isn't controlled. As for the voltage components, also the current components reach the steady-state after a transient, with the negative sequence components equal to zero at steady-state.

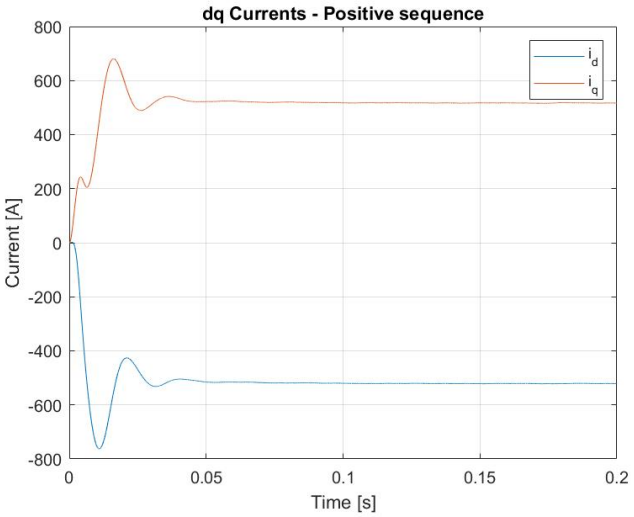


Figure 49 - dq-current components in faulted conditions for the positive sequence

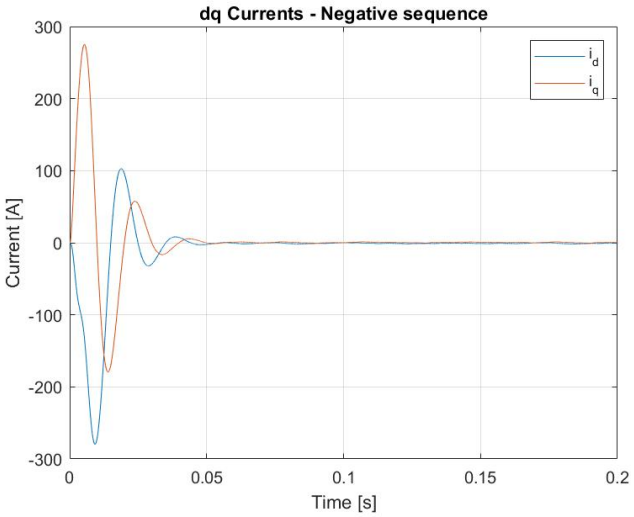


Figure 50 - dq-current components in faulted conditions for the negative sequence

When a source current equal to 50 A is imposed, the dq-currents behaviour shown in *Figure 51* and *Figure 52* is similar to the one in no-load conditions, but they reach higher peak values and the positive sequence components settle to higher values at steady-state since the system isn't controlled as explained before.

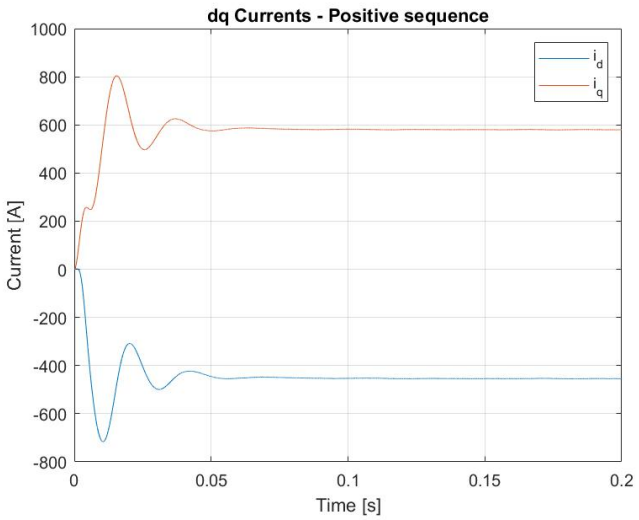


Figure 51 - dq-current components in faulted conditions for the positive sequence with a source current

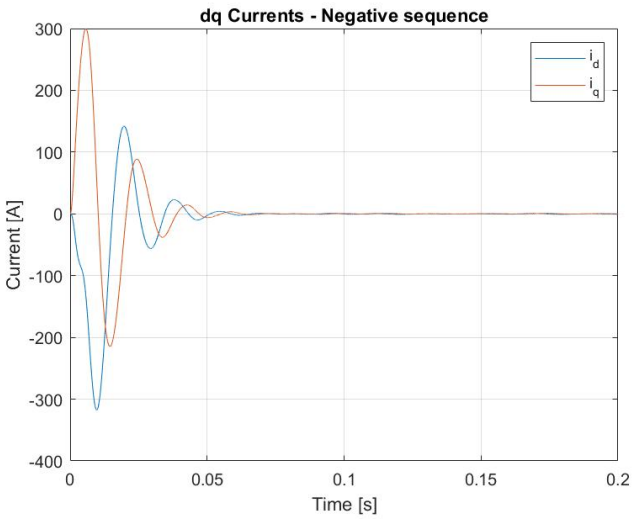


Figure 52 - dq-current components in faulted conditions for the negative sequence with a source current

Conclusions

As previously stated, the control system parameters selected during the open-loop and closed-loop analysis of the current and DC-link voltage control transfer functions for balanced systems represent suitable values for the control system of the converter since they guarantee good performances as confirmed in the Simulink simulation.

It’s important to take into account that the results obtained in the MatLab and Simulink simulations, such as those regarding the system time-constant, slightly diverge. The main reason is that the tuning MatLab model is just an ideal approximation of the Simulink model which is an estimation of a real grid-connected converter as well since not all circuit effects have been considered, for example those regarding the transformer leakage impedance. Despite that, they are in agreement with each other and they can be considered a good approximation of the real system, also on the safe-side.

Regarding the modelling of unbalanced systems, the implemented approach provided good results in terms of stability of the controlled signal, but it would be necessary to also carry out the control system circuit and its tuning in order to deeply evaluate the performance of the whole system in those conditions.