Design Space Exploration for a MaxJ PRF

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1. Introduction

This technical report contains the latest status of the synthesis presented in our submission to the SAMOS 2017 conference. The results showed are relative to a Maxeler implementation of the Polymorphic Register File (PRF) that we published in a github repository with an open source license[1].

PRF

A PRF is a parameterizable register file, which can be logically reorganized by the programmer or a runtime system to support multiple register dimensions and sizes simultaneously. We promote the use of this architecture as a parallel scratchpad memory to store data structures that need high-speed access.

The configuration of a PRF consists of a storage capacity **C** (e.g., 512KB) distributed to *p***q* memory modules and a mapping function. The number of memory modules implied define the number of elements that can be accessed in parallel – p*q elements –which we will also refer to as *number of lanes*. The mapping function specifies a subset of six PRF access patterns that will be accessible in parallel. Table 1 shows the PRF Mapping schemes and the available parallel access pattern that each of them guarantees – to know the constrains of the PRF the reader can refer to [1].

Mapping Scheme	Available patterns
ReO	Rectangle
ReRo	Rectangle, Row, Main Diagonal, Secondary Diagonal
ReCo	Rectangle, Column, Main Diagonal, Secondary Diagonal
RoCo	Row, Column, Rectangle.
ReTr	Rectangle, Transposed Rectangle.

Table 1 PRF Mapping Schemes

Implementation

We have implemented the PRF using the MaxJ high level synthesis language. Figure 1 shows a block diagram that describes our implementation. We adopted a bottom up development process, and designed all the modules presented below as separate kernels. Each module was tested separately for correctness. The first implementation – which we refer to in this document as *split* – was realized linking through

[1] https://github.com/giuliostramondo/prf_maxeler_samos

the Maxeler kernel the modules in a PRF complete design. In our second implementation – referred to as *fused* - we merged the first design into a single kernel, hoping to reduce the logic overhead that could incur when using multiple separate kernels in the same design. Section 2 provides the result we obtained for these implementations.

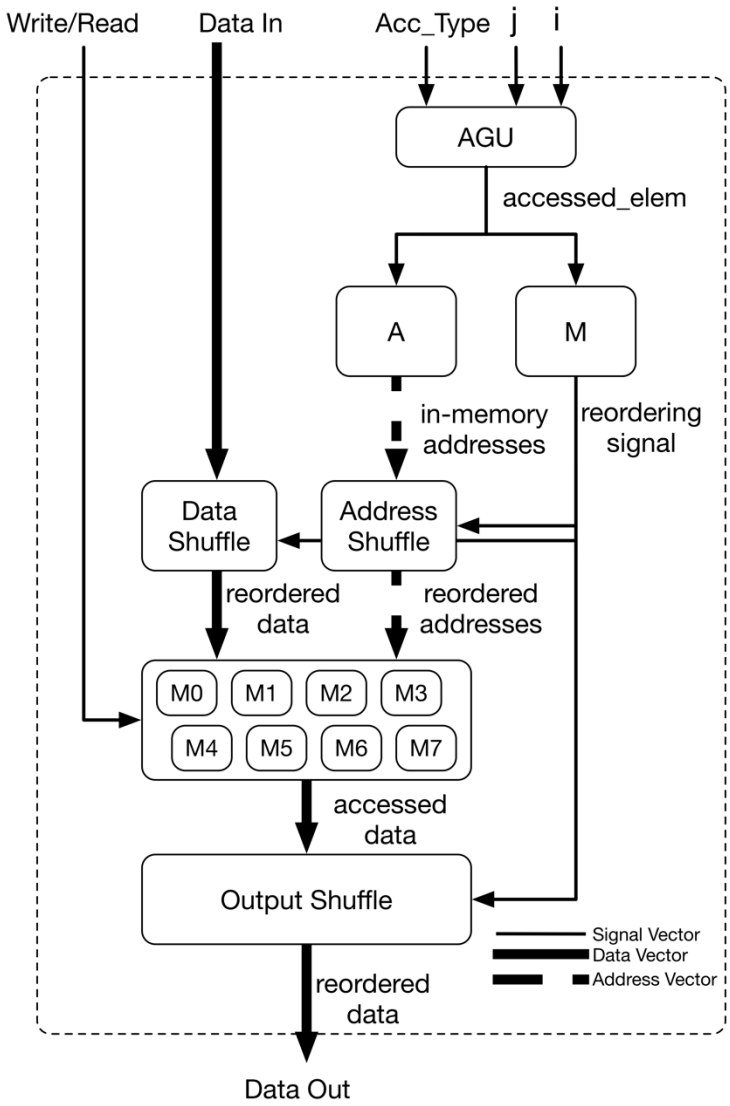


Figure 1 PRF Block Diagram

In Figure 1, the input signals are: *Write/Read, AccType, i, j*, and are all scalars. The thick arrows represent the data buses. They are $p \times q$ elements wide, with each element containing *dataSize* bits i.e., 32 bits or 64 bits. The dotted thick arrows are address buses. Each address bus contains $p \times q$ addresses; the size of each address depends on the total capacity (C) of the PRF and on the number of memory banks used: those define the number of addressable elements in each PRF memory module. The remaining buses output of **AGU**, **M** and **A** are all $p \times q$ elements wide. When performing a write access, the input data - *DataIn* - is written in the memory locations identified by **A** and **M**, after they have been

reordered by the **Write Data Shuffle**; the values that are being overwritten are sent to the **Read Data Shuffle**. During a read access the *DataIn* elements are ignored, and the contents of the selected memory location is read and sent to the Read Data Shuffle.

This design relies on two stages of reordering to allow the correct mapping of the data in the memory modules - (e.g., M0-M7 in the example in Figure 1) – and a transparent output to the user. The first reordering stage is performed by the **Write Data Shuffle** and **Address Shuffle** blocks; it enables, during read accesses, the mapping of the input data - *Data In* – to the correct memory location defined by the currently employed Mapping Scheme, during write accesses, the selection of the correct memory location containing the requested elements. The second reordering stage is performed by the **Read Data Shuffle** reorders its inputs to their original position, performing the inverse reordering with respect to the one done in the first stage.

We achieved this dual reordering in two ways, which resulted in two different implementation of the blocks in the diagram showed in Figure 1. We refer to those two implementation as *InvMath* and *InvShuffle.*

In the *InvMath* design, the mathematical function M computes two sets of reordering signals: the regular ones and their mathematical inverse. The reordering signals writing data to the PRF are the inverse of the ones used for reading data from the PRF. The regular, non-inverted output of M is sent to the Read Data Shuffle and the Address Shuffle, while the mathematically inverse reordering signal is sent to the Write Shuffle. In this design, all the Shuffles are identical, as only the reordering command signals are different.

The *InvShuffle* design is implemented using a dual pair of Shuffles. Given a reordering signal, applying one Shuffle reorders the elements, while the Inverse Shuffle, with the same reordering signal, restores the initial order. In this de- sign, therefore, the Read Data Shuffle and Address Shuffle are implemented using a regular Shuffle, while the Data Write Shuffle is implemented using an Inverse Shuffle. In this case, M produces three identical reordering signals and implements only the regular mapping function described in [1].

For a more comprehensive description of the blocks showed in Figure 1 the reader can refer to our submission to the SAMOS 2017 Conference.

2. Raw Data

We selected a number of relevant parameters for the Design Space Exploration which are showed in Table 2. The rest of this section shows table containing the raw data we obtained from our synthesis which we will keep updated daily.

DSE Parameter	Explanation and Affected Blocks
The PRF capacity (C), in KB	Depth of each FMem instantiated in the Memory Banks.
Number of lanes = p x q	Number of read/write operation that can occur in parallel. *Affects each block of the design.*
Clock Frequency (in MHz).	*Affects the clock period and latency (in nanoseconds) of the PRF and, consequently, the attainable bandwidth.*
PRF latency (in clock cycles)	The latency of reading and writing data in the PRF, in clock cycles. *Affects the Design Clock Frequency and the PRF access time.*
Data-Width of each BRAM	The bandwidth of the input and output data. *Affects the aggregated PRF bandwidth*
Type of Write Crossbar (inverse crossbar module –InvShuffle- vs. a mathematically inverted M function - InvMath)	Mapping data to memories and reordering output data are implemented in a reorder stage. For writing values into the PRF, the rearrangement is done either with an inverse crossbar and the regular M function, or using a regular crossbar and the mathematically inverted M function. *Affects the M blocks and the Crossbar blocks.*

Table 2 DSE Paramet

Synthesis results for Inverse Shuffle, 64 bits, fused design

Frequency [MHz]	Capacity [KB]	Lanes	Scheme	Logic Utilization %	LUTs Utilization %	Primary FFs Utilization %	Secondary FFs Utilization %	Multipliers25x18 Utilization %	DSP blocks Utilization %	BRAM Utilization %	Bandwidth (GB/s)	Bits	Inverse	Fused
100	512	8	ReO	0,0862	0,0606	0,0721	0,0225	0	0	0,1551	5,960464478	64	S	Y
100	512	8	ReRo	0,0882	0,0597	0,0736	0,0213	0	0	0,1551	5,960464478	64	S	Y
100	512	8	ReCo	0,0896	0,0583	0,075	0,0198	0	0	0,1551	5,960464478	64	S	Y
100	512	8	RoCo	0,081	0,0646	0,0672	0,0277	0	0	0,1551	5,960464478	64	S	Y
100	512	8	ReTr	0,0871	0,0607	0,0726	0,0223	0	0	0,1551	5,960464478	64	S	Y
100	512	16	ReO	0,177	0,1387	0,1483	0,0758	0	0	0,187	11,92092896	64	S	Y
100	512	16	ReRo	0,1768	0,139	0,1483	0,0761	0	0	0,187	11,92092896	64	S	Y
100	512	16	ReCo	0,1766	0,139	0,1484	0,076	0	0	0,187	11,92092896	64	S	Y
100	512	16	RoCo	0,1747	0,1408	0,1463	0,0782	0	0	0,187	11,92092896	64	S	Y
100	512	16	ReTr	0,1742	0,1413	0,1461	0,0788	0	0	0,187	11,92092896	64	S	Y
100	512	32	ReO	0	0	0	0	0	0	0	0	64	S	Y
100	512	32	ReRo	0	0	0	0	0	0	0	0	64	S	Y
100	512	32	ReCo	0	0	0	0	0	0	0	0	64	S	Y
100	512	32	RoCo	0	0	0	0	0	0	0	0	64	S	Y
100	512	32	ReTr	0	0	0	0	0	0	0	0	64	S	Y
100	1024	8	ReO	0,0923	0,0679	0,077	0,0248	0,004	0,004	0,2603	5,960464478	64	S	Y
100	1024	8	ReRo	0,0948	0,0665	0,0794	0,023	0,004	0,004	0,2603	5,960464478	64	S	Y
100	1024	8	ReCo	0,0905	0,0697	0,0756	0,0268	0,004	0,004	0,2603	5,960464478	64	S	Y
100	1024	8	RoCo	0,0835	0,0723	0,0711	0,0315	0,004	0,004	0,2603	5,960464478	64	S	Y
100	1024	8	ReTr	0,0932	0,0679	0,0777	0,0244	0,004	0,004	0,2603	5,960464478	64	S	Y
100	1024	16	ReO	0,1838	0,1562	0,1551	0,084	0,0079	0,0079	0,2923	11,92092896	64	S	Y
100	1024	16	ReRo	0,1895	0,1541	0,1601	0,0801	0,0079	0,0079	0,2923	11,92092896	64	S	Y

100	1024	16	ReCo	0,189	0,1553	0,1593	0,0811	0,0079	0,0079	0,2923	11,92092896	64	S	Y
100	1024	16	RoCo	0,1899	0,1549	0,1597	0,0809	0,0079	0,0079	0,2923	11,92092896	64	S	Y
100	1024	16	ReTr	0,1892	0,1548	0,1592	0,0807	0,0079	0,0079	0,2923	11,92092896	64	S	Y
100	1024	32	ReO	0	0	0	0	0	0	0	0	64	S	Y
100	1024	32	ReRo	0	0	0	0	0	0	0	0	64	S	Y
100	1024	32	ReCo	0	0	0	0	0	0	0	0	64	S	Y
100	1024	32	RoCo	0	0	0	0	0	0	0	0	64	S	Y
100	1024	32	ReTr	0	0	0	0	0	0	0	0	64	S	Y
100	2048	8	ReO	0,0931	0,0619	0,0758	0,0204	0	0	0,4746	5,960464478	64	S	Y
100	2048	8	ReRo	0,0926	0,0628	0,0752	0,0213	0	0	0,4746	5,960464478	64	S	Y
100	2048	8	ReCo	0,0925	0,0627	0,0754	0,0211	0	0	0,4746	5,960464478	64	S	Y
100	2048	8	RoCo	0,0928	0,0626	0,0756	0,0209	0	0	0,4746	5,960464478	64	S	Y
100	2048	8	ReTr	0,0926	0,0628	0,0754	0,0212	0	0	0,4746	5,960464478	64	S	Y
100	2048	16	ReO	0,1848	0,1425	0,1533	0,0749	0	0	0,5028	11,92092896	64	S	Y
100	2048	16	ReRo	0,1841	0,1437	0,1525	0,0762	0	0	0,5028	11,92092896	64	S	Y
100	2048	16	ReCo	0,1799	0,1462	0,1489	0,0796	0	0	0,5028	11,92092896	64	S	Y
100	2048	16	RoCo	0,1831	0,1447	0,1514	0,0773	0	0	0,5028	11,92092896	64	S	Y
100	2048	16	ReTr	0,1836	0,1449	0,1517	0,0774	0	0	0,5028	11,92092896	64	S	Y
100	2048	32	ReO	0	0	0	0	0	0	0	0	64	S	Y
100	2048	32	ReRo	0	0	0	0	0	0	0	0	64	S	Y
100	2048	32	ReCo	0	0	0	0	0	0	0	0	64	S	Y
100	2048	32	RoCo	0	0	0	0	0	0	0	0	64	S	Y
100	2048	32	ReTr	0	0	0	0	0	0	0	0	64	S	Y
100	4096	8	ReO	0,0996	0,0727	0,0787	0,0238	0,004	0,004	0,9032	5,960464478	64	S	Y
100	4096	8	ReRo	0,105	0,0687	0,0837	0,0193	0,004	0,004	0,9032	5,960464478	64	S	Y
100	4096	8	ReCo	0,1026	0,0706	0,0817	0,0214	0,004	0,004	0,9032	5,960464478	64	S	Y
100	4096	8	RoCo	0,0957	0,0754	0,0756	0,0275	0,004	0,004	0,9032	5,960464478	64	S	Y

100	4096	8	ReTr	0,1014	0,0716	0,0804	0,0223	0,004	0,004	0,9032	5,960464478	64	S	Y
100	4096	16	ReO	0,1967	0,1597	0,1612	0,08	0,0079	0,0079	0,9314	11,92092896	64	S	Y
100	4096	16	ReRo	0,1991	0,1592	0,1634	0,079	0,0079	0,0079	0,9314	11,92092896	64	S	Y
100	4096	16	ReCo	0,1994	0,1592	0,1637	0,0788	0,0079	0,0079	0,9314	11,92092896	64	S	Y
100	4096	16	RoCo	0,2041	0,1563	0,1678	0,0749	0,0079	0,0079	0,9314	11,92092896	64	S	Y
100	4096	16	ReTr	0,2026	0,1569	0,1664	0,0756	0,0079	0,0079	0,9314	11,92092896	64	S	Y
100	4096	32	ReO	0	0	0	0	0	0	0	0	64	S	Y
100	4096	32	ReRo	0	0	0	0	0	0	0	0	64	S	Y
100	4096	32	ReCo	0	0	0	0	0	0	0	0	64	S	Y
100	4096	32	RoCo	0	0	0	0	0	0	0	0	64	S	Y
100	4096	32	ReTr	0	0	0	0	0	0	0	0	64	S	Y

Table 3 Raw Synthesis results for Inverse Shuffle, 64 bits, fused design

Synthesis results for Inverse Math, 64 bits, fused design

Frequency [MHz]	Capacity [KB]	Lanes	Scheme	Logic Utilization %	LUTs Utilization %	Primary FFs Utilization %	Secondary FFs Utilization %	Multipliers25x18 Utilization %	DSP blocks Utilization %	BRAM Utilization %	Bandwidth (GB/s)	Bits	Inverse	Fused
100	512	8	ReO	0,0803	0,054	0,0704	0,0196	0	0	0,1551	5,960464478	64	M	Y
100	512	8	ReRo	0,0864	0,0562	0,0748	0,0187	0	0	0,1551	5,960464478	64	M	Y
100	512	8	ReCo	0,0828	0,0619	0,0713	0,0243	0	0	0,1551	5,960464478	64	M	Y
100	512	8	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	512	8	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	512	16	ReO	0,1452	0,1151	0,1349	0,0786	0	0	0,187	11,92092896	64	M	Y
100	512	16	ReRo	0,1569	0,1185	0,1436	0,0766	0	0	0,187	11,92092896	64	M	Y
100	512	16	ReCo	0,1625	0,1227	0,148	0,0777	0	0	0,187	11,92092896	64	M	Y
100	512	16	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	512	16	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	512	32	ReO	0	0	0	0	0	0	0	0	64	M	Y
100	512	32	ReRo	0	0	0	0	0	0	0	0	64	M	Y
100	512	32	ReCo	0	0	0	0	0	0	0	0	64	M	Y
100	512	32	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	512	32	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	1024	8	ReO	0,0895	0,059	0,0786	0,0186	0,004	0,004	0,2603	5,960464478	64	M	Y
100	1024	8	ReRo	0,095	0,0621	0,0826	0,0188	0,004	0,004	0,2603	5,960464478	64	M	Y
100	1024	8	ReCo	0,0969	0,0632	0,0839	0,019	0,004	0,004	0,2603	5,960464478	64	M	Y
100	1024	8	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	1024	8	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	1024	16	ReO	0,1596	0,1292	0,1484	0,08	0,0079	0,0079	0,2923	11,92092896	64	M	Y
100	1024	16	ReRo	0,1675	0,1359	0,1537	0,0825	0,0079	0,0079	0,2923	11,92092896	64	M	Y

100	1024	16	ReCo	0,1698	0,1412	0,1551	0,086	0,0079	0,0079	0,2923	11,92092896	64	M	Y
100	1024	16	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	1024	16	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	1024	32	ReO	0,4227	0,3573	0,4093	0,272	0,0159	0,0159	0,3562	23,84185791	64	M	Y
100	1024	32	ReRo	0	0	0	0	0	0	0	0	64	M	Y
100	1024	32	ReCo	0	0	0	0	0	0	0	0	64	M	Y
100	1024	32	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	1024	32	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	2048	8	ReO	0,0865	0,0559	0,0737	0,0179	0	0	0,4746	5,960464478	64	M	Y
100	2048	8	ReRo	0,0919	0,0585	0,0775	0,0177	0	0	0,4746	5,960464478	64	M	Y
100	2048	8	ReCo	0,0934	0,0611	0,0784	0,019	0	0	0,4746	5,960464478	64	M	Y
100	2048	8	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	2048	8	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	2048	16	ReO	0,1544	0,1185	0,1405	0,077	0	0	0,5028	11,92092896	64	M	Y
100	2048	16	ReRo	0,1646	0,1235	0,1477	0,0765	0	0	0,5028	11,92092896	64	M	Y
100	2048	16	ReCo	0,1693	0,1281	0,1516	0,0781	0	0	0,5028	11,92092896	64	M	Y
100	2048	16	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	2048	16	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	2048	32	ReO	0	0	0	0	0	0	0	0	64	M	Y
100	2048	32	ReRo	0	0	0	0	0	0	0	0	64	M	Y
100	2048	32	ReCo	0	0	0	0	0	0	0	0	64	M	Y
100	2048	32	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	2048	32	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	4096	8	ReO	0,0959	0,0644	0,0795	0,0182	0,004	0,004	0,9032	5,960464478	64	M	Y
100	4096	8	ReRo	0,0963	0,0709	0,079	0,023	0,004	0,004	0,9032	5,960464478	64	M	Y
100	4096	8	ReCo	0,1014	0,0699	0,083	0,0205	0,004	0,004	0,9032	5,960464478	64	M	Y
100	4096	8	RoCo	0	0	0	0	0	0	0	0	64	M	Y

100	4096	8	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	4096	16	ReO	0,1719	0,132	0,1543	0,0761	0,0079	0,0079	0,9314	11,92092896	64	M	Y
100	4096	16	ReRo	0,1808	0,1386	0,1601	0,078	0,0079	0,0079	0,9314	11,92092896	64	M	Y
100	4096	16	ReCo	0,1832	0,1437	0,1625	0,0806	0,0079	0,0079	0,9314	11,92092896	64	M	Y
100	4096	16	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	4096	16	ReTr	0	0	0	0	0	0	0	0	64	M	Y
100	4096	32	ReO	0	0	0	0	0	0	0	0	64	M	Y
100	4096	32	ReRo	0	0	0	0	0	0	0	0	64	M	Y
100	4096	32	ReCo	0	0	0	0	0	0	0	0	64	M	Y
100	4096	32	RoCo	0	0	0	0	0	0	0	0	64	M	Y
100	4096	32	ReTr	0	0	0	0	0	0	0	0	64	M	Y

Table 4 Inverse Math, 64 bits, fused design

Synthesis results for Inverse Shuffle, 32 bits, fused design.

Frequency [MHz]	Capacity [KB]	Lanes	Scheme	Logic Utilization %	LUTs Utilization %	Primary FFs Utilization %	Secondary FFs Utilization %	Multipliers25x18 Utilization %	DSP blocks Utilization %	BRAM Utilization %	Bandwidth (GB/s)	Bits	Inverse	Fused
100	512	8	ReO	0,0749	0,0533	0,0626	0,0168	0,004	0,004	0,1372	2,980232239	32	S	Y
100	512	8	ReRo	0,0746	0,0541	0,0622	0,0178	0,004	0,004	0,1372	2,980232239	32	S	Y
100	512	8	ReCo	0,0753	0,0537	0,0628	0,0172	0,004	0,004	0,1372	2,980232239	32	S	Y
100	512	8	RoCo	0,0757	0,0534	0,0633	0,0168	0,004	0,004	0,1372	2,980232239	32	S	Y
100	512	8	ReTr	0,0753	0,0535	0,0627	0,017	0,004	0,004	0,1372	2,980232239	32	S	Y
100	512	16	ReO	0,1433	0,109	0,123	0,044	0,0079	0,0079	0,1551	5,960464478	32	S	Y
100	512	16	ReRo	0,1462	0,1082	0,1253	0,0429	0,0079	0,0079	0,1551	5,960464478	32	S	Y
100	512	16	ReCo	0,1462	0,1086	0,1255	0,0429	0,0079	0,0079	0,1551	5,960464478	32	S	Y
100	512	16	RoCo	0,1475	0,1078	0,1268	0,0417	0,0079	0,0079	0,1551	5,960464478	32	S	Y
100	512	16	ReTr	0,1433	0,1108	0,1224	0,0454	0,0079	0,0079	0,1551	5,960464478	32	S	Y
100	512	32	ReO	0,3466	0,2848	0,2956	0,1566	0,0159	0,0159	0,1941	11,92092896	32	S	Y
100	512	32	ReRo	0,3489	0,285	0,2984	0,1563	0,0159	0,0159	0,1941	11,92092896	32	S	Y
100	512	32	ReCo	0,3533	0,2838	0,3014	0,1535	0,0159	0,0159	0,1941	11,92092896	32	S	Y
100	512	32	RoCo	0,3502	0,2865	0,2983	0,1572	0,0159	0,0159	0,1941	11,92092896	32	S	Y
100	512	32	ReTr	0,3491	0,2849	0,298	0,1552	0,0159	0,0159	0,1941	11,92092896	32	S	Y
100	1024	8	ReO	0,066	0,0535	0,0542	0,0208	0	0	0,2462	2,980232239	32	S	Y
100	1024	8	ReRo	0,0718	0,0509	0,0587	0,0165	0	0	0,2462	2,980232239	32	S	Y
100	1024	8	ReCo	0,0678	0,0537	0,0549	0,0204	0	0	0,2462	2,980232239	32	S	Y
100	1024	8	RoCo	0,0721	0,0508	0,0589	0,0164	0	0	0,2462	2,980232239	32	S	Y
100	1024	8	ReTr	0,0724	0,0505	0,0594	0,016	0	0	0,2462	2,980232239	32	S	Y
100	1024	16	ReO	0,1397	0,1003	0,1183	0,0402	0	0	0,2603	5,960464478	32	S	Y
100	1024	16	ReRo	0,135	0,1043	0,1135	0,0455	0	0	0,2603	5,960464478	32	S	Y

100	1024	16	ReCo	0,1343	0,104	0,1139	0,045	0	0	0,2603	5,960464478	32	S	Y
100	1024	16	RoCo	0,136	0,1039	0,1148	0,0444	0	0	0,2603	5,960464478	32	S	Y
100	1024	16	ReTr	0,1357	0,1045	0,1144	0,0451	0	0	0,2603	5,960464478	32	S	Y
100	1024	32	ReO	0,3333	0,274	0,2817	0,1562	0	0	0,2993	11,92092896	32	S	Y
100	1024	32	ReRo	0,3364	0,2734	0,2844	0,1544	0	0	0,2993	11,92092896	32	S	Y
100	1024	32	ReCo	0,3359	0,2736	0,2838	0,1544	0	0	0,2993	11,92092896	32	S	Y
100	1024	32	RoCo	0,3347	0,2747	0,2825	0,1563	0	0	0,2993	11,92092896	32	S	Y
100	1024	32	ReTr	0,3389	0,2722	0,2865	0,1524	0	0	0,2993	11,92092896	32	S	Y
100	2048	8	ReO	0,0773	0,0567	0,0624	0,0176	0,004	0,004	0,4643	2,980232239	32	S	Y
100	2048	8	ReRo	0,078	0,0567	0,0631	0,0175	0,004	0,004	0,4643	2,980232239	32	S	Y
100	2048	8	ReCo	0,0788	0,056	0,0638	0,0168	0,004	0,004	0,4643	2,980232239	32	S	Y
100	2048	8	RoCo	0,0797	0,0555	0,0646	0,0161	0,004	0,004	0,4643	2,980232239	32	S	Y
100	2048	8	ReTr	0,0774	0,057	0,0624	0,0179	0,004	0,004	0,4643	2,980232239	32	S	Y
100	2048	16	ReO	0,1502	0,1113	0,1268	0,0423	0,0079	0,0079	0,4784	5,960464478	32	S	Y
100	2048	16	ReRo	0,1516	0,1111	0,1281	0,0422	0,0079	0,0079	0,4784	5,960464478	32	S	Y
100	2048	16	ReCo	0,153	0,1103	0,1296	0,0409	0,0079	0,0079	0,4784	5,960464478	32	S	Y
100	2048	16	RoCo	0,1515	0,1118	0,1282	0,0425	0,0079	0,0079	0,4784	5,960464478	32	S	Y
100	2048	16	ReTr	0,1486	0,1138	0,1254	0,0446	0,0079	0,0079	0,4784	5,960464478	32	S	Y
100	2048	32	ReO	0,3555	0,2931	0,301	0,1607	0,0159	0,0159	0,5099	11,92092896	32	S	Y
100	2048	32	ReRo	0,358	0,2942	0,3028	0,1617	0,0159	0,0159	0,5099	11,92092896	32	S	Y
100	2048	32	ReCo	0,3599	0,2932	0,3051	0,1595	0,0159	0,0159	0,5099	11,92092896	32	S	Y
100	2048	32	RoCo	0,359	0,2949	0,3039	0,1613	0,0159	0,0159	0,5099	11,92092896	32	S	Y
100	2048	32	ReTr	0,3572	0,2947	0,3018	0,1611	0,0159	0,0159	0,5099	11,92092896	32	S	Y
100	4096	8	ReO	0	0	0	0	0	0	0	0	32	S	Y
100	4096	8	ReRo	0	0	0	0	0	0	0	0	32	S	Y
100	4096	8	ReCo	0	0	0	0	0	0	0	0	32	S	Y
100	4096	8	RoCo	0	0	0	0	0	0	0	0	32	S	Y

100	4096	8	ReTr	0	0	0	0	0	0	0	0	32	S	Y
100	4096	16	ReO	0	0	0	0	0	0	0	0	32	S	Y
100	4096	16	ReRo	0	0	0	0	0	0	0	0	32	S	Y
100	4096	16	ReCo	0	0	0	0	0	0	0	0	32	S	Y
100	4096	16	RoCo	0	0	0	0	0	0	0	0	32	S	Y
100	4096	16	ReTr	0	0	0	0	0	0	0	0	32	S	Y
100	4096	32	ReO	0	0	0	0	0	0	0	0	32	S	Y
100	4096	32	ReRo	0	0	0	0	0	0	0	0	32	S	Y
100	4096	32	ReCo	0	0	0	0	0	0	0	0	32	S	Y
100	4096	32	RoCo	0	0	0	0	0	0	0	0	32	S	Y
100	4096	32	ReTr	0	0	0	0	0	0	0	0	32	S	Y

Table 5 Inverse Shuffle, 32 bits, fused design

Synthesis results for Inverse Math, 32 bits, fused design.

Frequency [MHz]	Capacity [KB]	Lanes	Scheme	Logic Utilization %	LUTs Utilization %	Primary FFs Utilization %	Secondary FFs Utilization %	Multipliers25x18 Utilization %	DSP blocks Utilization %	BRAM Utilization %	Bandwidth (GB/s)	Bits	Inverse	Fused
100	512	8	ReO	0,0719	0,0497	0,062	0,0146	0,004	0,004	0,1372	2,980232239	32	M	Y
100	512	8	ReRo	0,0781	0,0507	0,0671	0,0138	0,004	0,004	0,1372	2,980232239	32	M	Y
100	512	8	ReCo	0,0776	0,0536	0,0664	0,0162	0,004	0,004	0,1372	2,980232239	32	M	Y
100	512	8	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	512	8	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	512	16	ReO	0,1407	0,092	0,1299	0,0302	0,0079	0,0079	0,1551	5,960464478	32	M	Y
100	512	16	ReRo	0,1494	0,0964	0,1366	0,0307	0,0079	0,0079	0,1551	5,960464478	32	M	Y
100	512	16	ReCo	0,1528	0,1006	0,1395	0,0324	0,0079	0,0079	0,1551	5,960464478	32	M	Y
100	512	16	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	512	16	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	512	32	ReO	0,3508	0,2373	0,3372	0,0964	0,0159	0,0159	0,1908	11,92092896	32	M	Y
100	512	32	ReRo	0,3689	0,2424	0,3528	0,0952	0,0159	0,0159	0,1908	11,92092896	32	M	Y
100	512	32	ReCo	0,3694	0,2563	0,3516	0,1052	0,0159	0,0159	0,1908	11,92092896	32	M	Y
100	512	32	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	512	32	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	1024	8	ReO	0,0602	0,0515	0,0509	0,0213	0	0	0,2462	2,980232239	32	M	Y
100	1024	8	ReRo	0,0729	0,0493	0,0611	0,0147	0	0	0,2462	2,980232239	32	M	Y
100	1024	8	ReCo	0,0743	0,051	0,0622	0,0157	0	0	0,2462	2,980232239	32	M	Y
100	1024	8	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	1024	8	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	1024	16	ReO	0,1326	0,0868	0,1205	0,031	0	0	0,2603	5,960464478	32	M	Y
100	1024	16	ReRo	0,1411	0,0902	0,1268	0,0306	0	0	0,2603	5,960464478	32	M	Y
100	1024	16	ReCo	0,1417	0,0969	0,1275	0,0351	0	0	0,2603	5,960464478	32	M	Y

100	1024	8	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	1024	8	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	1024	32	ReO	0,3379	0,225	0,324	0,0951	0	0	0,2961	11,92092896	32	M	Y
100	1024	32	ReRo	0,3563	0,2274	0,3397	0,0915	0	0	0,2961	11,92092896	32	M	Y
100	1024	32	ReCo	0,3639	0,2362	0,3453	0,0947	0	0	0,2961	11,92092896	32	M	Y
100	1024	32	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	1024	32	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	2048	8	ReO	0,0768	0,0508	0,0643	0,013	0,004	0,004	0,4643	2,980232239	32	M	Y
100	2048	8	ReRo	0,0803	0,0541	0,0669	0,0146	0,004	0,004	0,4643	2,980232239	32	M	Y
100	2048	8	ReCo	0,0832	0,0542	0,0693	0,0138	0,004	0,004	0,4643	2,980232239	32	M	Y
100	2048	8	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	2048	8	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	2048	16	ReO	0,144	0,0967	0,1303	0,0316	0,0079	0,0079	0,4784	5,960464478	32	M	Y
100	2048	16	ReRo	0,1511	0,1024	0,1354	0,0338	0,0079	0,0079	0,4784	5,960464478	32	M	Y
100	2048	16	ReCo	0,1578	0,1039	0,1417	0,0322	0,0079	0,0079	0,4784	5,960464478	32	M	Y
100	2048	16	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	2048	16	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	2048	32	ReO	0,3577	0,2469	0,342	0,1007	0,0159	0,0159	0,5066	11,92092896	32	M	Y
100	2048	32	ReRo	0,374	0,2537	0,3557	0,1015	0,0159	0,0159	0,5066	11,92092896	32	M	Y
100	2048	32	ReCo	0,3832	0,2601	0,3631	0,1029	0,0159	0,0159	0,5066	11,92092896	32	M	Y
100	2048	32	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	2048	32	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	4096	8	ReO	0,0778	0,054	0,06	0,0133	0	0	0,9004	2,980232239	32	M	Y
100	4096	8	ReRo	0,0837	0,0552	0,0646	0,0124	0	0	0,9004	2,980232239	32	M	Y
100	4096	8	ReCo	0,0842	0,0576	0,065	0,014	0	0	0,9004	2,980232239	32	M	Y
100	4096	16	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	4096	16	ReTr	0	0	0	0	0	0	0	0	32	M	Y

100	4096	16	ReO	0,1439	0,0901	0,1267	0,0279	0	0	0,9145	5,960464478	32	M	Y
100	4096	16	ReRo	0,1505	0,0956	0,1312	0,0294	0	0	0,9145	5,960464478	32	M	Y
100	4096	16	ReCo	0,1564	0,0979	0,1367	0,029	0	0	0,9145	5,960464478	32	M	Y
100	4096	16	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	4096	16	ReTr	0	0	0	0	0	0	0	0	32	M	Y
100	4096	32	ReO	0,352	0,2339	0,3332	0,0957	0	0	0,9427	11,92092896	32	M	Y
100	4096	32	ReRo	0,3692	0,2387	0,3473	0,0937	0	0	0,9427	11,92092896	32	M	Y
100	4096	32	ReCo	0,375	0,2491	0,3513	0,0985	0	0	0,9427	11,92092896	32	M	Y
100	4096	32	RoCo	0	0	0	0	0	0	0	0	32	M	Y
100	4096	32	ReTr	0	0	0	0	0	0	0	0	32	M	Y

Table 6 Inverse Math, 32 bits, fused design

Synthesis results for Inverse Math, 32 bits, split design.

Frequency [MHz]	Capacity [KB]	Lanes	Scheme	Logic Utilization %	LUTs Utilization %	Primary FFs Utilization %	Secondary FFs Utilization %	Multipliers25x18 Utilization %	DSP blocks Utilization %	BRAM Utilization %	Bandwidth (GB/s)	Bits	Inverse	Fused
100	512	8	ReO	13,41%	9,05%	11,29%	2,65%	1,19%	1,19%	18,42%	2,980232239	32	M	N
100	512	8	ReRo	12,66%	11,37%	10,79%	4,93%	1,19%	1,19%	18,52%	2,980232239	32	M	N
100	512	8	ReCo	14,69%	10,23%	12,36%	3,30%	1,19%	1,19%	18,52%	2,980232239	32	M	N
100	512	8	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	2,980232239	32	M	N
100	512	8	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	2,980232239	32	M	N
100	512	16	ReO	25,75%	16,47%	22,70%	4,98%	2,38%	2,38%	24,62%	5,960464478	32	M	N
100	512	16	ReRo	28,73%	18,84%	25,05%	6,08%	2,38%	2,38%	24,72%	5,960464478	32	M	N
100	512	16	ReCo	28,46%	18,84%	24,95%	6,21%	2,38%	2,38%	24,72%	5,960464478	32	M	N
100	512	16	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	5,960464478	32	M	N
100	512	16	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	5,960464478	32	M	N
100	512	32	ReO	50,48%	39,46%	45,94%	22,88%	4,76%	4,76%	37,03%	11,92092896	32	M	N
100	512	32	ReRo	57,29%	43,57%	51,73%	24,44%	4,76%	4,76%	37,12%	11,92092896	32	M	N
100	512	32	ReCo	56,38%	43,95%	50,87%	24,92%	4,76%	4,76%	37,12%	11,92092896	32	M	N
100	512	32	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	11,92092896	32	M	N
100	512	32	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	11,92092896	32	M	N
80	1024	8	ReO	13,45%	8,94%	11,23%	2,55%	0,00%	0,00%	29,32%	2,384185791	32	M	N
80	1024	8	ReRo	14,72%	10,37%	12,19%	3,37%	0,00%	0,00%	29,42%	2,384185791	32	M	N
80	1024	8	ReCo	14,74%	10,14%	12,28%	3,21%	0,00%	0,00%	29,42%	2,384185791	32	M	N
100	1024	8	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	2,980232239	32	M	N
100	1024	8	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	2,980232239	32	M	N
100	1024	16	ReO	25,56%	16,34%	22,49%	4,86%	0,00%	0,00%	35,15%	5,960464478	32	M	N
100	1024	16	ReRo	28,46%	18,76%	24,74%	6,05%	0,00%	0,00%	35,24%	5,960464478	32	M	N

100	1024	16	ReCo	28,43%	18,66%	24,85%	5,98%	0,00%	0,00%	35,24%	5,960464478	32	M	N
100	1024	16	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	5,960464478	32	M	N
100	1024	16	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	5,960464478	32	M	N
100	1024	32	ReO	49,86%	39,14%	45,22%	22,91%	0,00%	0,00%	47,56%	11,92092896	32	M	N
100	1024	32	ReRo	56,51%	43,33%	51,01%	24,59%	0,00%	0,00%	47,65%	11,92092896	32	M	N
100	1024	32	ReCo	55,87%	43,26%	50,44%	24,66%	0,00%	0,00%	47,65%	11,92092896	32	M	N
100	1024	32	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	11,92092896	32	M	N
100	1024	32	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	11,92092896	32	M	N
100	2048	8	ReO	14,01%	9,05%	11,59%	2,37%	1,19%	1,19%	51,13%	2,980232239	32	M	N
100	2048	8	ReRo	15,81%	10,09%	13,03%	2,71%	1,19%	1,19%	51,22%	2,980232239	32	M	N
100	2048	8	ReCo	15,57%	10,04%	12,89%	2,78%	1,19%	1,19%	51,22%	2,980232239	32	M	N
100	2048	8	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	2,980232239	32	M	N
100	2048	8	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	2,980232239	32	M	N
100	2048	16	ReO	25,63%	16,99%	22,46%	5,24%	2,38%	2,38%	56,95%	5,960464478	32	M	N
100	2048	16	ReRo	28,70%	19,31%	24,92%	6,24%	2,38%	2,38%	57,05%	5,960464478	32	M	N
100	2048	16	ReCo	29,12%	18,84%	25,42%	5,76%	2,38%	2,38%	57,05%	5,960464478	32	M	N
100	2048	16	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	5,960464478	32	M	N
100	2048	16	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	5,960464478	32	M	N
100	2048	32	ReO	50,75%	39,64%	46,22%	22,64%	4,76%	4,76%	68,61%	11,92092896	32	M	N
100	2048	32	ReRo	56,32%	44,66%	50,85%	25,36%	4,76%	4,76%	68,70%	11,92092896	32	M	N
100	2048	32	ReCo	56,73%	43,94%	51,25%	24,59%	4,76%	4,76%	68,70%	11,92092896	32	M	N
100	2048	32	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	11,92092896	32	M	N
100	2048	32	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	11,92092896	32	M	N
75	4096	8	ReO	14,40%	9,51%	11,44%	2,35%	0,00%	0,00%	94,74%	2,235174179	32	M	N
75	4096	8	ReRo	15,19%	11,39%	11,97%	3,61%	0,00%	0,00%	94,83%	2,235174179	32	M	N
75	4096	8	ReCo	13,28%	12,09%	10,51%	5,00%	0,00%	0,00%	94,83%	2,235174179	32	M	N
75	4096	8	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	2,235174179	32	M	N

75	4096	8	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	2,235174179	32	M	N
75	4096	16	ReO	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	4,470348358	32	M	N
75	4096	16	ReRo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	4,470348358	32	M	N
75	4096	16	ReCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	4,470348358	32	M	N
75	4096	16	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	4,470348358	32	M	N
75	4096	16	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	4,470348358	32	M	N
75	4096	32	ReO	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	8,940696716	32	M	N
75	4096	32	ReRo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	8,940696716	32	M	N
75	4096	32	ReCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	8,940696716	32	M	N
75	4096	32	RoCo	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	8,940696716	32	M	N
75	4096	32	ReTr	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	0,00%	8,940696716	32	M	N

Table 7 Inverse Math, 32 bits, split design

Maximum Frequency results for Inverse Shuffle, 64 bits, fused design.

Tempted Frequency [MHz]	Problem	Capacity [KB]	Lanes	Sheme	Min ns [ns]	Max Frequency [MHz]	Bandwidth [GB/s]
300MHz	STREAM	512	8	ReO	5,095	196,2708538	11,69865452
300MHz	STREAM	512	8	ReRo	5,04	198,4126984	11,82631841
300MHz	STREAM	512	8	ReCo	4,84	206,6115702	12,31500925
300MHz	STREAM	512	8	RoCo	4,6	217,3913043	12,95753147
300MHz	STREAM	512	8	ReTr	5,259	190,1502187	11,33383624
300MHz	STREAM	512	16	ReO	5,197	192,4187031	22,93809689
300MHz	STREAM	512	16	ReRo	4,976	200,9646302	23,95685079
300MHz	STREAM	512	16	ReCo	5,534	180,7011203	21,54125218
300MHz	STREAM	512	16	RoCo	4,738	211,0595188	25,16025529
300MHz	STREAM	512	16	ReTr	5,388	185,5976244	22,12496094
300MHz	STREAM	1024	8	ReO	5,569	179,5654516	10,70293496
300MHz	STREAM	1024	8	ReRo	5,671	176,3357433	10,51042934
300MHz	STREAM	1024	8	ReCo	6,635	150,7159005	8,983367713
300MHz	STREAM	1024	8	RoCo	5,836	171,3502399	10,21327018
300MHz	STREAM	1024	8	ReTr	5,807	172,2059583	10,26427497
300MHz	STREAM	1024	16	ReO	6,449	155,0628004	18,48492628
300MHz	STREAM	1024	16	ReRo	5,94	168,3501684	20,06890396
300MHz	STREAM	1024	16	ReCo	6	166,6666667	19,86821493
300MHz	STREAM	1024	16	RoCo	6,457	154,870683	18,46202409
300MHz	STREAM	1024	16	ReTr	6,325	158,1027668	18,84731851
300MHz	STREAM	2048	8	ReO	7,521	132,9610424	7,925095702
300MHz	STREAM	2048	8	ReRo	6,712	148,9868892	8,880310604
300MHz	STREAM	2048	8	ReCo	7,365	135,7773252	8,092959236

300MHz	STREAM	2048	8	RoCo	7,573	132,0480655	7,870678037
300MHz	STREAM	2048	8	ReTr	7,122	140,4099972	8,369088006
300MHz	STREAM	2048	16	ReO	6,755	148,03849	17,64756322
300MHz	STREAM	2048	16	ReRo	6,455	154,9186677	18,46774431
300MHz	STREAM	2048	16	ReCo	7,104	140,7657658	16,78058693
300MHz	STREAM	2048	16	RoCo	7,482	133,6541032	15,93281069
300MHz	STREAM	2048	16	ReTr	6,67	149,9250375	17,8724572
300MHz	STREAM	4096	8	ReO	9,075	110,1928375	6,568004934
300MHz	STREAM	4096	8	ReRo	8,994	111,1852346	6,627156413
300MHz	STREAM	4096	8	ReCo	8,785	113,8303927	6,784820122
300MHz	STREAM	4096	8	RoCo	8,687	115,114539	6,861361204
300MHz	STREAM	4096	8	ReTr	8,295	120,5545509	7,185611184

Table 8 Inverse Shuffle, 64 bits, fused design

Maximum Frequency results for Inverse Shuffle, 64 bits, fused design.

Tempted Frequency [MHz]	Problem	Capacity [KB]	Lanes	Sheme	Min ns [ns]	Max Frequency [MHz]	Bandwidth [GB/s]
300MHz	STREAM	1024	8	ReO	5,696	175,5617978	10,46429859
300MHz	STREAM	1024	8	ReRo	6,056	165,1254954	9,842246495
300MHz	STREAM	1024	8	ReCo	5,401	185,150898	11,0358535
300MHz	STREAM	1024	8	RoCo	NA		
300MHz	STREAM	1024	8	ReTr	NA		
300MHz	STREAM	1024	16	ReO	6,817	146,6920933	17,48706022
300MHz	STREAM	1024	16	ReRo	6,174	161,9695497	19,30827495
300MHz	STREAM	1024	16	ReCo	7,755	128,9490651	15,37192644
300MHz	STREAM	1024	16	RoCo	NA		
300MHz	STREAM	1024	16	ReTr	NA		

Table 9 Maximum Frequency results for Inverse Shuffle, 64 bits, fused design

Maximum Frequency results for Inverse Math, 32 bits, split design.

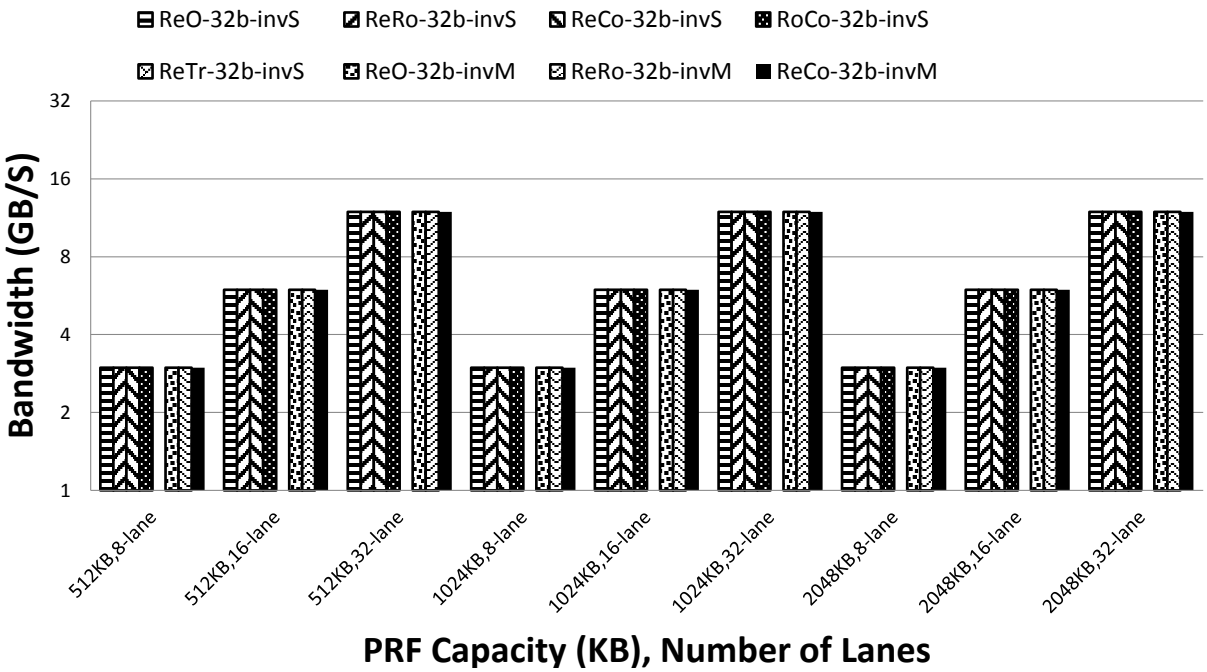
Tempted Frequency [MHz]	Problem	Capacity [KB]	Lanes	Sheme	Min ns [ns]	Max Frequency [MHz]	Bandwidth [GB/s]
300MHz	STREAM	512	8	ReRo	9,083	110,0957833	6,880986458
300MHz	STREAM	512	8	ReO	8,187	122,1448638	7,634053988
300MHz	STREAM	512	8	ReCo	9,569	104,5041279	6,531507995
300MHz	STREAM	512	16	ReRo	7,03	142,2475107	17,78093883
300MHz	STREAM	512	16	ReO	7,736	129,2657704	16,1582213
300MHz	STREAM	512	16	ReCo	7,409	134,9709812	16,87137265
300MHz	STREAM	512	32	ReRo	8,848	113,0198915	28,25497288
300MHz	STREAM	512	32	ReO	11,717	85,34607835	21,33651959
300MHz	STREAM	512	32	ReCo	10,701	93,44921035	23,36230259
300MHz	STREAM	1024	8	ReRo	13,33	75,01875469	4,688672168
300MHz	STREAM	1024	8	ReO	10,706	93,40556697	5,837847936
300MHz	STREAM	1024	8	ReCo	9,847	101,5537727	6,347110795
300MHz	STREAM	1024	16	ReRo	8,06	124,0694789	15,50868486
300MHz	STREAM	1024	16	ReO	7,28	137,3626374	17,17032967
300MHz	STREAM	1024	16	ReCo	8,498	117,674747	14,70934337
300MHz	STREAM	1024	32	ReRo	8,549	116,9727454	29,24318634
300MHz	STREAM	1024	32	ReO	8,731	114,5344176	28,6336044
300MHz	STREAM	1024	32	ReCo	8,582	116,522955	29,13073876
300MHz	STREAM	2048	8	ReRo	10,491	95,31979792	5,95748737
300MHz	STREAM	2048	8	ReO	9,221	108,4481076	6,778006724
300MHz	STREAM	2048	8	ReCo	10,054	99,46290034	6,216431271
300MHz	STREAM	2048	16	ReRo	11,841	84,45232666	10,55654083

300MHz	STREAM	2048	16	ReO	11,261	88,80206021	11,10025753
300MHz	STREAM	2048	16	ReCo	8,664	115,4201293	14,42751616
300MHz	STREAM	2048	32	ReRo	11,529	86,73779166	21,68444791
300MHz	STREAM	2048	32	ReO	10,775	92,80742459	23,20185615
300MHz		2048	32	ReCo			0
300MHz	STREAM	4096	8	ReRo	10,255	97,51340809	6,094588006
300MHz	STREAM	4096	8	ReO	10,218	97,86651008	6,11665688
300MHz	STREAM	4096	8	ReCo	17,209	58,10912894	3,631820559
300MHz	STREAM	4096	16	ReRo	10,255	97,51340809	12,18917601
300MHz	STREAM	4096	16	ReO	10,218	97,86651008	12,23331376
300MHz	STREAM	4096	16	ReCo	17,209	58,10912894	7,263641118
300MHz	STREAM	4096	32	ReRo	10,255	97,51340809	24,37835202
300MHz	STREAM	4096	32	ReO	10,218	97,86651008	24,46662752
300MHz	STREAM	4096	32	ReCo	17,209	58,10912894	14,52728224

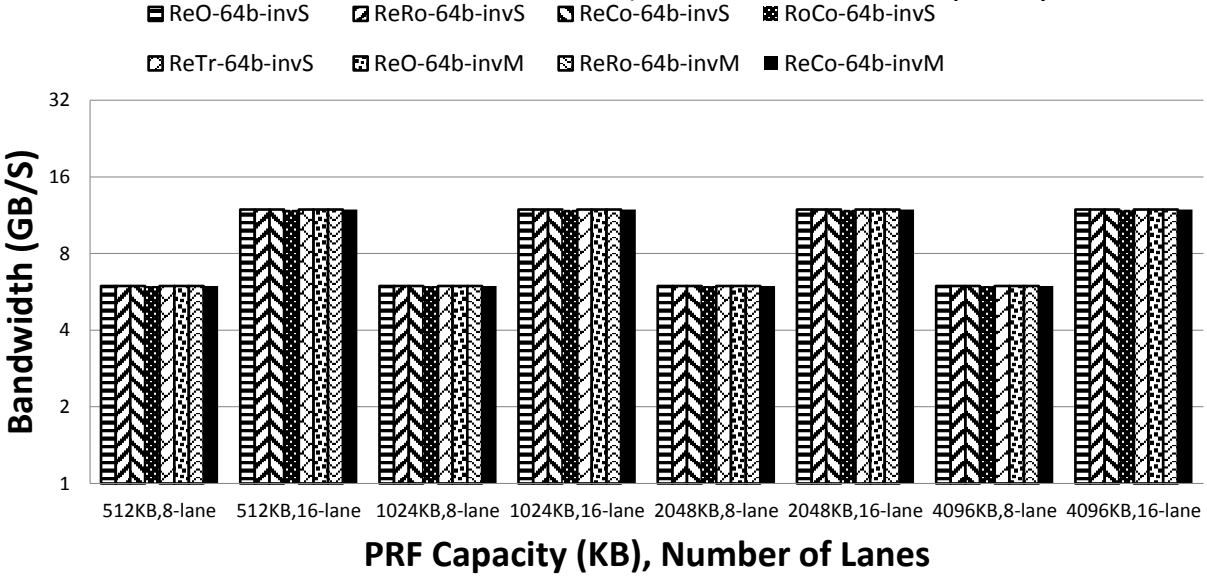
Table 10 Maximum Frequency results for Inverse Math, 32 bits, split design

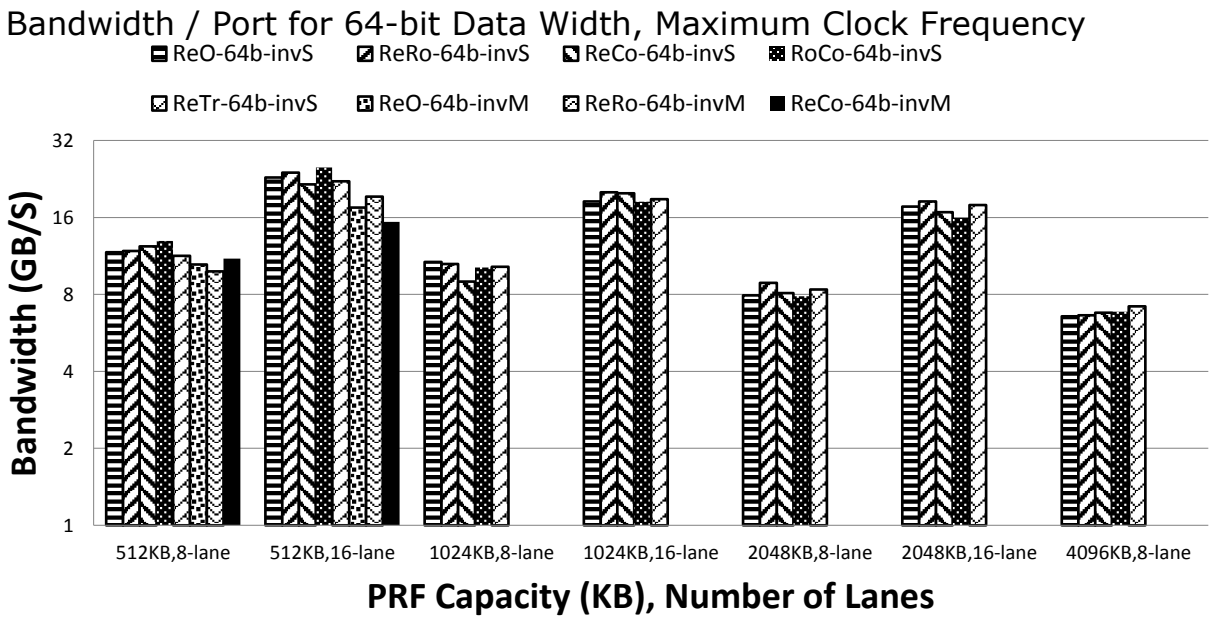
3. Graphs resulting from the analysis

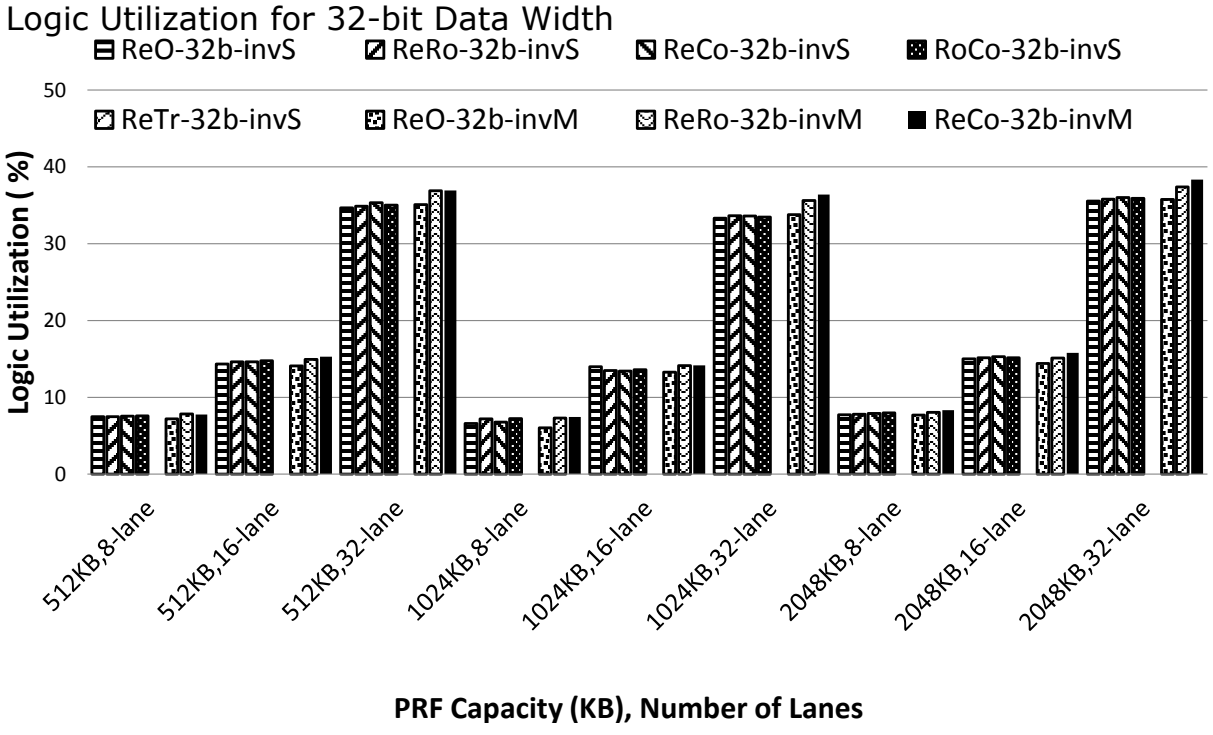
Bandwidth / Port for 32-bit Data Width, 100MHz Clock Frequency

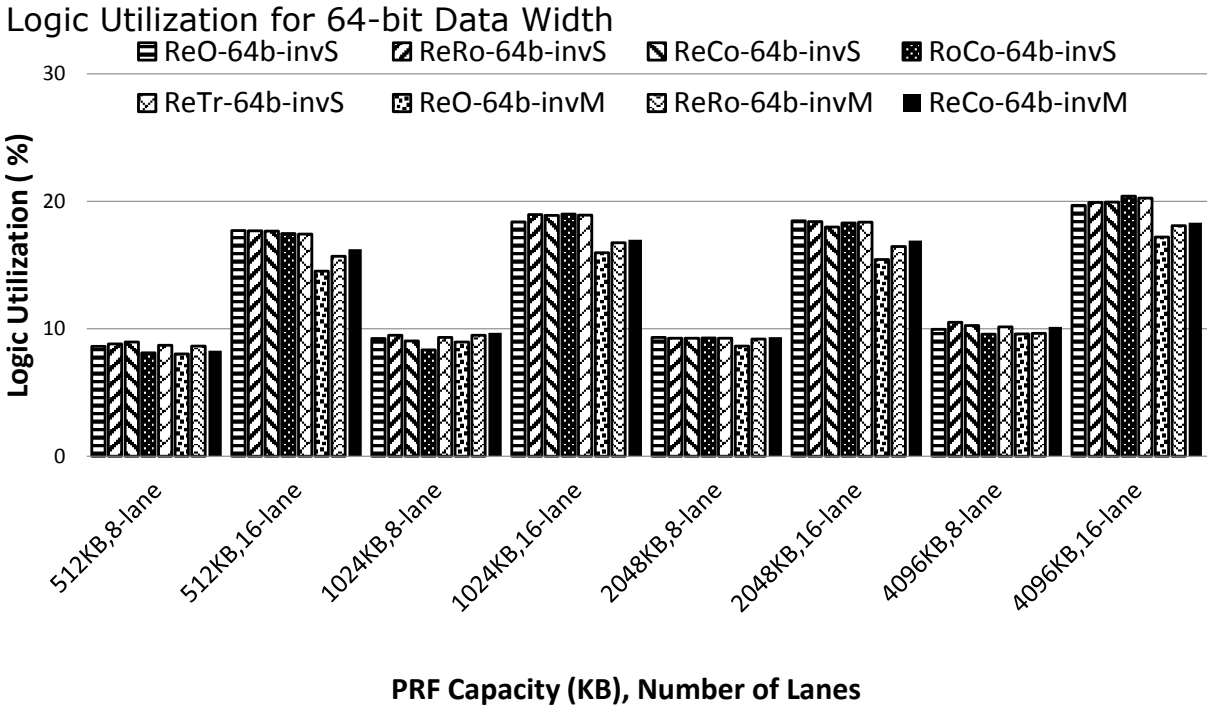


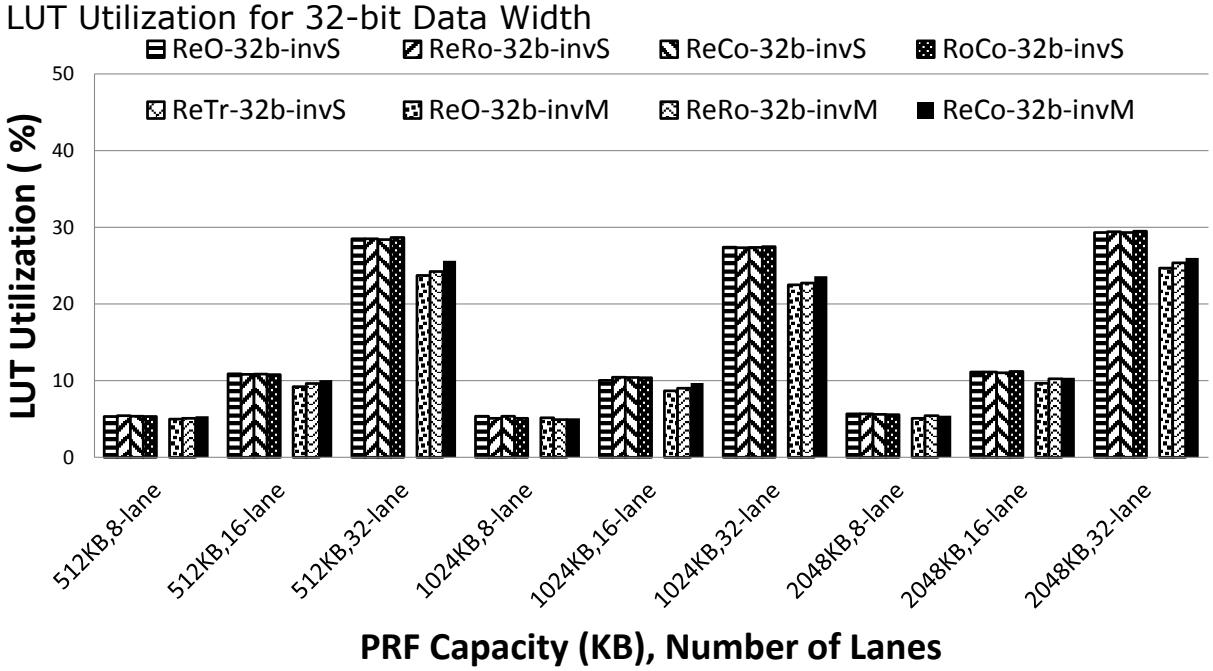
Bandwidth / Port for 64-bit Data Width, 100MHz Clock Frequency

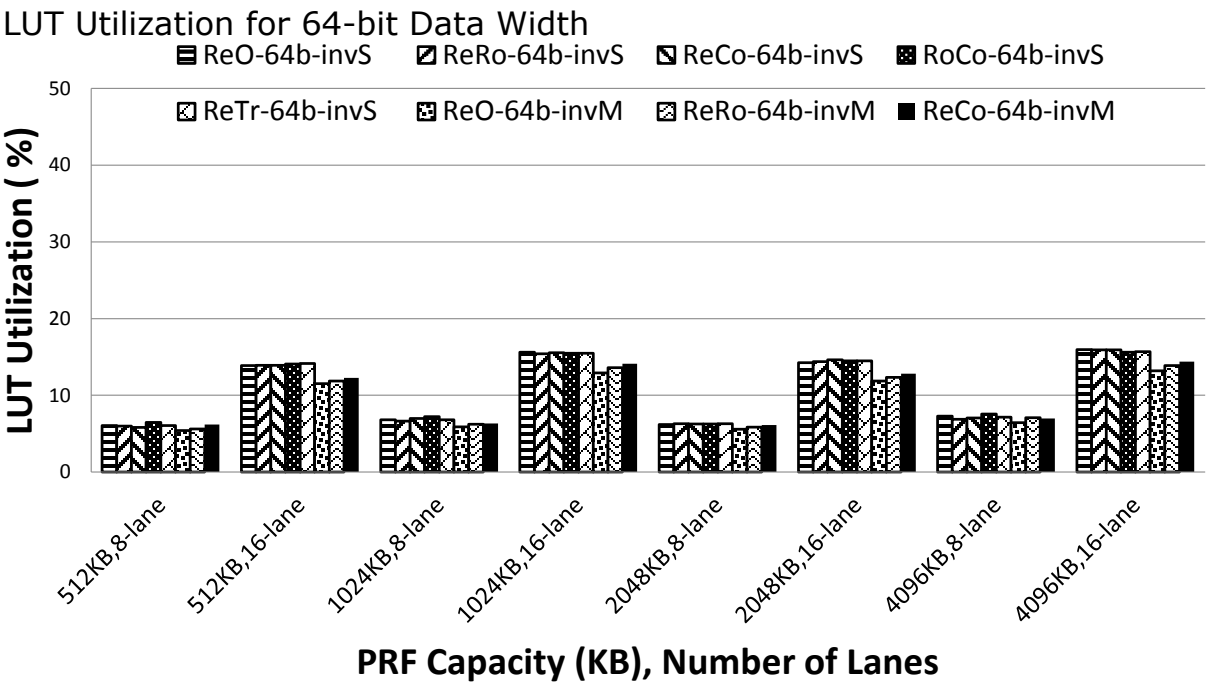


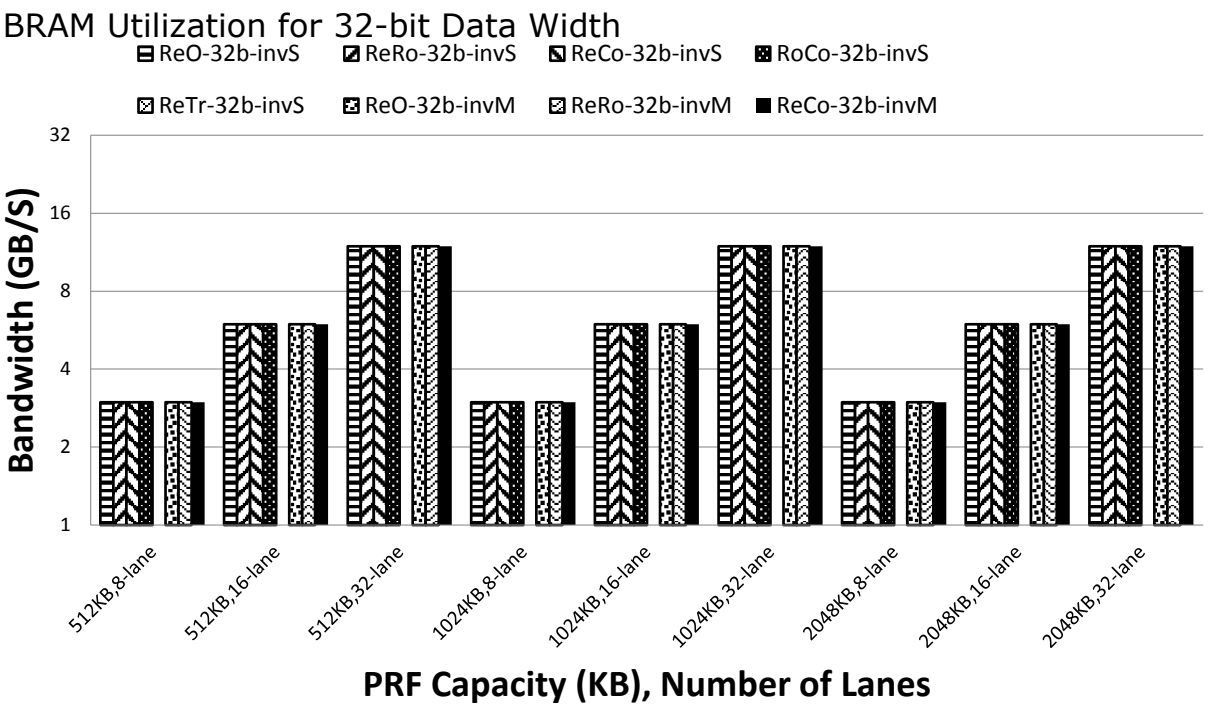

Bandwidth / Port for 64-bit Data Width, Maximum Clock Frequency
ReO-64b-invS
ReRo-64b-invS
ReCo-64b-invS
RoCo-64b-invS
ReTr-64b-invS
ReO-64b-invM
ReRo-64b-invM
ReCo-64b-invM
Bandwidth (GB/S)
32
16
8
4
2
1
512KB,8-lane
512KB,16-lane
1024KB,8-lane
1024KB,16-lane
2048KB,8-lane
2048KB,16-lane
4096KB,8-lane
PRF Capacity (KB), Number of Lanes

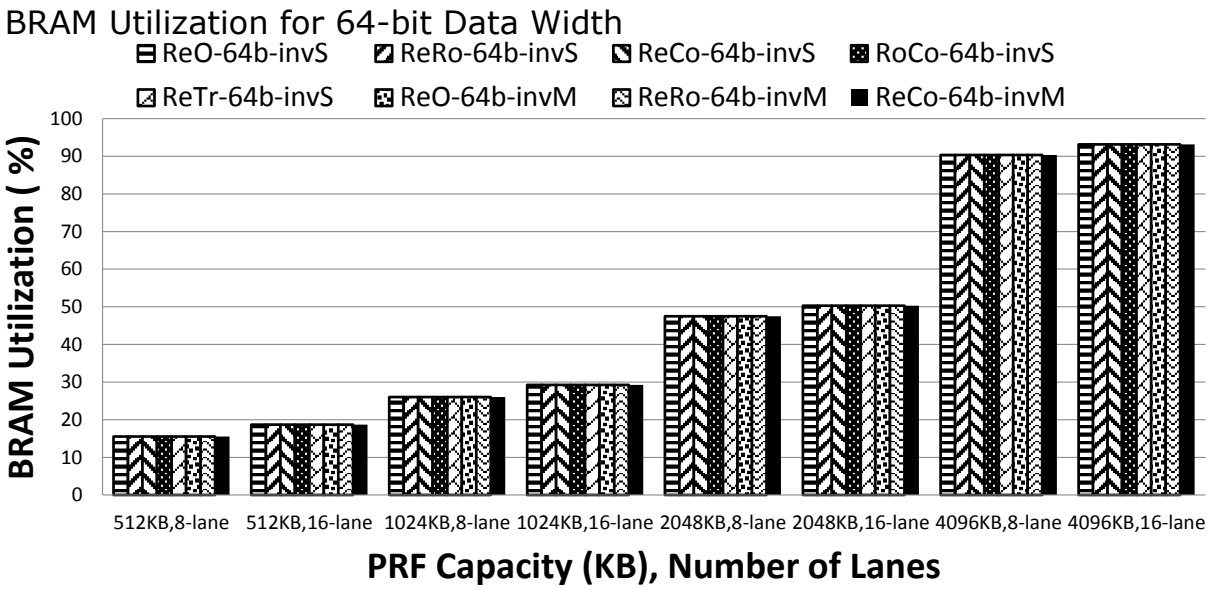

Logic Utilization for 32-bit Data Width
ReO-32b-invS
ReRo-32b-invS
ReCo-32b-invS
RoCo-32b-invS
ReTr-32b-invS
ReO-32b-invM
ReRo-32b-invM
ReCo-32b-invM
Logic Utilization (%)
50
40
30
20
10
0
512KB,8-lane
512KB,16-lane
512KB,32-lane
1024KB,8-lane
1024KB,16-lane
1024KB,32-lane
2048KB,8-lane
2048KB,16-lane
2048KB,32-lane
PRF Capacity (KB), Number of Lanes


Logic Utilization for 64-bit Data Width
ReO-64b-invS
ReRo-64b-invS
ReCo-64b-invS
RoCo-64b-invS
ReTr-64b-invS
ReO-64b-invM
ReRo-64b-invM
ReCo-64b-invM
Logic Utilization (%)
30
20
10
0
512KB,8-lane
512KB,16-lane
1024KB,8-lane
1024KB,16-lane
2048KB,8-lane
2048KB,16-lane
4096KB,8-lane
4096KB,16-lane
PRF Capacity (KB), Number of Lanes


LUT Utilization for 32-bit Data Width
ReO-32b-invS
ReRo-32b-invS
ReCo-32b-invS
RoCo-32b-invS
ReTr-32b-invS
ReO-32b-invM
ReRo-32b-invM
ReCo-32b-invM
LUT Utilization (%)
50
40
30
20
10
0
512KB,8-lane
512KB,16-lane
512KB,32-lane
1024KB,8-lane
1024KB,16-lane
1024KB,32-lane
2048KB,8-lane
2048KB,16-lane
2048KB,32-lane
PRF Capacity (KB), Number of Lanes


LUT Utilization for 64-bit Data Width
ReO-64b-invS
ReRo-64b-invS
ReCo-64b-invS
RoCo-64b-invS
ReTr-64b-invS
ReO-64b-invM
ReRo-64b-invM
ReCo-64b-invM
LUT Utilization (%)
50
40
30
20
10
0
512KB,8-lane
512KB,16-lane
1024KB,8-lane
1024KB,16-lane
2048KB,8-lane
2048KB,16-lane
4096KB,8-lane
4096KB,16-lane
PRF Capacity (KB), Number of Lanes


BRAM Utilization for 32-bit Data Width
ReO-32b-invS
ReRo-32b-invS
ReCo-32b-invS
RoCo-32b-invS
ReTr-32b-invS
ReO-32b-invM
ReRo-32b-invM
ReCo-32b-invM
Bandwidth (GB/S)
32
16
8
4
2
1
512KB,8-lane
512KB,16-lane
512KB,32-lane
1024KB,8-lane
1024KB,16-lane
1024KB,32-lane
2048KB,8-lane
2048KB,16-lane
2048KB,32-lane
PRF Capacity (KB), Number of Lanes



4. Summary

In total we ran 345 synthesis experiments, so far we present results for 295.

Works Cited

[1] C. Ciobanu and A. R. Georgi Kuzmanov, "A Polymorphic Register File for Matrix Operations," in *Proceedings of SAMOS*, 2010.