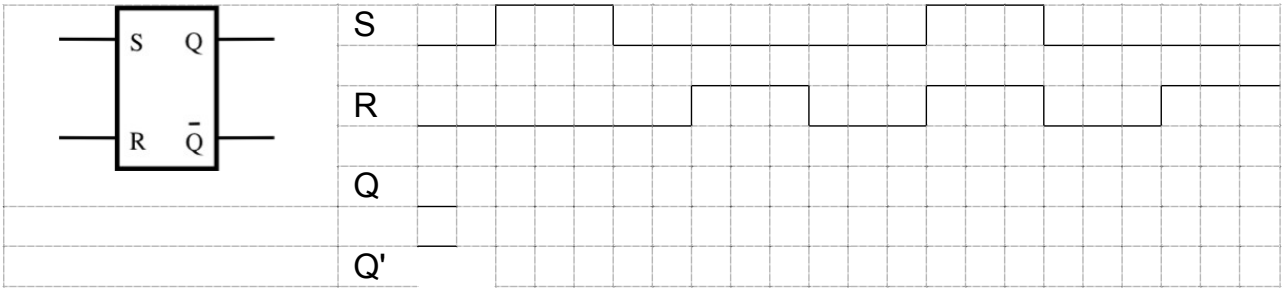
Lógica Digital (1001351): **Latches & Flip-flops**

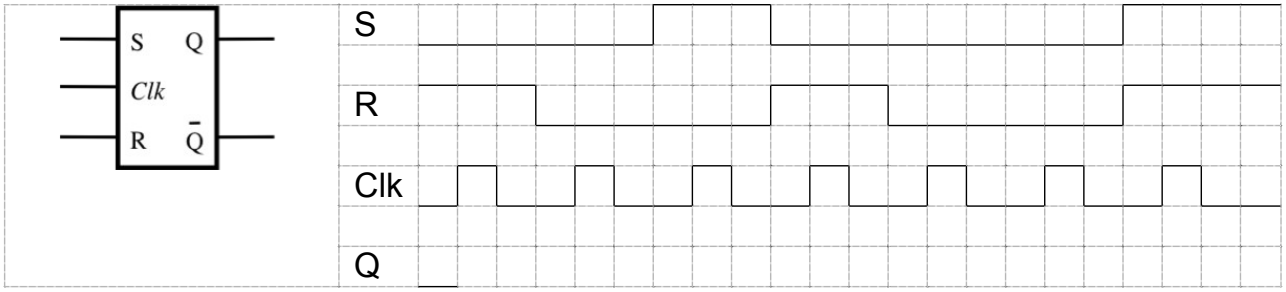
| **RA:** [ ] **Nome**: |
|---|

## 1. Para cada um dos elementos a seguir, forneça a saída correta da simulação:

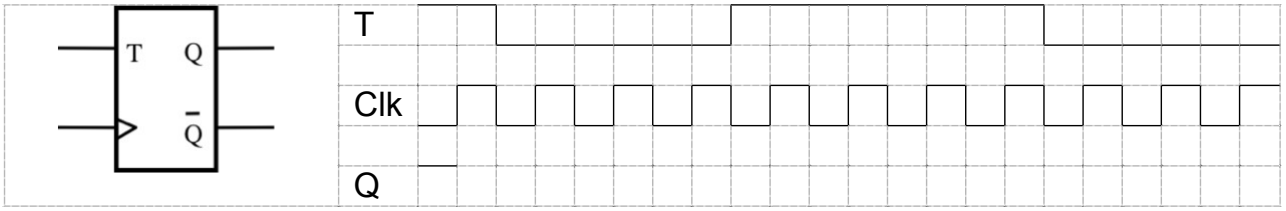
a)



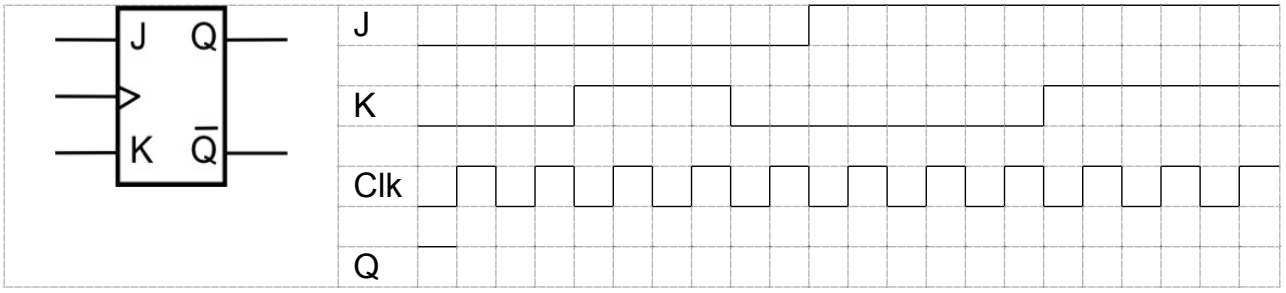

b)




c)




d)



## 2. Para cada um dos códigos a seguir, forneça o circuito resultante (observe que = ≠ <= ):

a)
```
module foo1 (a, b, c, clk, x, y);
  input a, b, c, clk;
  output reg x, y;
  always @(posedge clk)
  begin
    x <= a | b;
    y <= x ~& c;
  end
endmodule
```

b)
```
module bar1 (a, b, c, clk, x, y, w);
  input a, b, c, clk;
  output reg x, y, w;
  always @(negedge clk)
  begin
    x <= a | b;
    y <= x ~& c;
    w <= a | y;
  end
endmodule
```

c)
```
module foo2 (a, b, c, clk, x, y);
  input a, b, c, clk;
  output reg x, y;
  always @(negedge clk)
  begin
    x = a | b;
    y = x ~^ c;
  end
endmodule
```

d)
```
module bar2 (a, b, c, clk, x, y, w);
  input a, b, c, clk;
  output reg x, y, w;
  always @(posedge clk)
  begin
    x = a ^ c;
    y = ~b;
    w = x | y;
  end
endmodule
```