

Engineering System on Chip (SoC) Flows for SkyWater 130nm Open PDK



James E. Stine
Oklahoma State University
FOSSi Dial-Up
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Outline

- Introduction
- SoC Design for SkyWater 130nm
- Standard cell review
- Conclusion



Who are we?



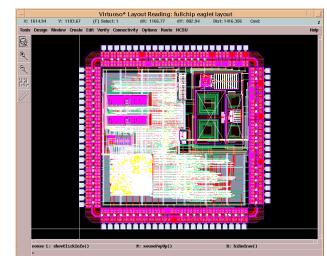
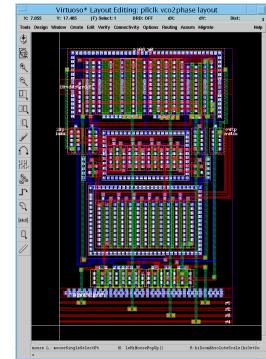
Who are we?

- More than 25 years of experience designing standard cells for MOSIS, FreePDK45, EDA companies, and other academic pursuits
- Our area of research interest is in the design of computer arithmetic and architectures.
 - However, many of our designs needed some form of implementation.
- I started along with many talented students designing System on Chip Design Flows to help alleviate this problem as it was difficult to acquire standard-cells and IP from companies.
 - Goal: to help others in learning how to work with and create these design flows.

History



- Our OSU team has a strong history of SoC design flows including many forms of IP.
- Designed cells for use with MOSIS SCMOS PDK
 - <http://freepdk.ecen.okstate.edu>
- Semiconductor Research Corporation (SRC) FreePDK45
 - Design cells for use with this technology along with Rhett Davis/NCSU
- Co-Developed initial NSF-funded OpenRAM with Professor Matt Guthaus who leads the movement to providing open-source memories.
- Cell Libraries, IO pads, memories, and flows for Cadence Design Systems GPDK
- Designed memories, cell libraries and flows for Synopsys and Mentor Graphics Corporation for use with their toolsets.
- Designed cell sets for Air Force Research Laboratory (AFRL).
- Many others, as well.



Motivation

- **Goal:** help others with the process of designing and exploring the wonderful area of System on Chip (SoC) design and use our experience to push the envelope of what we can discover.
- We set out to create an alternative standard cell kit to the pre-existing Skywater cells, with constant updates and active support.
- You can reach us any time on skywater-pdk.slack.com in the #osu slack channel. We welcome both ideas and requests!



Motivation (Continued)

- In addition, we want to share our knowledge of standard cell design so that others may be able to create their own cells in this open-source technology.
- The git repository containing our source files and full flow is published at
 - https://foss-eda-tools.googlesource.com/skywater-pdk/libs/sky130_osu_sc/
- Our cells are always a work in progress that we hope to keep updating!

SkyWater 130nm Standard Cells

- The SkyWater 130nm PDK comes with several standard cell kits:

Standard cell library	Type	Cell height	MOSFET threshold	
			nfet	pfet
sky130_fd_sc_hs	High Speed	9T (3.33um)	low Vt	regular Vt
sky130_fd_sc_ms	Medium Speed	9T (3.33um)	low Vt	regular Vt
sky130_fd_sc_ls	Low Speed	9T (3.33um)	regular Vt	high Vt
sky130_fd_sc_hd	High Density	7.35T (2.72um)	regular Vt	high Vt
sky130_fd_sc_lp	Low Power	9T (3.33um)	regular Vt	high Vt

- These cells only provide five combinations out of dozens possible.
- All the columns in this table are design parameters that can be adjusted independently, meaning there are far more possibilities than the SkyWater cells provide.

Why would we want more?

- By creating standard cell with different design parameters, we can provide more options for the ASIC designer to fit all needs.
- For a design defined by long wires and high logic fan-out, taller cells would be a better fit than what is currently available.
- High-density cells are only offered in a single flavor: low-speed. More flavors possible allows more customization and fine-tuning!

What else?

- SkyWater standard cells do not have built-in substrate contacts, while ours do.
- Minimizes the body effect.
- Routing philosophy: we restrict inter-cell routing on high-resistance layers.
- Thicker power rails possible.
- All these small details add up and change the performance of the final product.

OSU Standard Cells and SoC Design Flows

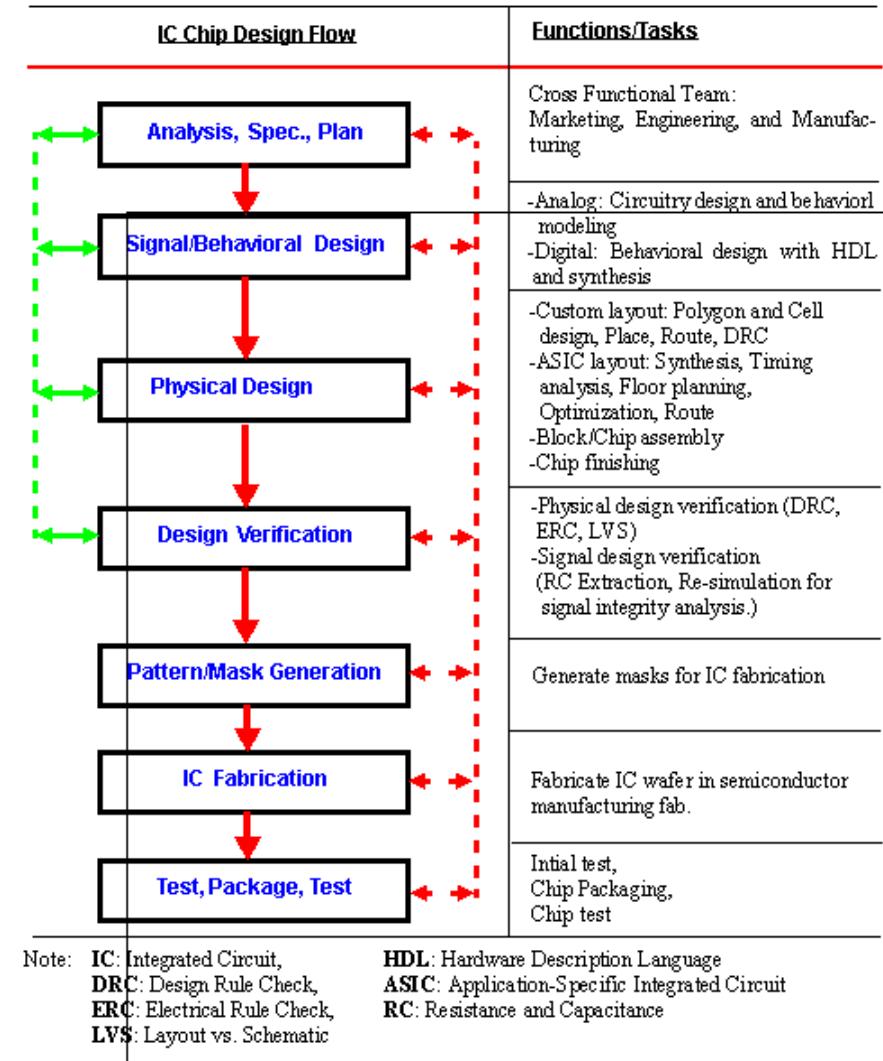
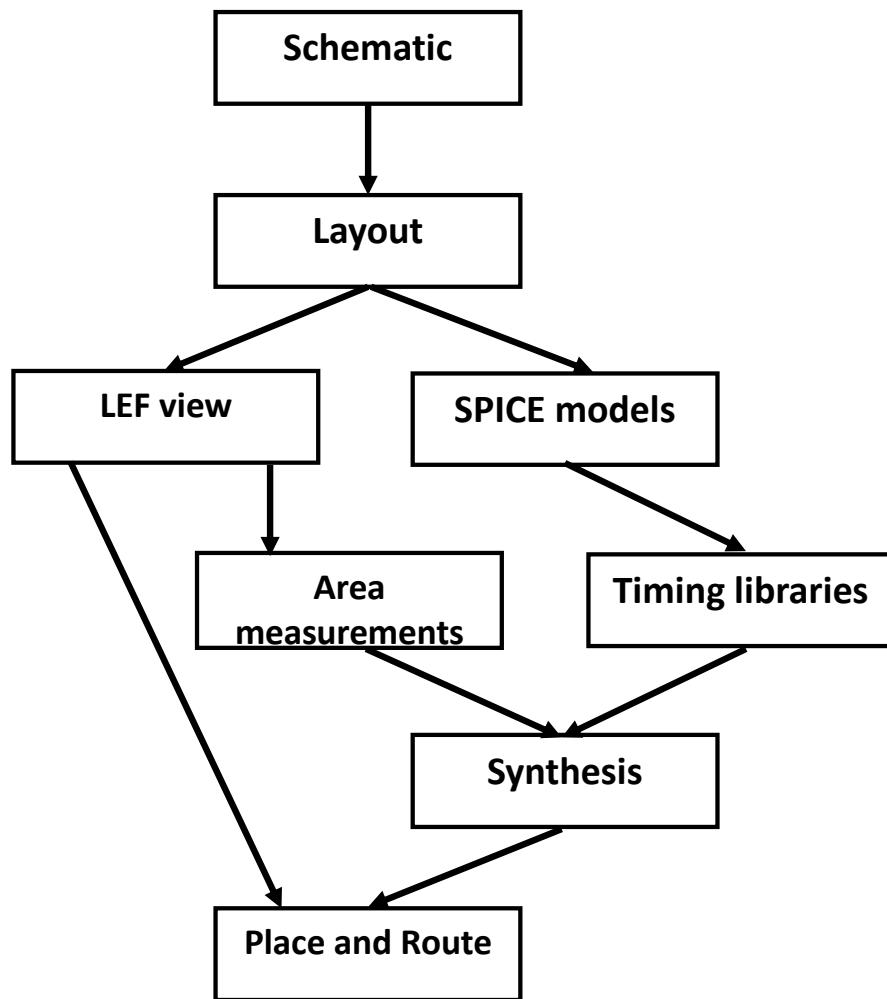
- Due to initial issues with modeling, we designed our base set cells around an 18T (6.66um) height.
- 62 cells currently in library, with 27 more cells temporarily removed.
 - We want to make sure all cells conform to the same design standards
- Our goal is to create the best cells we can through repeated iteration and refinements.
- Community feedback welcome!
 - All files and scripts provided for library so others can use and expand.
 - Design flows are provided to allow others to use cells with a SoC design in mind.



Currently-Planned OSU Cell Variants

Variant library		Cell height	MOSFET threshold	Legend:
sky130_osu_18T	_hs	18T (6.66um)	low Vt	done!
	_ms		regular Vt	
	_ls		high Vt	
sky130_osu_15T	_hs	15T (5.55um)	low Vt	done, pending characterization
	_ms		regular Vt	
	_ls		high Vt	
sky130_osu_12T	_hs	12T (4.44um)	low Vt	in progress
	_ms		regular Vt	
	_ls		high Vt	
sky130_osu_9T	_hs	9T (3.33um)	low Vt	
	_ms		regular Vt	
	_ls		high Vt	

System on Chip (SoC) Design Flow



Standard Cell Design Philosophy

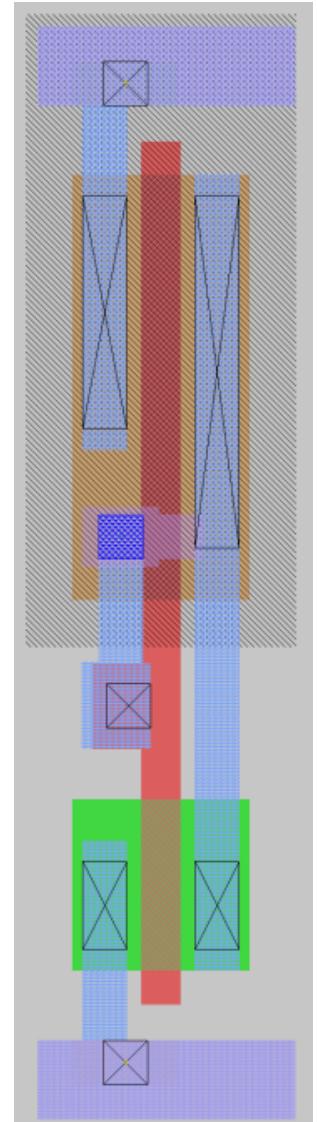
- Standard cells sit at the base of all good designs. Without good standard cells you cannot make a good chip!
- The main design goals in a standard cell kit are to minimize area and power consumption while maximizing speed.
- Each of these comes at the cost of the others: you must sacrifice some to meet the others.

Standard Cell Design Philosophy (Continued)

- Modern standard cell kits are commonly provided with multiple versions of each cell, some optimized for power while others for speed.
- Usually done by changing the threshold voltage of the cells
- These can be intermixed within a single design
- Makes it easy to trade power for speed within the scope of a single design
- Our main goal is providing the ability to implement SoC designs as well as provide files that others can use and hopefully contribute back to the project.

Layout

- For standard cell layout, we use Magic, an open-source tool actively maintained by Tim Edwards from eFabless.
- We prefer it over commercial tools for our research, even involving nodes all the way down to 14nm.
- <http://opencircuitdesign.com/magic/>



Layout (Continued)

- Tim Edwards is part of the 130nm Open PDK team and frequently updates Magic to meet the needs of his project.
- Magic was originally designed with SCMOS in mind, but can be used at any technology by editing a tech file.
- The Magic tech file for the 130nm Open PDK will be included as part of the general release, so anyone can start creating layouts from day one.



SPICE Models

- To obtain SPICE models we begin with our magic layout. Magic makes it to extract a baseline spice model, containing all devices and dimensions.
- We then take this baseline spice model along with the cell's GDS and perform parasitic extraction (PeX).
- PeX consists of accurate extraction of the resistors, capacitors, and parasitic devices present within a design.
- We currently use Calibre to perform our PeX.
- This gives us a much better model of how the cells will behave.

```
* File: INVX1.spice
* Created: Sun Sep 20 09:38:05 2020
* Program "Calibre xRC"
* Version "v2020.2_35.23"
*
.include "INVX1.pex.spice"
.subckt INVX1 GND VDD A Y
*
* Y Y
* A A
* VDD VDD
* GND GND
MM1000 N_Y_M1000_d N_A_M1000_g N_GND_M1000_s GND NSHORT L=0.15 W=1 AD=0.265
+ AS=0.265 PD=2.53 PS=2.53 NRD=0 NRS=0 M=1 R=6.66667 SA=75000.2 SB=75000.2
+ A=0.15 P=2.3 MULT=1
MM1001 N_Y_M1001_d N_A_M1001_g N_VDD_M1001_s N_VDD_M1001_b PSHORT L=0.15 W=3
+ AD=0.795 AS=0.795 PD=6.53 PS=6.53 NRD=0 NRS=0 M=1 R=20 SA=75000.2 SB=75000.2
+ A=0.45 P=6.3 MULT=1
*
.include "INVX1.pkl.spice"
*
.ends
```



SPICE Simulation

- SPICE can be used to accurately simulate our cells in a variety of condition.
- The SkyWater 130nm Open PDK has been hard at work over the last few weeks to release a full set of SPICE models for all devices that can be fabricated in this technology node.
- Compatible with open-source ngspice!



LEF View

- LEF/DEF is a globally-used format for representing design rules, abstract information about standard cells, and circuit layout.
- The format is entirely text-based and used by most open-source EDA tools.
- LEF (library exchange format) provides abstract information about cells to be used during place and route, such as pin locations, routing obstructions, and antenna restrictions.
- We extract LEF views from all our designs for easy use.

```
MACRO ADDFX1
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN ADDFX1 0 0 ;
  SIZE 7.04 BY 6.66 ;
  SYMMETRY X Y ;
  SITE 18T ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER met1 ;
      RECT 5.01 1.735 5.3 1.965 ;
      RECT 0.34 1.765 5.3 1.935 ;
      RECT 2.35 1.735 2.64 1.965 ;
      RECT 0.34 1.735 0.63 1.965 ;
    END
  END A
  PIN B
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER met1 ;
      RECT 4.12 2.475 4.41 2.705 ;
      RECT 0.34 2.51 4.41 2.675 ;
      RECT 4.06 2.505 4.41 2.675 ;
```



Timing Libraries

- The Liberty Timing Format (LIB) is a file format for providing timing models containing cell delays and transition times, setup and hold time requirements, logical cell function, and optionally area.
- The format is entirely text-based and used by most open-source EDA tools.
- All libraries are fully characterized and include scripts to help others in expanding the library, if needed
- We provide both CCS and ECSM liberty files as well as back-annotated VHDL and Verilog files.

Delay Information

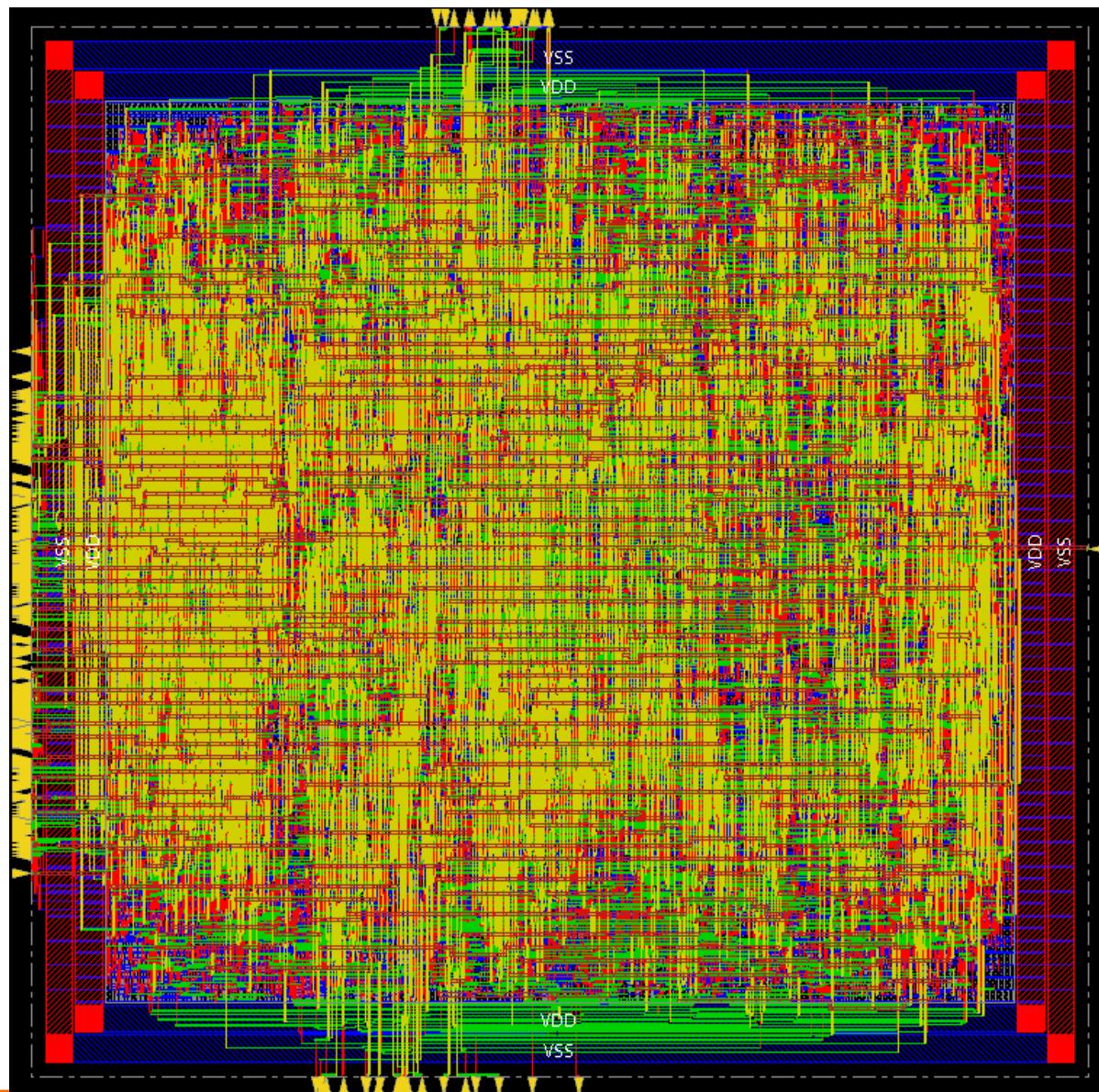
Delay(ns) to Y rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		First	Mid	Last
AND2X1	A->Y (RR)	0.07489	0.20503	0.65648
	B->Y (RR)	0.07985	0.20601	0.65841
AND2X2	A->Y (RR)	0.08542	0.20967	0.70273
	B->Y (RR)	0.09034	0.20929	0.69907
AND2X4	A->Y (RR)	0.11595	0.24205	0.79319
	B->Y (RR)	0.12084	0.24136	0.78209
AND2X6	A->Y (RR)	0.14558	0.27412	0.86364
	B->Y (RR)	0.15042	0.27399	0.84680
AND2X8	A->Y (RR)	0.17518	0.30612	0.91873
	B->Y (RR)	0.18007	0.30631	0.89836
AND2XL	A->Y (RR)	0.08460	0.22592	0.66372
	B->Y (RR)	0.08984	0.22668	0.66538

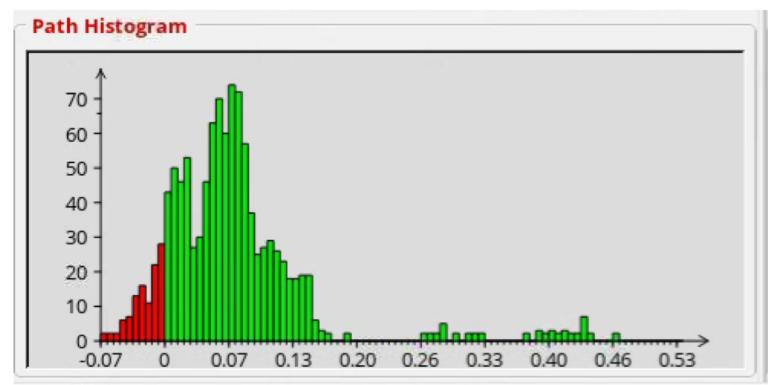
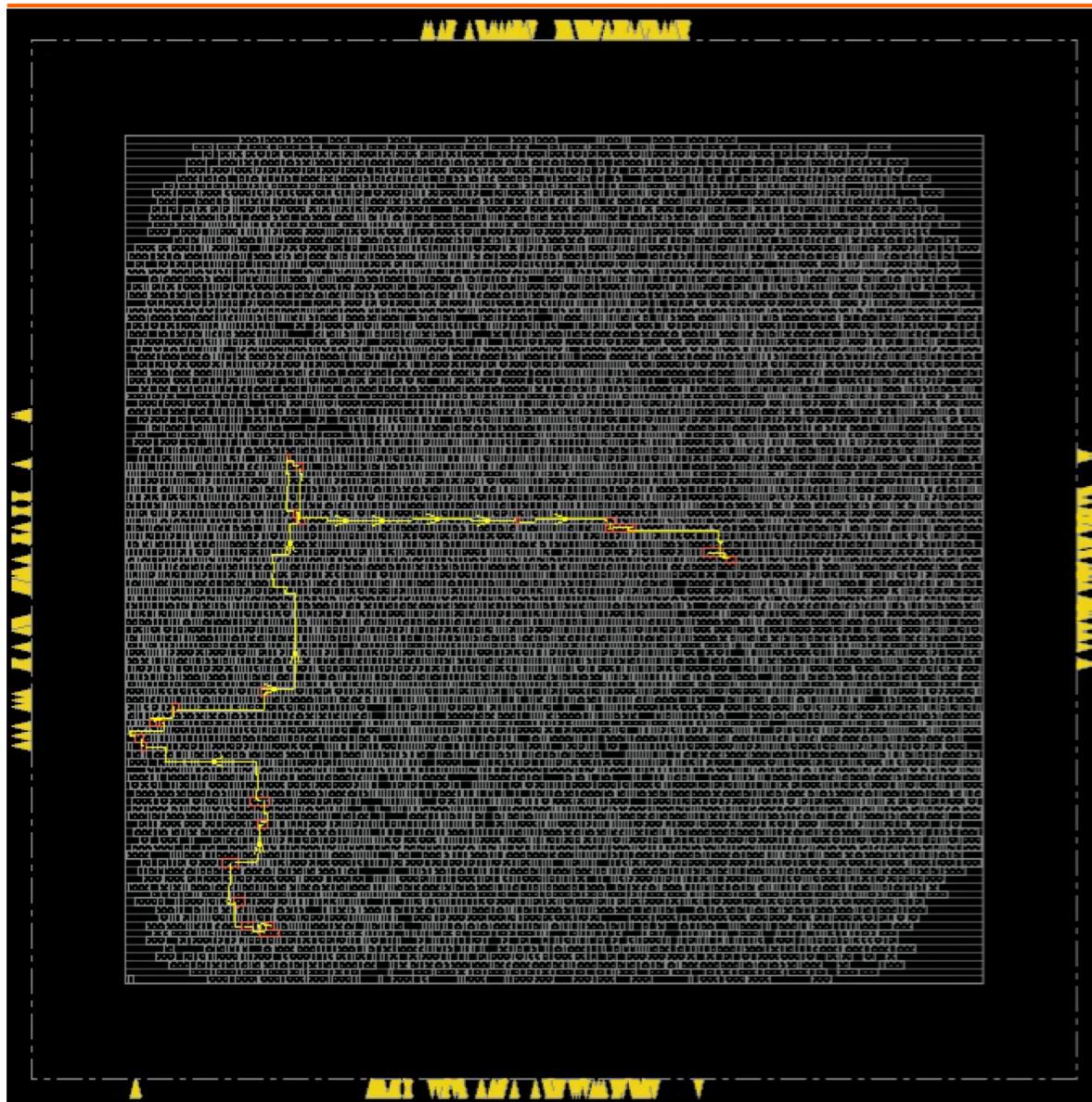
Synthesis and Place and Route

- Once cells are fully characterized, the best way to test them is by using them to implement an HDL design.
- Liberty timing files and LEF view provide only an abstract description of timing and physical layout, respectively.
- Cells behavior may change once implemented
- Synthesis is commonly used in literature to compare results across different designs
- Place-and-route results depend on a physical layout, so they are inherently more accurate but can also show greater variance with regards to initial parameters.

Place and Route Output Example



Place and Route Output Example (Continued)



OpenLANE Integration

- At present, we rely on commercial tools to perform synthesis and place-and-route.
- We are currently working on integrating OpenLANE, the eFabless open-source design flow, into our own flow.
 - Co-operation with OpenLANE has already led to improvements in our design.
 - We have been testing our cells through OpenLANE internally, but need to work towards making our file structure allow for seamless integration into OpenLANE.
 - We hope that further co-operation will lead to improvements for both of our projects!

Open-Source Flows

- In general, we are excited to completely switch over to open-source tools as they become available.
 - Not just OpenLANE, but any tools we are informed of.
- Magic has been a great tool for both education and research.
 - Easy to teach to students but versatile with more complex designs.
- We support open-source flows!

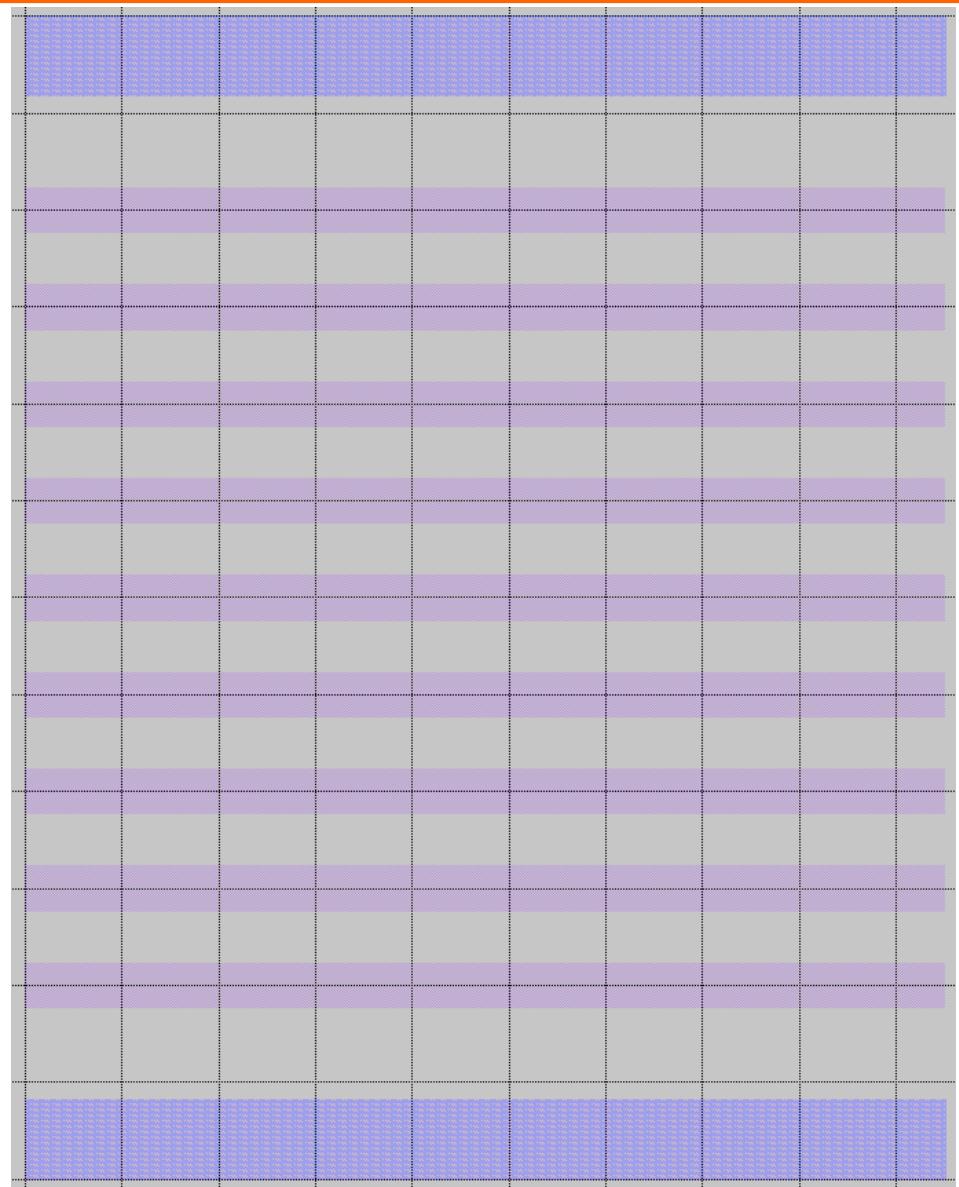


Standard Cell Tracks

- One key design choice for any library is the height of the cells.
 - Taller cells have transistors with larger widths, resulting in higher speeds.
 - Taller cells also have more room available for routing wires, meaning lowering congestion.
- Cell height is measured in terms of routing tracks of the lowest non-interconnect metal layer.
 - A track is the smallest section of space that can accommodate a drawn wire.
 - Typically defined in terms of the width and spacing design rules for the respective layer.
- Typically, 9-track (9T) cells are standard.
 - 12-track (12T) cells are often provided for high-speed designs.
 - Smaller cells, such as 7T are used for ultra-high density designs.

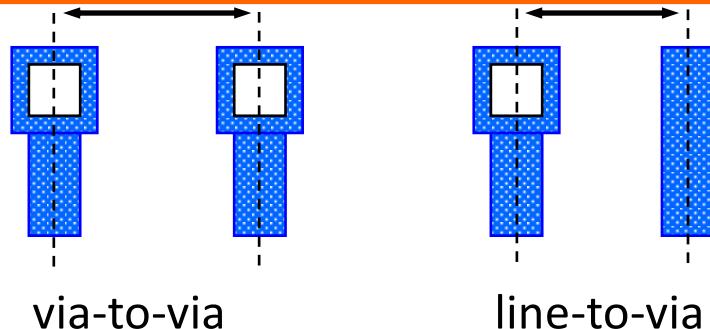
Standard Cell Tracks (Continued)

- An example of a 12-track setup can be seen to the right.
- Note that although being 12 tracks tall, the cell can only accommodate 9 routed wires
- Power rails take space on these tracks as well.
- Cells of different heights provide a simple solution for trading off speed vs area.
- But they cannot typically be mixed within the same design!

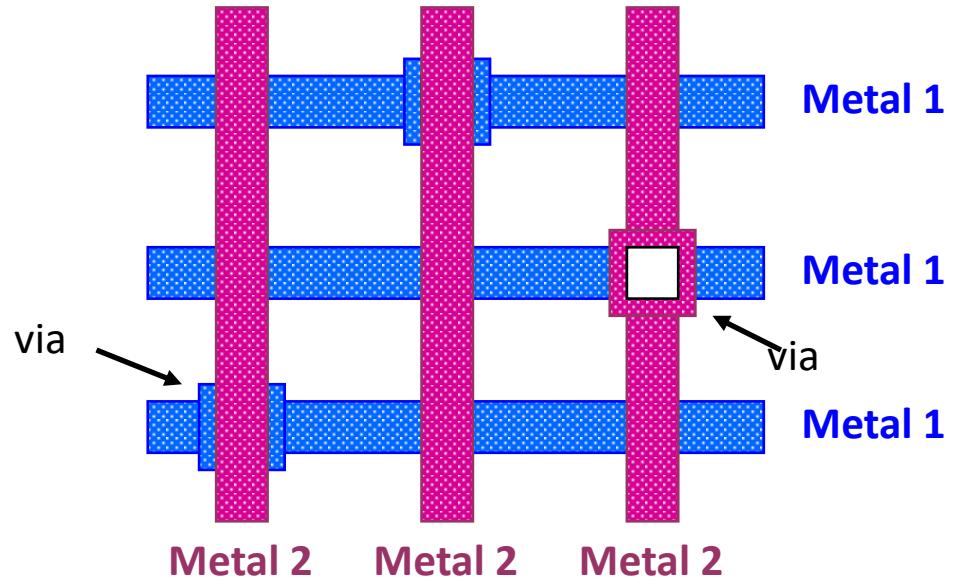


Track Pitch and Direction

- The pitch at which wires are spaced defines the size of a routing track.
- Can be defined either via-to-via or line-to-via.
- To simplify Place and Route, metal layers are used in alternating directions.
 - Odd layers for horizontal routing and even layers for vertical routing (HVH).
 - On more advanced tech nodes, it is common to see both of the first two metal layers run horizontally.

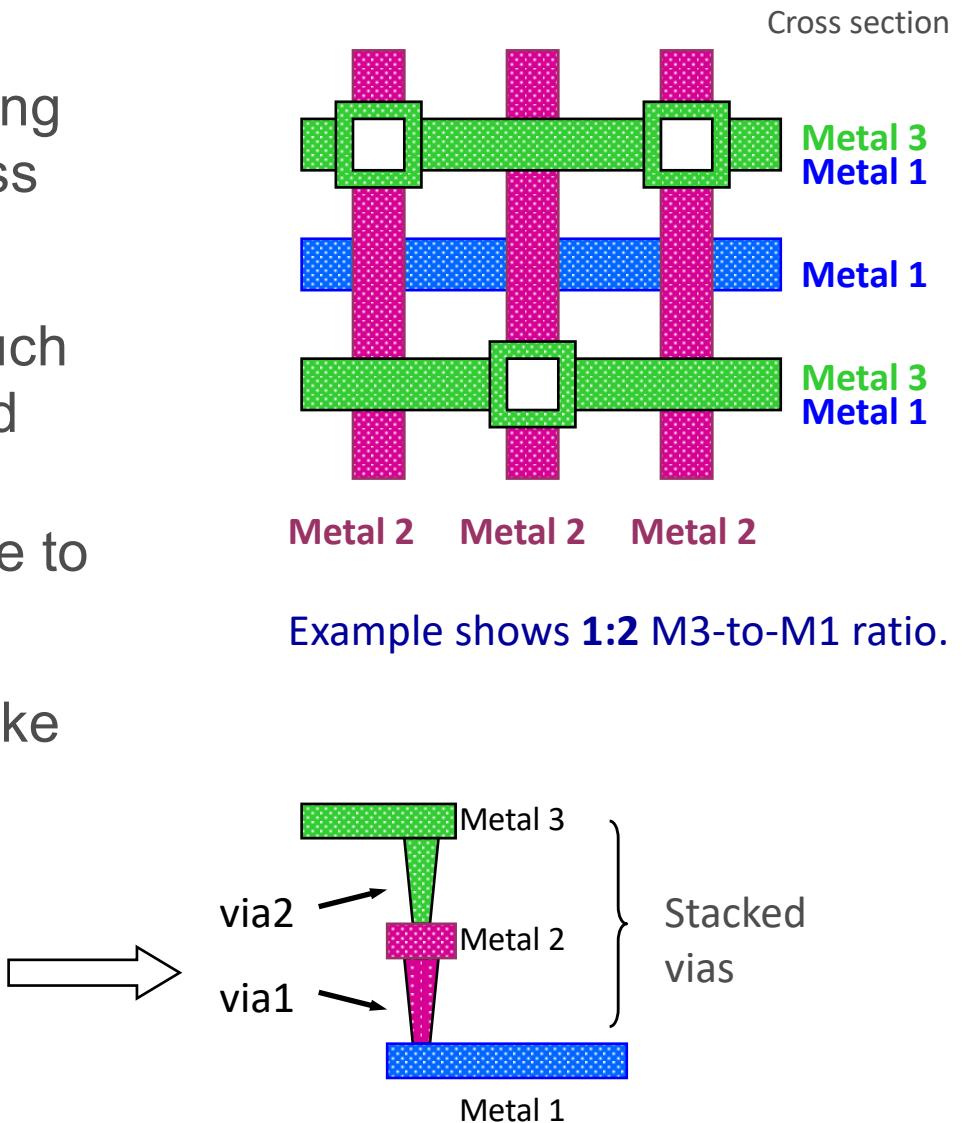


Line-to-via because it is the minimum pitch in which you can place a via next to a route track



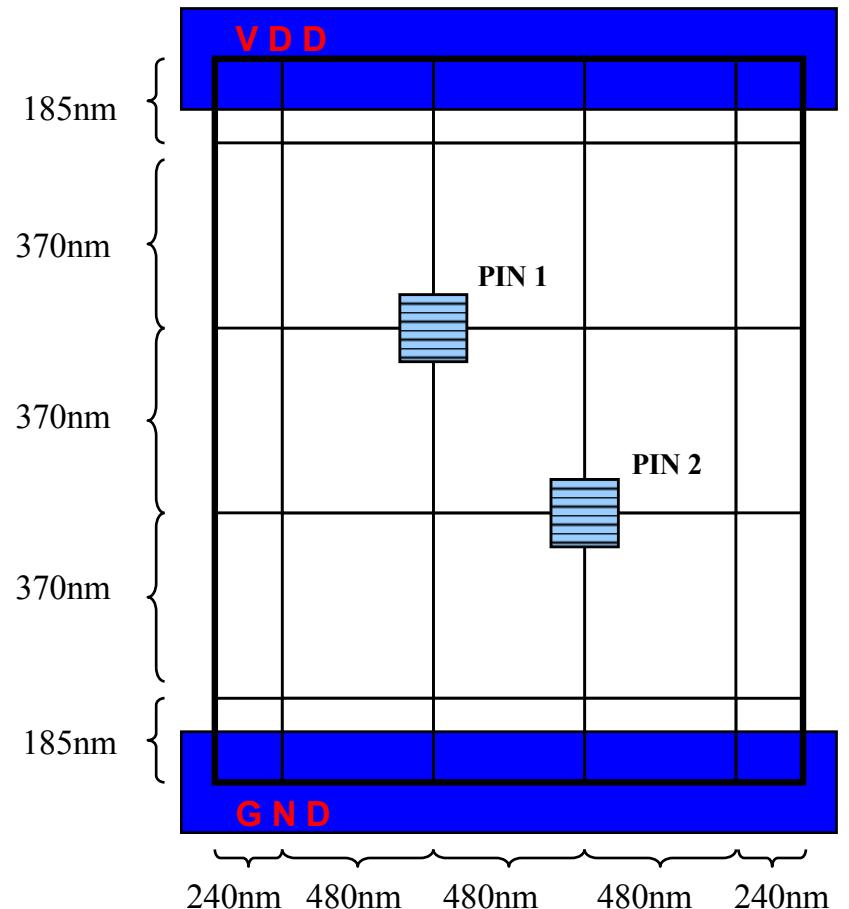
Routing Grid Definitions

- Different layers with the same routing direction will have different thickness and spacing: different pitch.
- If M3:M1 have a track pitch ratio such as 11:8 both horizontal tracks would be on top of each other seldomly making it difficult or even impossible to create an M3-to-M1 contact.
- Importance of using simple ratios like 1:1, 1:2, 2:3, 3:4 between adjacent same direction routing tracks.
- It is desirable for the tracks to be aligned to allow stacked vias.



Layout Creation and Routing Grid

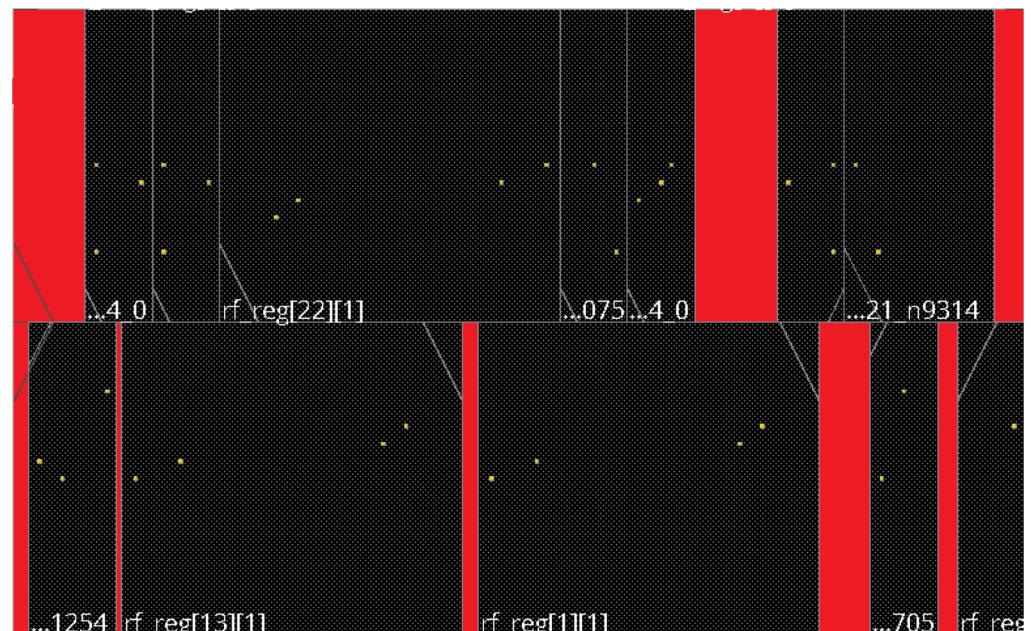
- Pins should placed on the grid (reduce routing efforts).
- Staggered if possible (reachable by both horizontal and vertical layers).
- Power signals routed through abutment (increase density).



Power rails designed to allow abutment.

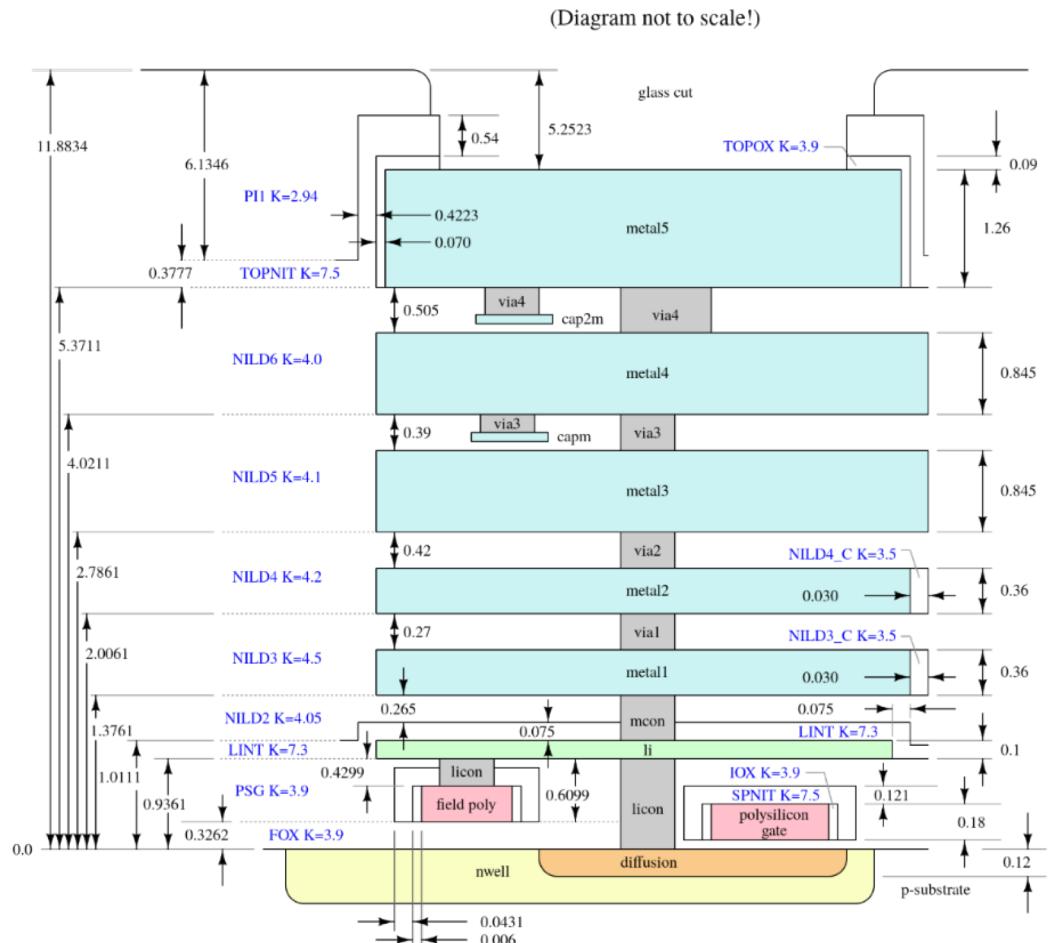
Standard Cell Dimensions

- Standard cell heights must be the same across the entire library.
- Gaps between cells are not allowed and must be filled with “filler” cells.
- All standard cells widths must be integer multiples of our smallest filler cells.
- The smaller this common divisor is, the less wasted space.



Skywater 130nm Metal Stack

- 5 metal layers, plus 1 local interconnect.
- Metal layers are aluminum
- Local Interconnect is TiN
- As can be seen, the li layer is much thinner than metal layers.
- Local interconnect has 97.6x more resistance per square area than m1.
- li1 sits between the FEOL layers and the metal layers, so we must use it.
- If we can use it well, we free up most of m1 for routing.

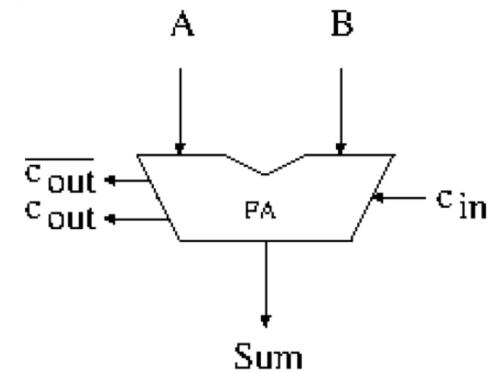
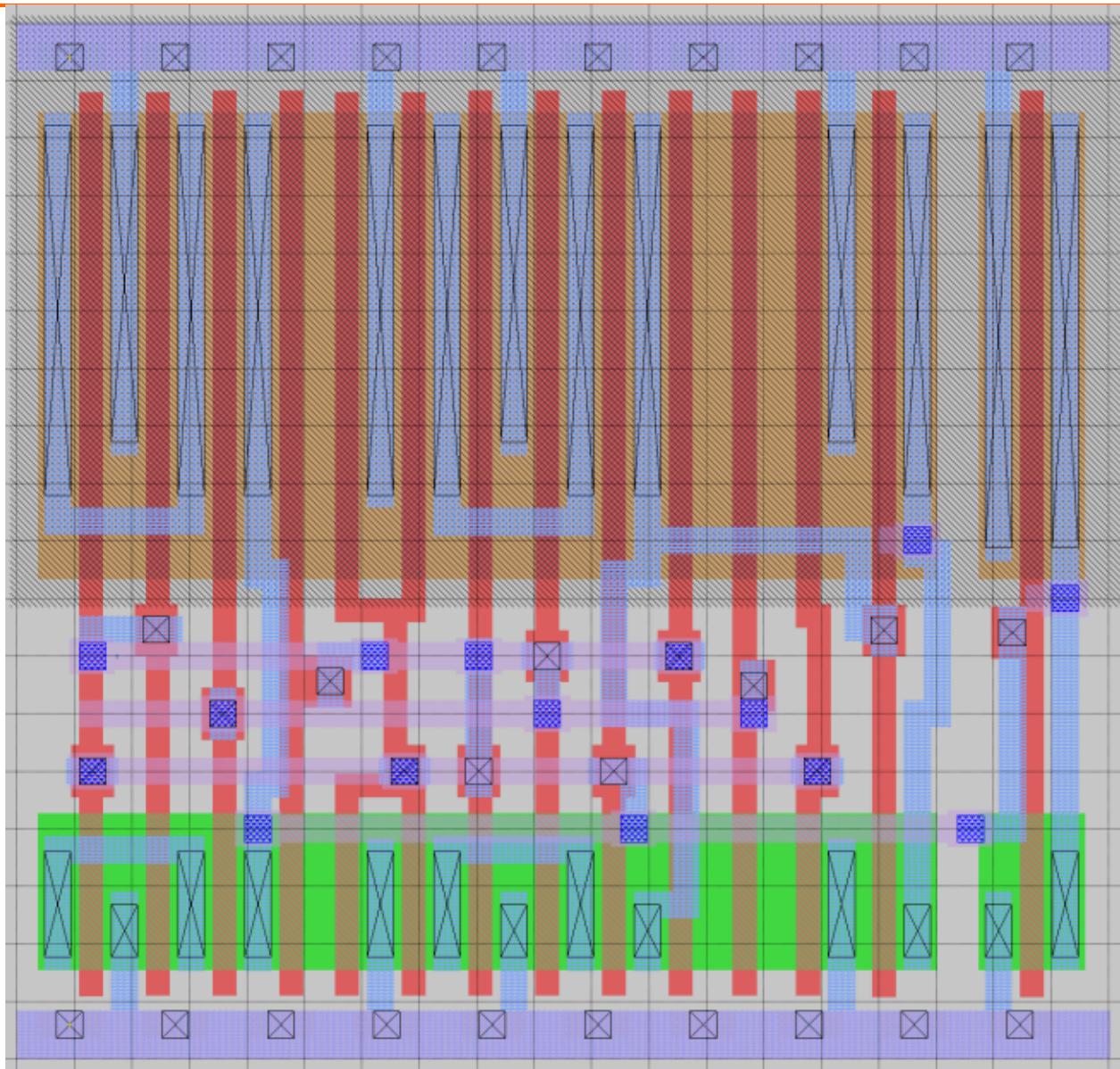


Dealing with Local Interconnect

- The design rule manual suggest that local interconnect wires should be restricted to an aspect ratio of 10:1.
- As mentioned previously, this TiN layer has much more resistivity than the aluminum layers.
- The decision was made to provide all cell in/out pins on metal1 and prevent routing on li1.
- We must take care that our in/out pins do not block metal1 routing tracks

```
# NOTE:  
# The use of li1 as a routing layer is commented  
# out and replaced with a definition of li1 as a  
# non-routing layer. This is done to ensure good  
# results regardless of tool used.  
#  
# If li1 is enabled as a routing layer take note  
# of its resistance compared to that of metall1.  
  
LAYER li1  
    TYPE MASTERSLICE ;  
END li1  
  
#LAYER li1  
#    TYPE ROUTING ;  
#    DIRECTION VERTICAL ;
```

Pins Attached to metal1 Routing Tracks

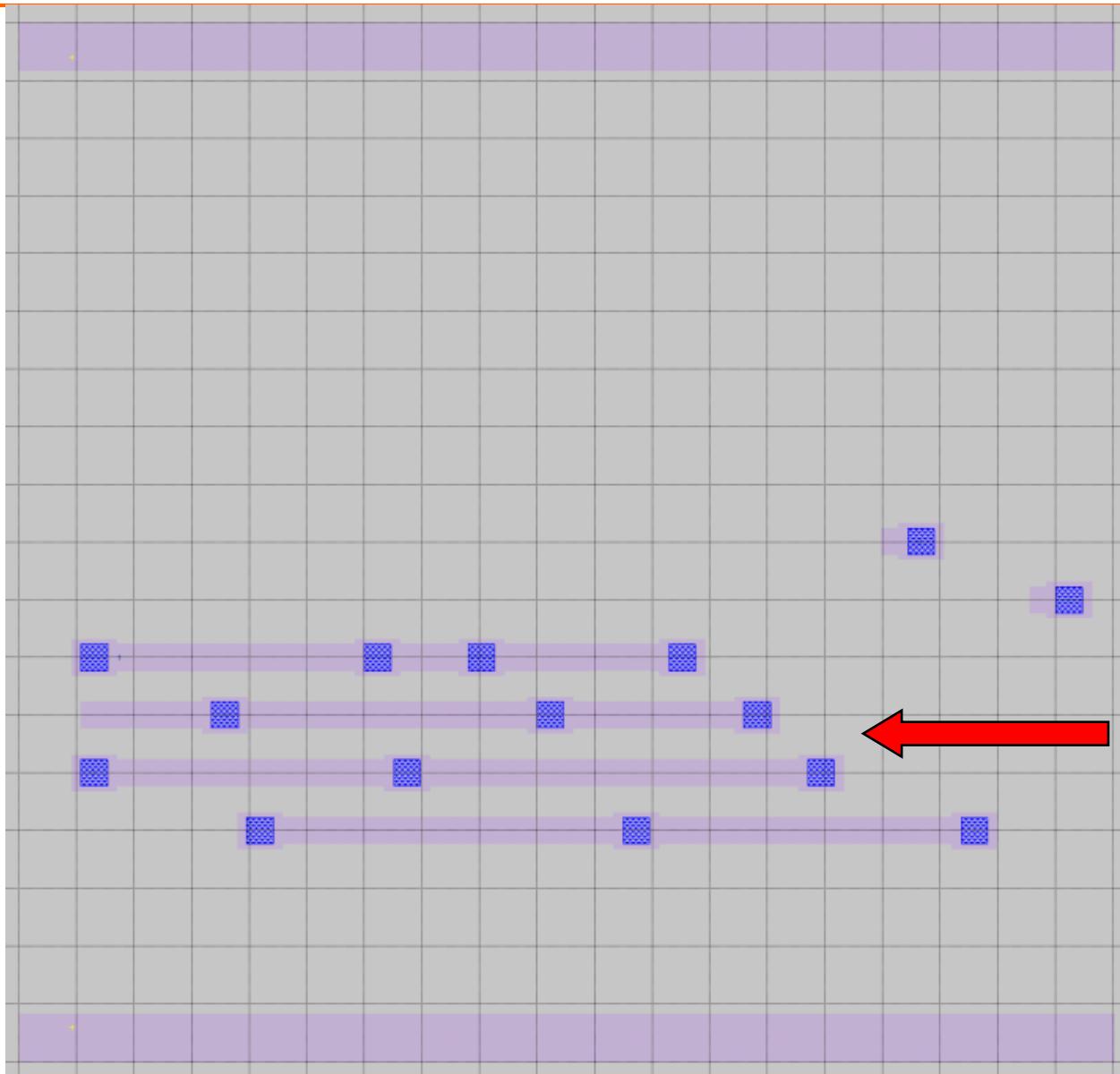


There are three inputs
and three outputs

That means six total
pins, each on a
separate metal1 track

Next we will have a
clearer view!

Pins Attached to metal1 Routing Tracks (Continued)

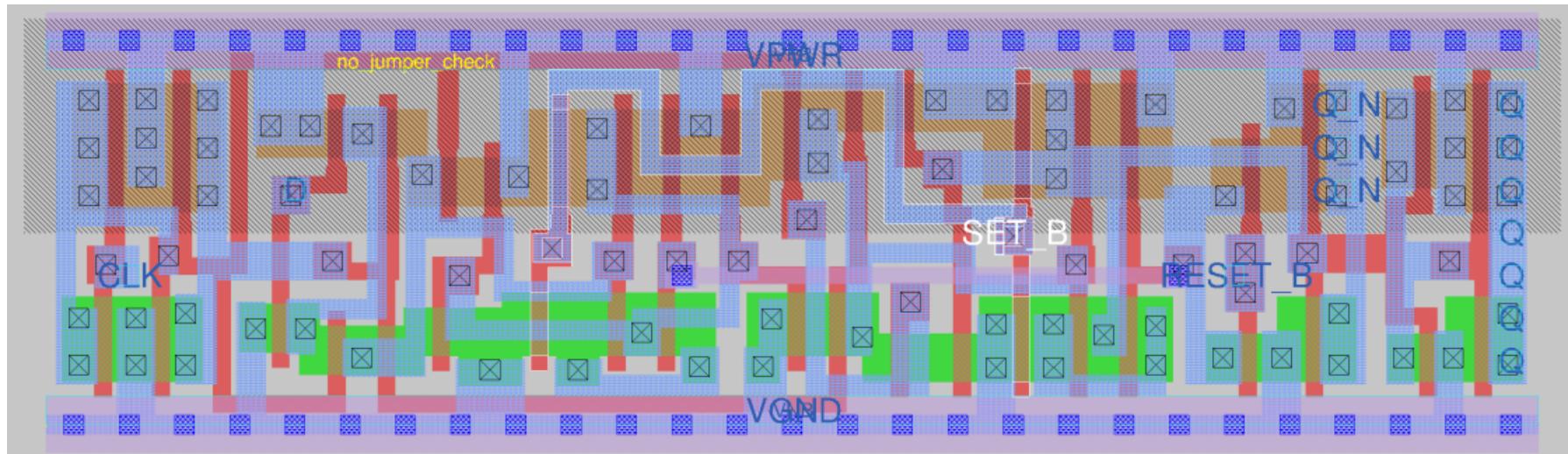


A better look at just the m1 routing tracks.

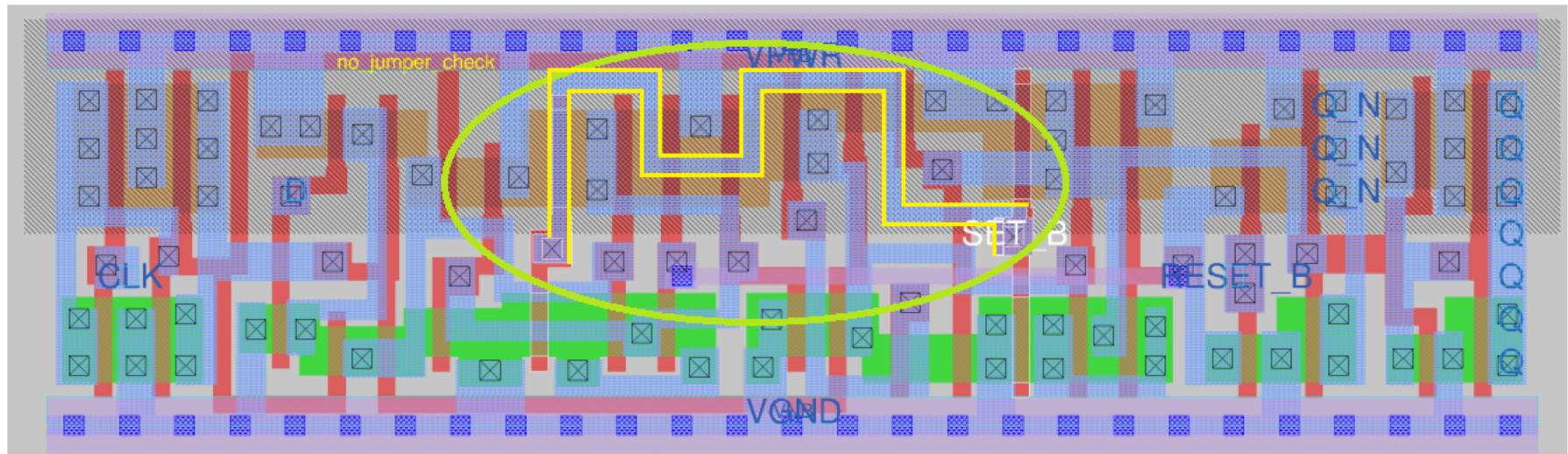
Since the pins block a routing track anyway, we can use metal1 inside our cells!

We don't have to use high-resistance li1 here.

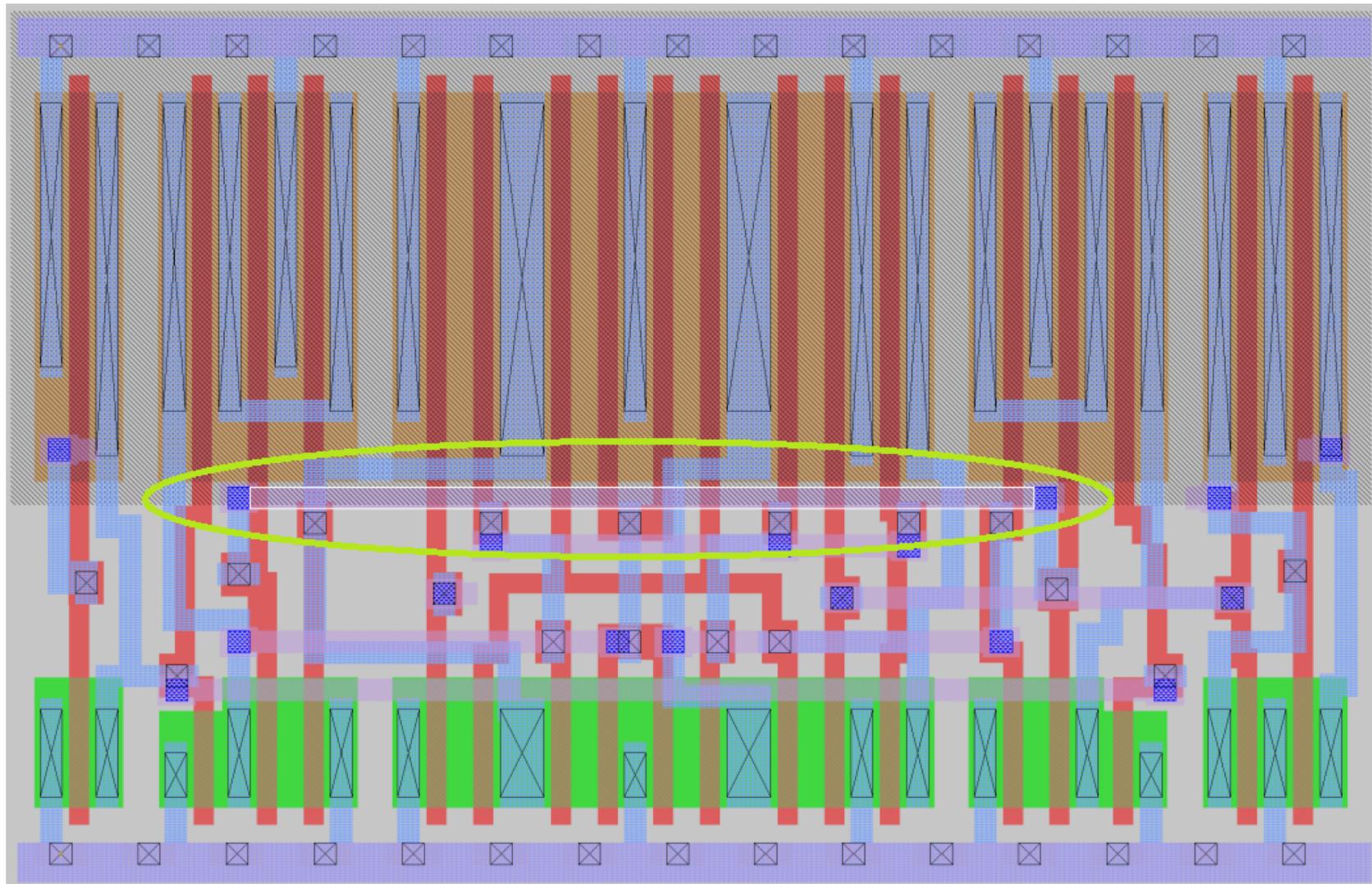
sky130_fd_sc_hs DFFSR



One of the inputs signal is routed on li1. This is a long, high-resistance wire!



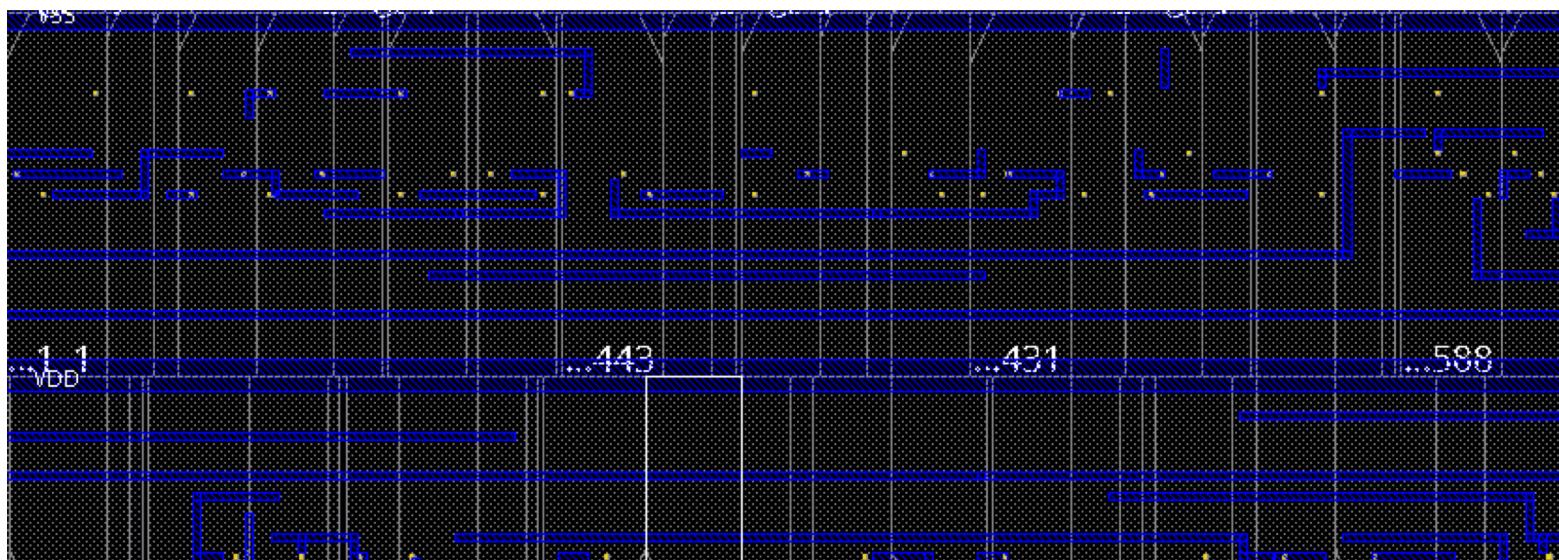
OSU DFFSR



The same input is routed on metal1. 97.6x less resistance than li1!

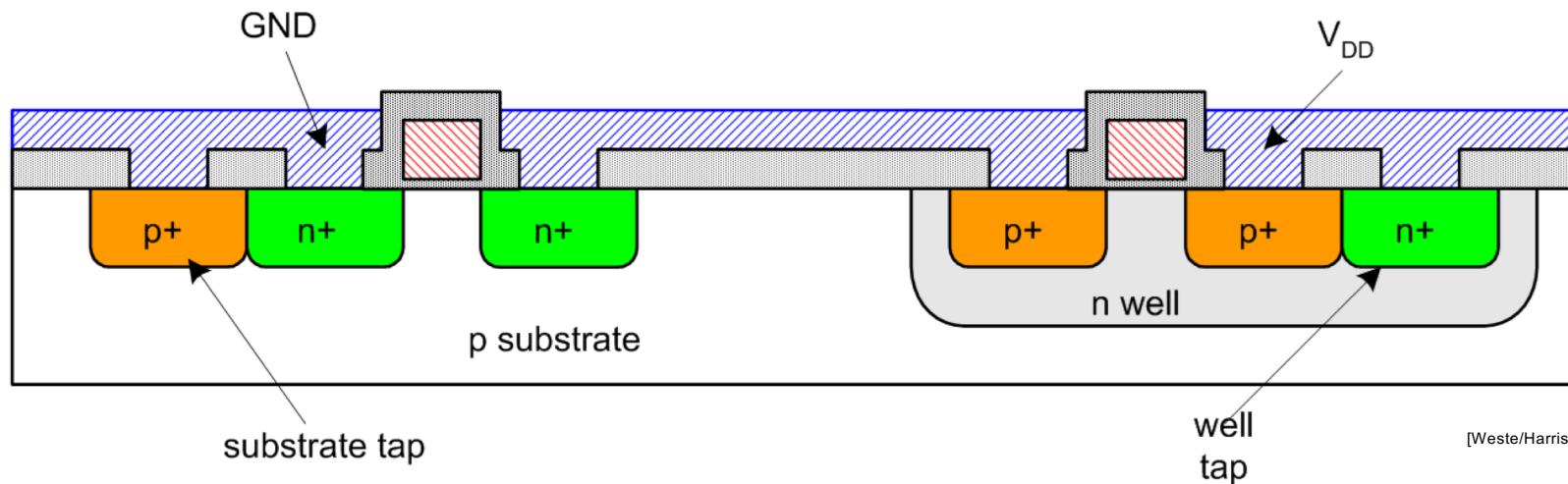
Metal1 Inter-Cell Routing

- To allow for efficient inter-cell routing, metal1 usage must be kept to a minimum within cells.
- We complement this effort in our cells by keeping all of our pins limited to the same six metal1 tracks throughout our library.
 - This guarantees that all other tracks are available for top-level routing.
 - Less routing congestion.
 - An example of the tools able to draw long, straight wires, shown here:



Well and Substrate Taps

- The pre-existing SkyWater standard cells do not have well and substrate taps built into their power rails.
- Instead they offer specialized tap cells that are meant to be placed alongside the standard cells in a design.
- Our cells offer thicker power rails with built-in well and substrate taps.
- This provides better connectivity with the body of the transistors, minimizing the impact of the body effect.



OSU Standard Cell Kit

Cell Name	Description
ADDFXL	3-2 counters
ADDFX1	
ADDHXL	2-2 counters
ADDHX1	
AOI21XL	AND-OR-INVERT gate
OAI21XL	OR-AND-INVERT gate
NAND2XL	NAND cells
NAND2X1	
NOR2XL	NOR cells
NOR2X1	
MUX21XL	2-1 muxes
MUX21X1	
TBUFIXL	Active-high inverting tri-state buffer
TBUFIX1	
TNBUFIXL	Active-low inverting tri-state buffer
TNBUFIX1	

Cell Name	Description
INVXL	Inverters
INVX1	
INVX2	
INVX4	
INVX6	
INVX8	

Cell Name	Description
BUFXL	Buffers
BUFX1	
BUFX2	
BUFX4	
BUFX6	
BUFX8	

OSU Standard Cell Kit (Continued)

Cell Name	Description
AND2XL	AND gates
AND2X1	
AND2X2	
AND2X4	
AND2X6	
AND2X8	

Cell Name	Description
OR2XL	OR gates
OR2X1	
OR2X2	
OR2X4	
OR2X6	
OR2X8	

Cell Name	Description
DFFXL	Positive edge D flip-flop
DFFX1	
DFFNXL	Negative edge D flip-flop
DFFNX1	
DFFSXL	D flip-flop with asynchronous active-low set
DFFSX1	
DFFRXL	D flip-flop with asynchronous active-low reset
DFFRX1	
DFFSRXL	D flip-flop with asynchronous active-low set and reset
DFFSRX1	

Cell Name	Description
ANT	Filler cells
ANTFILL	
FILLX1	
FILLX2	
FILLX4	
FILLX8	
FILLX16	
FILLX32	
TIEHI	Used to tie a net off to VDD through a FET
TIELO	Used to tie a net off to GND through a FET
DECAPXL	Decoupling capacitor
DECAPX1	

OSU Standard Cell Kit Information

- 62 cells currently in the library and expanding daily.
- Currently, we only have devices with standard threshold voltage (Vt).
- Cells were originally designed around 18-track (6.66um).
- Greatest common divisor of all cell widths is 0.11um (smallest filler cell).
- Cell pins exclusively on metal1, allowing us to forbid routing on li1.
- Well and substrate taps included in every cell.
- 0.61um power rails (3.6x minimum width) on li1.
 - Doubled by 0.61um power rails (4.4x minimum width) on metal1.

Current Status of Library

- Our base cells and flow has been published at
 - https://foss-eda-tools.googlesource.com/skywater-pdk/libs/sky130_osu_sc/
- Our 18-track cell set is published and fully open with all scripts, design flow and examples.
- We are currently running more characterization to provide additional corners.

Current Status of Library (Continued)

- Our 15-track and 12-track cell sets have been laid out and are currently undergoing characterization and final testing.
- Using the resources currently available to us, full characterization of a library takes 150 hours of unsupervised tool run-time and must be done sequentially
- They will be published under:
 - <https://foss-eda-tools.googlesource.com/skywater-pdk/libs>

Future goals

- Expanding upon the cell selection.
 - 27 cells have been temporarily removed to bring them up to the same standards as the rest of the cell-set
 - Designing new and improved cells
- Creating versions of the library utilizing both low-Vt and high-Vt.
 - low-Vt would provide high-speed high-power cells
 - high-Vt would provide low-speed low-power cells
- Experimenting with line-to-via track pitch, as opposed to via-to-via.
 - Track size can be reduced by an estimated 20%
- Also, creation of I/O pads for bond pads along with different output current strengths.
- Additional examples and design flow scripts

Pre-existing SkyWater Standard Cell Kits

- Several versions: high-density, high-voltage, high-speed, medium-speed, low-speed, low-power.
 - Most sets consist of roughly 150 cells.
 - Devices use not just standard Vt devices, but also low-Vt and high-Vt.
- Cells are mainly designed around 9-track (3.33um) height.
 - Greatest common divisor of all cell widths is 0.11um (smallest filler cell).
 - Cell pins on either metal1 or li1.
- Well and substrate cells must be placed separately.
- 0.17um power rails (1x minimum width) on li1.
 - Doubled by 0.49um power rails (3.5x minimum width) on metal1.

Comparison between OSU and SkyWater Cells

- Cells were compared by implementing a RISC-V single-cycle processor's datapath and controller.
- Synthesis was performed using Synopsys Design Compiler with a target clock period of 2ns.
- Place-and-route was performed using Cadence Innovus with a varied target clock period.
 - The target period for each place-and-route run was chosen by performing a binary search between 1x and 1.5x the passing period out of synthesis.
 - Roughly 6 iterations were necessary for each cell library.
 - Methodology was consistent for each cell library.

Comparison Results



Single-cycle RV32i design

Standard cell library	FET length [um]	Cell height	MOSFET threshold	
			nfet	pfet
sky130_osu_18T_hs	0.15	18T (6.66um)	low Vt	regular Vt
sky130_osu_18T_ms	0.15	18T (6.66um)	regular Vt	regular Vt
sky130_fd_sc_hs	0.15	9T (3.33um)	low Vt	regular Vt
sky130_fd_sc_ms	0.18	9T (3.33um)	low Vt	regular Vt
sky130_fd_sc_ls	0.15	9T (3.33um)	regular Vt	high Vt
sky130_fd_sc_hd	0.15	7.35T (2.72um)	regular Vt	high Vt

Comparison Results (Continued)



Single-cycle RV32i design

Standard cell library	Synthesis			Place-and-route		
	Frequency [MHz]	Area [um^2]	PDP [pJ]	Frequency [MHz]	Area [um^2]	PDP [pJ]
sky130_osu_18T_hs	398	155,774	33.8	327	197,744	239.1
sky130_osu_18T_ms	364	155,243	34.6	285	166,639	170.2
sky130_fd_sc_hs	431	87,560	65.8	308	102,119	163.7
sky130_fd_sc_ms	372	87,931	65.8	234	102,079	160.0
sky130_fd_sc_ls	322	88,663	62.2	202	108,555	139.4
sky130_fd_sc_hd	360	68,490	48.2	244	83,057	109.2

Results Discussion

- Our high-speed cells are best compared to the SkyWater cells, and our medium-speed cells to the SkyWater medium-speed cells
- Our main advantages are the higher drive strength of our cells and our ban on using `li1` for inter-cell routing.
 - Both of these factors lower the impact of wire delay.
 - This can be best seen by the fact that our cells have better performance than the Skywater cells post-synthesis.
- Although our 18T ms cells are twice as tall as the SkyWater 9T ms cells, our total area was only 63% larger at the end of P&R.
 - This makes us believe our 9T cells can achieve lower total cell area than `sky130_fd_sc_ms`.
- Our 18T medium-speed cells are already competitive with the SkyWater 9T medium-speed cells
 - This makes us excited to finish characterizing and testing our own 9T cells!

Results Discussion (Continued)

- The sky130_osu_18T_hs library is still a prototype, but already faster than the sky130_fd_sc_hs library.
- As we finalize it, we hope to lower its area usage to the same level as that of sky130_osu_18T_ms.
- We believe the power estimates obtained from place-and-route to be close representatives of the cells' behavior.
- The power consumption of our shorter cells (9T, 12T) will more closely align with that of the SkyWater standard cells.

Conclusion

- The git repository containing our source files and full flow is published at the following URL:
 - https://foss-eda-tools.googlesource.com/skywater-pdk/libs/sky130_osu_sc/
- A complete standard-cell library and System on Chip design flow that helps the community with open-source hardware.
- All scripts and files are included in the repository.
- All are welcome to help this initiative or ask questions on the slack channel or via Email.

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