

Multivibrator Circuits

Bistable multivibrators

Multivibrators

Circuits characterized by the existence of some well defined states, amongst which take place fast transitions, called switching processes. A switching process is a fast change in value of a current or a voltage, the fast process implying the existence of positive reaction loops, or negative resistances. The switching can be triggered from outside, by means of command signals, or from inside, by slow charge accumulation and the reaching of a critical state by certain electrical quantities in the circuit.

Circuits have two, well defined states, which can be either stable or unstable. A **stable state** is a state, in which the circuit, in absence of a driving signal, can remain for an unlimited period of time.

The circuit can remain in an **unstable state** only for a limited period of time, after which, in the absence of any exterior command signals, it switches into the other state.

The multivibrator circuits can be grouped, according to their number of stable (steady) states, into:

- **flip-flops** (bistable circuits) with both states being stable
- **monostable circuits**, having a stable and an unstable state
- **astable circuits**, with both states being unstable

Flip-flop circuits

The main feature of the flip-flop circuits is the existence of two stable states, in which the circuit may remain for a long time. The switching from one state to the other is triggered by command signals

Flip flop: an example for a **sequential circuit** (a circuit with outputs that present logical values depending on a certain sequence of signals, that have previously existed in the circuit). Because of this behavior, sequential circuits have the capability of storing information (memories).

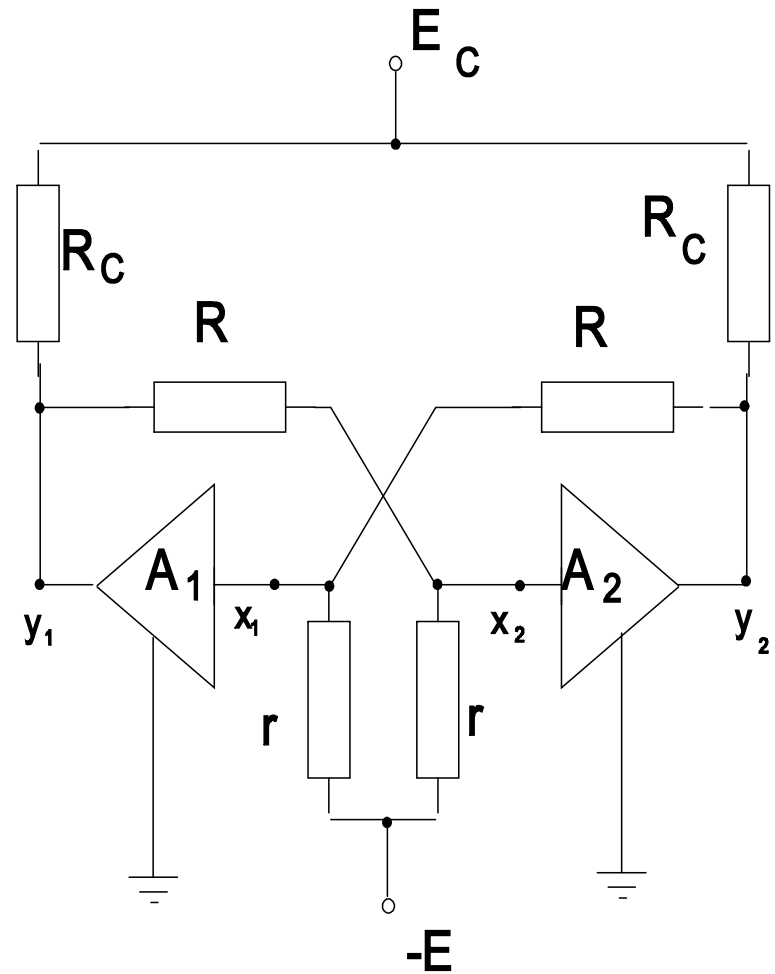
Unlike sequential circuits, **combinational circuits**, consisting of logical gates, have outputs, which depend only on the current inputs

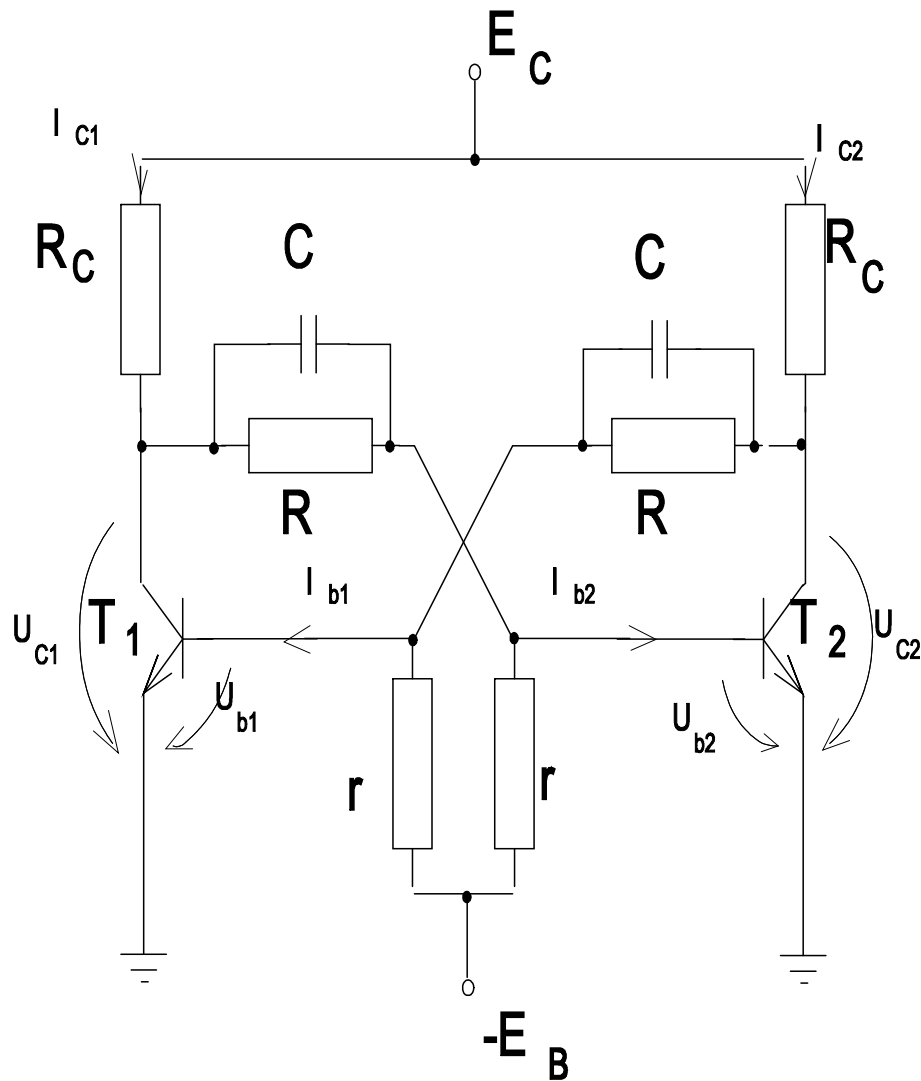
Flip-flop circuits may be classified into **symmetrical** and **non-symmetrical**

Symmetrical Flip-flop Circuits With Discrete Components

Basic layout presented at right

A_1 and A_2 are two amplifiers connected in a positive reaction loop, through the voltage divider made out of the resistances R and r





Design with discrete components

Amplifying stages made out of the transistors T_1 and T_2

Connected together through the positive reaction represented by the voltage dividers R and r

A part of the collector-emitter voltage of one transistor is transmitted into the base of the other transistor

Circuit operation:

If current I_{C1} experiences a small rise, this leads to the decrease of the voltage drop U_{C1} , which is transmitted through the voltage divider R-r into the base of T_2 transistor. The decrease in the voltage drop U_{B2} will be amplified and inverted by the transistor, so the voltage drop U_{C2} will increase, and this increase will be transmitted in the base of the T_1 transistor, through the R-r voltage divider. Because of that, I_{C1} will increase even more.

As a consequence a switching process takes place, which develops like an avalanche: the I_{C1} current increases and the I_{C2} decreases, until T_1 becomes saturated, and T_2 off

State is stable, because the positive reaction loop is interrupted, due to the Blocking state of transistor T_2

Two stable states:

1. T_1 – conducting (saturated), T_2 - blocked
2. T_1 - blocked, T_2 - conducting (saturated).

In order for a bistable to work in this manner elements have to be sized, so that they satisfy the following conditions:

- 1). when T_1 is blocked, T_2 has to be saturated
 - 2). when T_1 is saturated, T_2 has to be blocked
 - 3). when T_1 and T_2 are in forward active state, the amplification on the positive reaction loop has to be greater than one.
- Because of symmetry of the circuit, the conditions 1) and 2) are equivalent. Moreover, it can be proven, that, if conditions 1) and 2) are satisfied, then condition 3) will also be satisfied. Finally condition 1) is a necessary and sufficient condition for the correct functioning of the circuit

Condition 1) requires that the following inequalities be true:

$$U_{B1} \leq 0$$
$$I_{B2} \geq I_{Bs}, \text{ where } I_{Bs} = \frac{I_{Cs}}{\beta} \approx \frac{E_C}{R_C}$$

Blocking condition for T1 gives relations: $U_{B1} \leq 0, I_{C0} = \frac{U_{B1} + E_B}{r} - \frac{U_{B1}}{R}$

$$U_{B1} = I_{C0} \frac{R \cdot r}{R + r} - E_B \frac{R}{R + r} \quad r \leq \frac{E_B}{I_{C0}}$$

For any temperature conditions, take: $r \leq \frac{E_B}{I_{C0max}}$

The saturation condition for the T₂ transistor:

$$I_{B2} \approx \frac{E_C}{R + R_C} - \frac{E_B}{r} \quad R \leq \left(\frac{\beta}{1 + \beta \frac{E_B}{E_C} \cdot \frac{R_C}{r}} - 1 \right) \cdot R_C$$

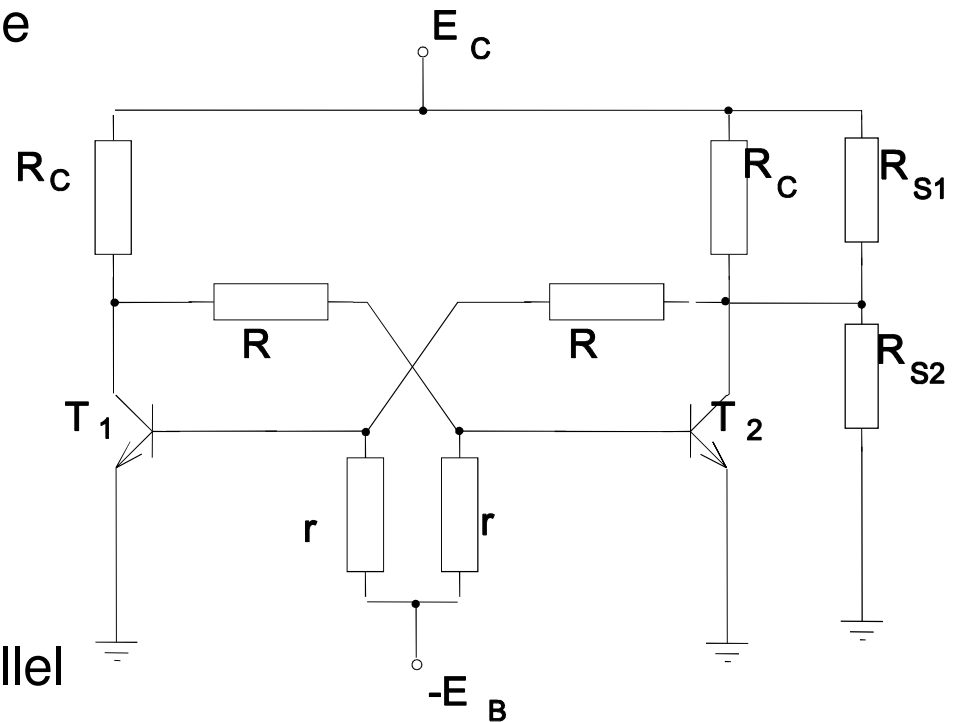
For worst case:

$$R \leq \left(\frac{\beta_{min}}{1 + \beta_{min} \frac{E_B R_C}{E_C r}} - 1 \right) \cdot R_C \quad \text{or} \quad R \leq \left(\frac{\beta_{min}}{1 + \beta_{min} \frac{I_{C0max}}{I_{Cs}}} - 1 \right) \cdot R_C$$

The Influence Of A Load Resistance On The States Stability

Connection of a load resistance at the output of a bistable may have a negative influence on the stability of the states, because it modifies the equivalent resistance of the collector circuit, affecting the distribution of voltages

Load resistance may be connected at one of the outputs, in parallel with the resistor R_C (case R_{s1}), or in parallel with the transistor T_2 (case R_{s2})



If load resistance R_{s1} is connected, equivalent collector resistance becomes:

$$R'_C = R_C || R_{s1} = \frac{R_C \cdot R_{s1}}{R_C + R_{s1}}$$

$R'_C < R_C$, so collector current is higher, driving base current must be higher

Greater base current I_{B2} is needed, so the value of the coupling resistor R has to be decreased. If the value of the load resistor decreases below a minimum value ($R_{s1} < R_{smin}$), then the saturation condition of the T_2 transistor, $\beta \cdot I_{B2} \geq I_{Cs}$ is no longer true.

When the transistor T_2 is blocked, the load resistance R_{s1} has no influence

The load resistance R_{s2} is connected:

If transistor T_2 is saturated, the load will practically have no influence because the output resistance of the transistor in saturation is extremely small

When T_2 is blocked, the load will cause the decrease of the collector voltage and of the base current I_{B1} of the saturated transistor T_1

$$U_{C2} = \frac{R_{s2}}{R_{s2} + R_C} \cdot E_C \qquad R'_C = \frac{R_C \cdot R_{s2}}{R_C + R_{s2}}$$

$$I_{B2} = \frac{U_{C2}}{R'_C + R} - \frac{E_B}{r}$$

$$\frac{E_B}{r} = I_{Co} \quad \text{may be neglected, also } R'_C \ll R_C \text{ so: } I_{B2} \approx \frac{U_{C2}}{R}$$

Because $U_{C2} < E_C$, to keep T_1 saturated, need for a lower value for R

Driving Flip-flop Circuits

Two fundamental methods for driving a flip-flop circuit:

- a). driving using separate paths for each transistor (RS type flip-flop circuit).
- b). driving using a common path (T type flip-flop circuit)

Flip-flop circuits use one of the above described methods, or even both methods (RST or JK type flip-flop circuits)

Driving pulses may be applied on either the base or collector of the transistors
The polarity of the driving impulses, may be either positive or negative.

The role of the driving signal is not necessarily to cause by itself the switching of the flip flop, but rather to initiate a regenerating process that will lead to this

Regardless of the type of the transistor (pnp or npn) driving the blocking of the conducting transistor has some advantages:

- the sensibility of the flip-flop is higher
- the energy needed for the impulse to trigger the switching is smaller.

A flip-flop circuit using npn transistors will switch in optimal conditions if a negative pulse is applied on the base of the blocked transistor

In order to drive a flip-flop circuit with both pulses and voltage levels circuits usually have RC differentiating circuits.

Through differentiation, positive and also negative peaks emerge, so, the possibility of unwanted double-switching exists.

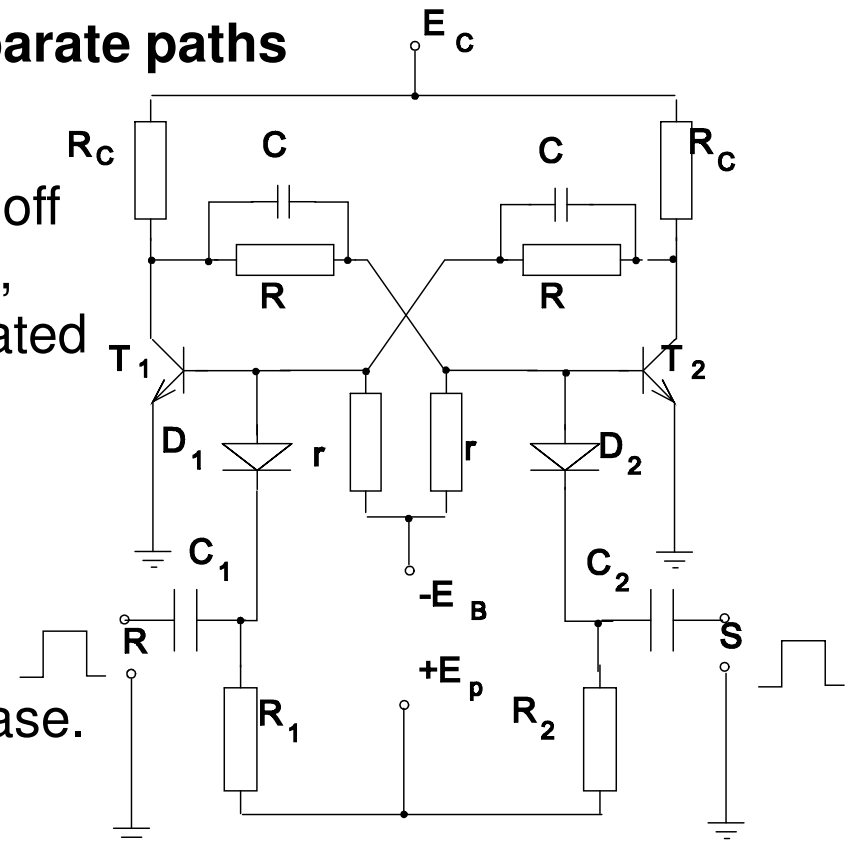
In order to avoid this situation the differentiating circuits are followed by clipping diodes, which prevent peaks with unwanted polarity from passing through

Base-driven flip-flop circuit using separate paths

Be the circuit in state T_1 - saturated and T_2 - off
If a driving impulse is applied at the input S, having the amplitude E_c , it will be differentiated by the R_2C_2 differentiating circuit.

Diode D_2 will cut the positive voltage peaks and permit only the negative peaks to pass
These negative voltage peaks will block T_2 even more

The switching does not take place in this case.



If the driving impulse is applied at the input R, the negative voltage peaks, which reach the base of the T_1 transistor, will block it, causing the switching of the flip-flop circuit

In order, for both diodes to be blocked in stationary functioning regime, it is recommended that they are both reverse biased with a positive voltage E_p . Value of this voltage is chosen a little higher than the base-emitter voltage drop of the saturated transistor. There are cases in which a separate voltage source for biasing the diodes is not used, but rather a positive voltage obtained from a voltage divider, which is connected to the voltage source E_C . This way, regardless of the polarity of the driving impulses only the negative peaks will reach the base circuit. They will cause the switching of the circuit, if the corresponding transistor is conducting, having no effect otherwise.

Collector-driven flip-flop circuit using separate paths

Driving circuit is identical, the driving signal is applied on the collectors of transistors. Potential E_C is used as a positive bias voltage for diodes.

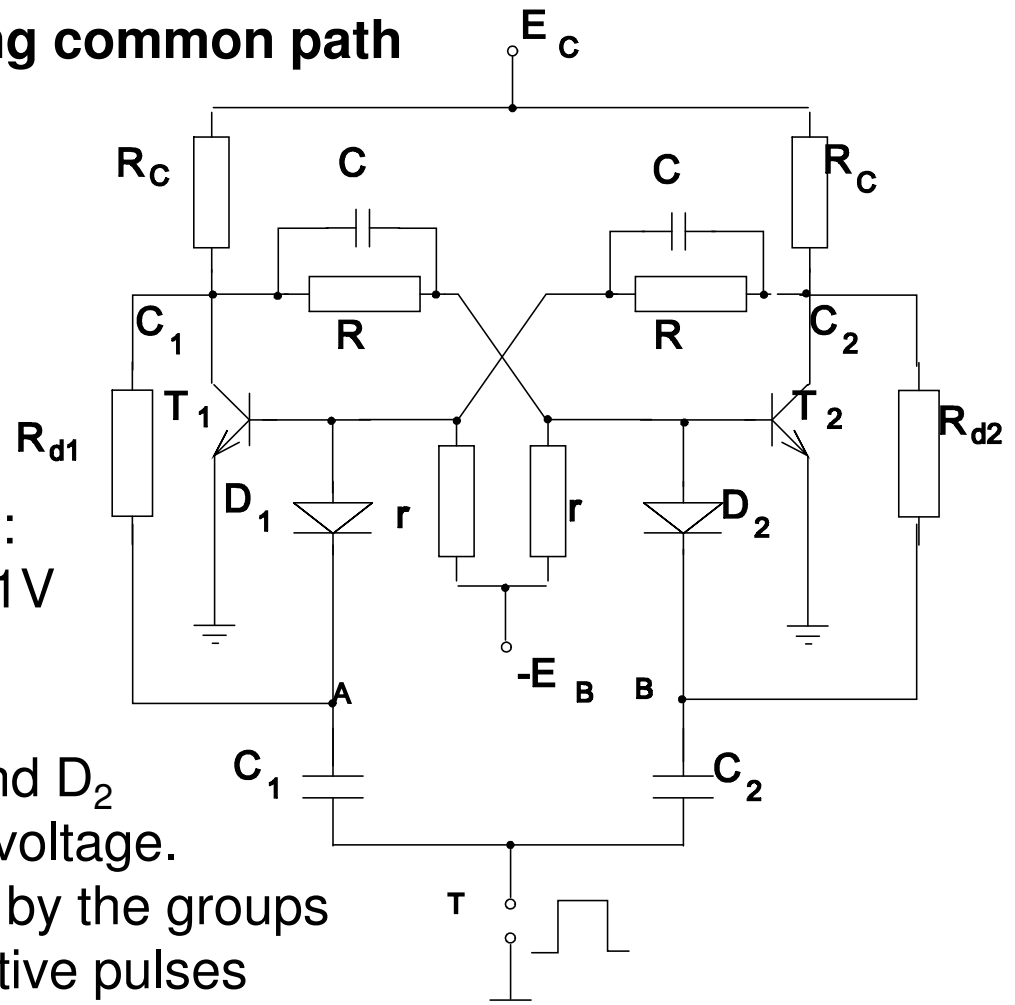
Base-driven circuits have some advantages, because allow for higher switching frequencies, and a higher sensitivity

Base-driven flip-flop circuit using common path

Be circuit in state:

T1- saturated and T2- blocked.

Voltages in different points of the schematics have the following typical values (for silicon transistors):
 $U_{C1} = +0,1V$; $U_{B1} = +0,7V$; $U_{B2} = -0,1V$



D_1 diode is therefore conducting, and D_2 is blocked with a high reverse bias voltage.

The driving pulse T is differentiated by the groups R_{d1} , C_1 and R_{d2} , C_2 . The sharp positive pulses resulted through differentiation will be cut-off by diodes D_1 and D_2 . From the two negative pulses resulted through differentiation, only the one applied on the cathode of the conducting diode D_1 will pass through, while the other one will not be able to pass through the blocked diode D_2 . Driving signal will cause the switching of the circuit, because a sharp negative pulse is applied on the base of the conducting transistor

Collector-driven flip-flop circuit using common path

Be the circuit is in state:

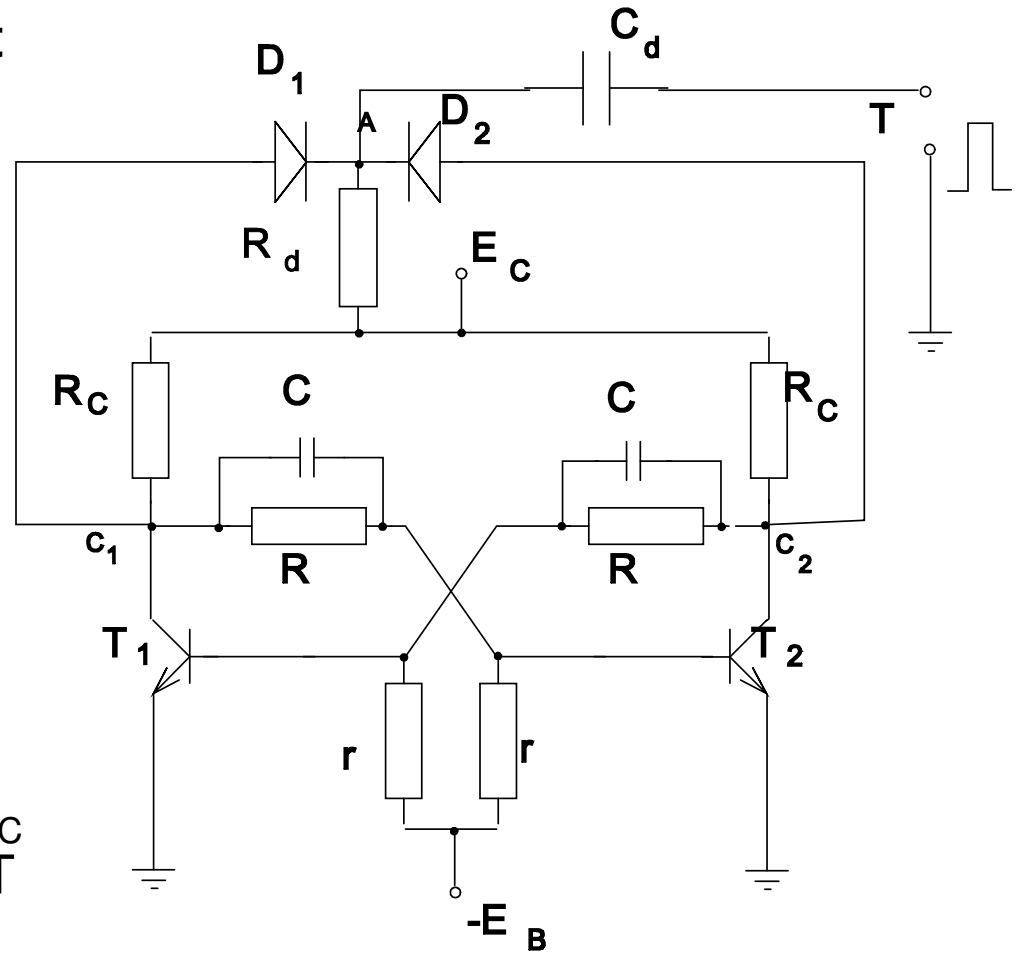
T_1 - saturated and T_2 - off

Voltages in different points:

$U_{C1} = +0,1V$; $U_{C2} \gg +E_C$,

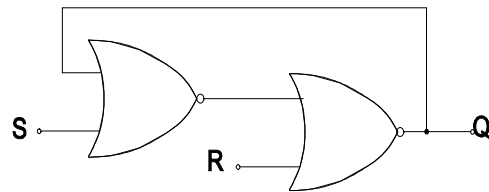
$U_A \gg E_C$

D_1 diode is blocked with a reverse bias voltage approx. equal to E_C , while D_2 diode is blocked with a small reverse bias voltage, equal to the voltage drop on the R_C .
Driving pulse applied at the input T is differentiated by $R_d C_d$.

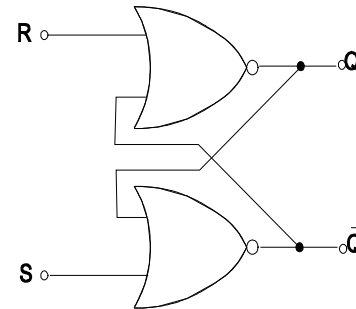


The negative voltage peaks, which result through differentiation (due to polarity of the diodes) can reach only the collector of the blocked transistor (the negative voltage leap is transmitted, in this case, through the D_2 diode in the collector of the cut-off T_2 transistor), making it to switch on.

Asynchronous S-R type flip-flop circuit



RS type flip-flop with NOR gates

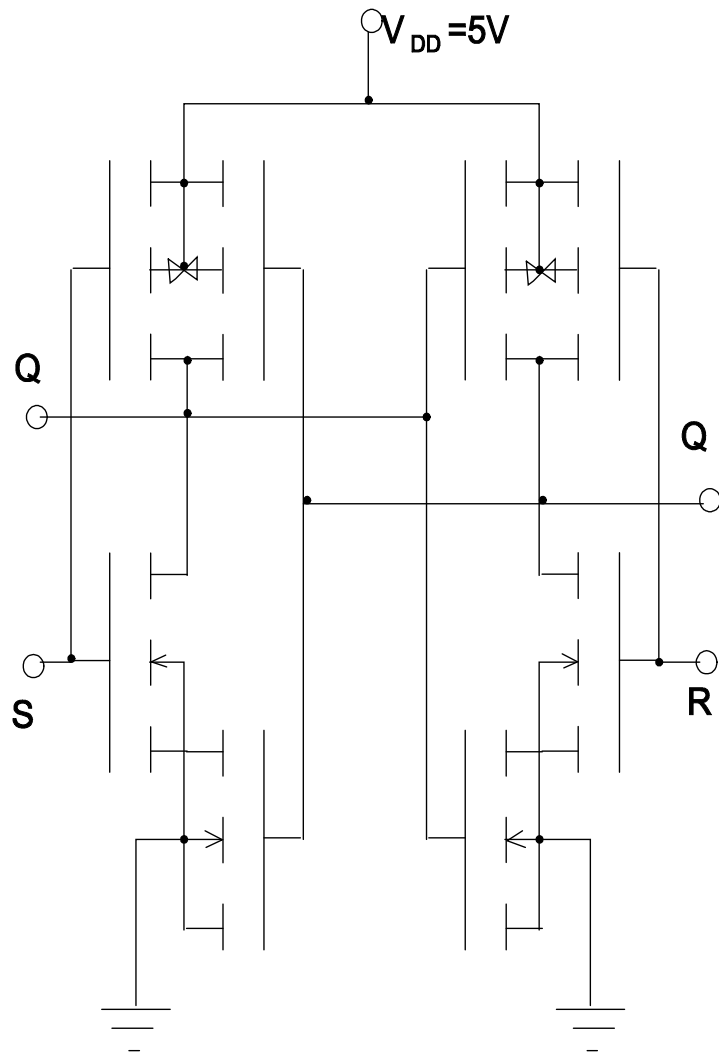


Symmetrical RS type flip-flop with NOR gates

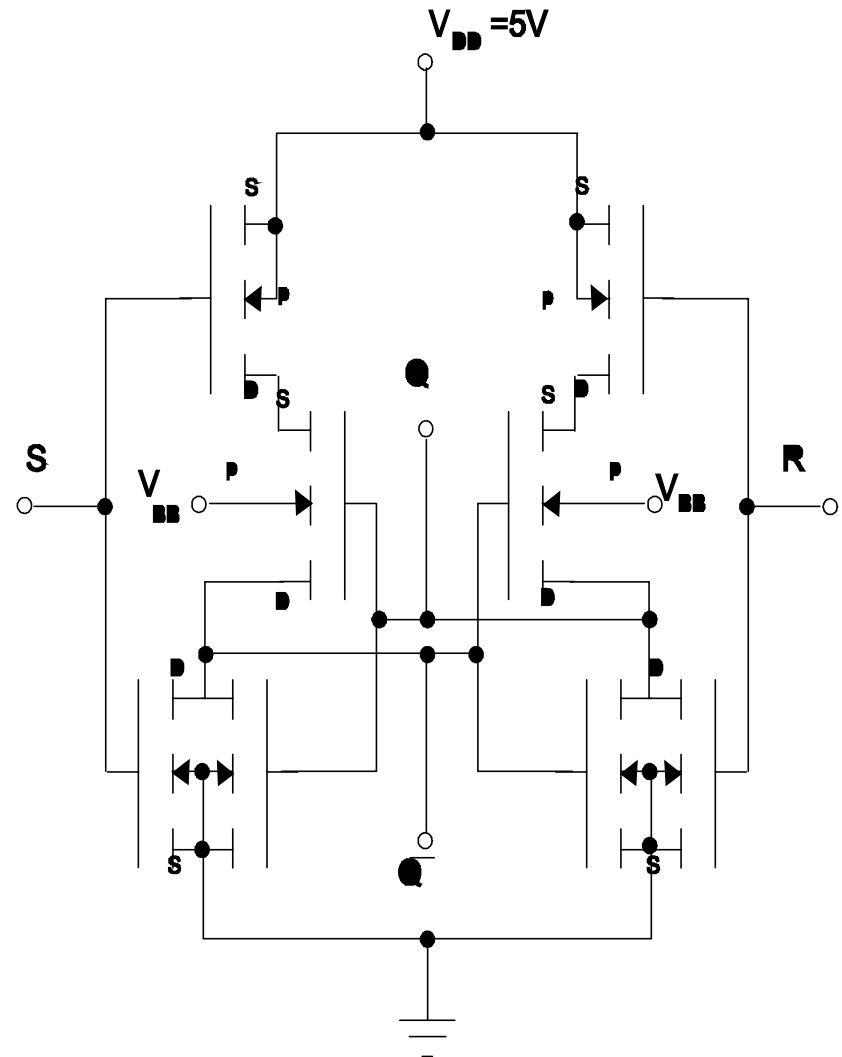
Simple flip-flop circuit may be built, from a logical point of view, by introducing a reaction loop in a logic gate network, made out of NOR or NAND gates. Inputs of the flip-flop circuit are called S (**set**) and R (**reset**)

S	R	Q^+
1	0	1
0	1	0
0	0	Q
1	1	Not allowed inputs

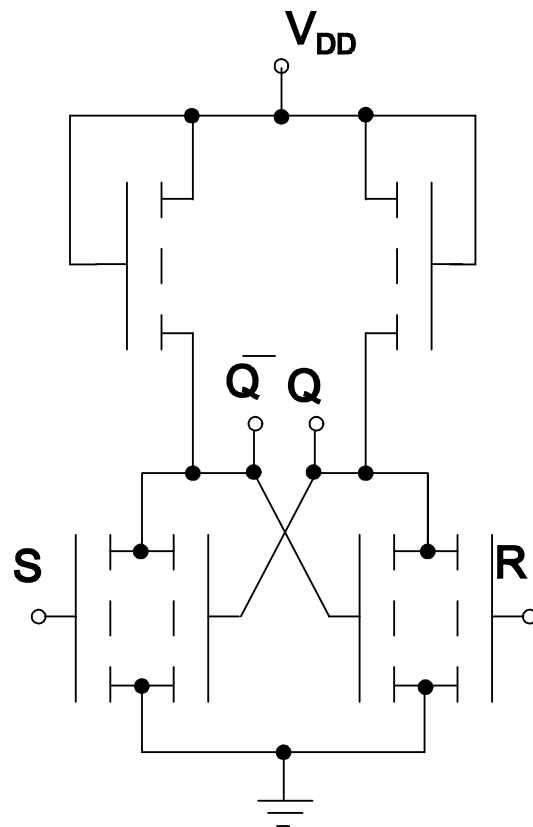
RS flip flop truth table



RS type CMOS integrated flip-flop
circuit with NAND gates

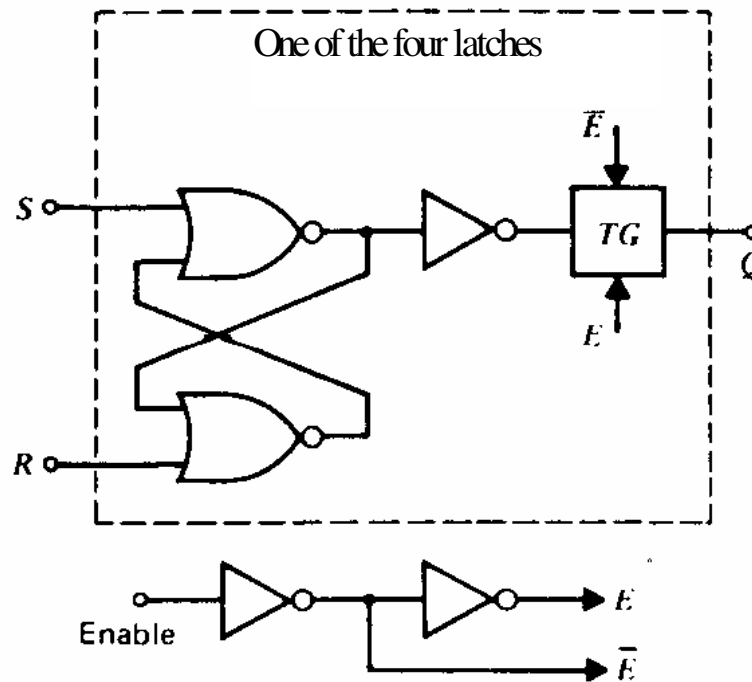


RS type CMOS integrated flip-flop
circuit with NOR gates



Flip-flop with MOS components

An integrated circuit that contains RS type flip-flops with CMOS components: 4043 integrated circuit, which has four RS type flip-flops (*latches*)



S	R	E	Q
X	X	0	OC
0	0	1	NC
0	1	1	0
1	0	1	1

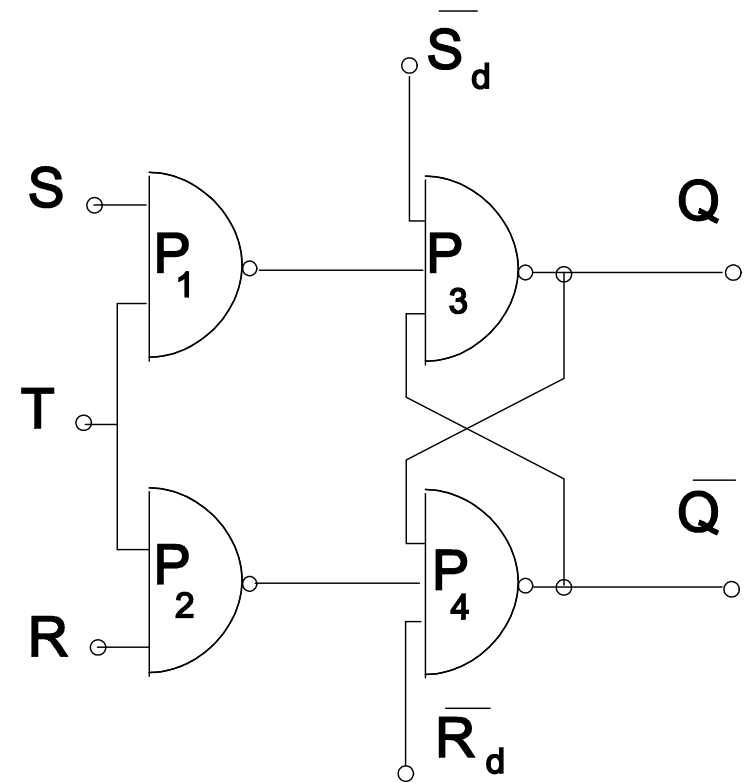
OC = Open circuit
 NC = No change
 X = Indifferent value

The internal logical schematics for the 4043 circuit

Synchronous SR type flip-flops

Synchronous RS type flip-flops have two data inputs: R and S and a clock input: T.

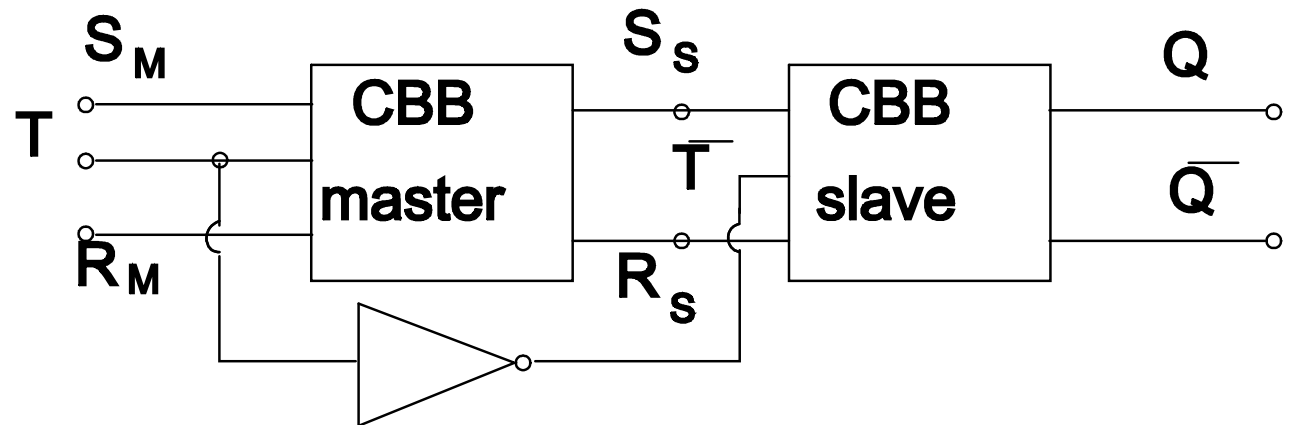
The information from the data inputs R and S is received by the flip-flop only at the arrival of a clock pulse, either the positive or the negative edge.



The synchronous RS type circuit has a clock signal (the inputs R and S remain asynchronous), which controls the evolution of the circuit.

It also has two other inputs, **Clear** and **Preset**, which act directly on the outputs Q and Q- overriding the inputs R and S

RS master-slave flip-flop



RS master-slave flip-flop: designed to overcome the disadvantages of cascading several RS type flip-flops (the possible non-determination of the states for each flip-flop)

First flip-flop, called master flip-flop is driven by the data inputs R and S, while the second flip-flop, called slave flip-flop, is being driven by the outputs of the master flip-flop. Short description:

- on the rising edge of clock pulse, the master flip-flop is disconnected from the slave flip-flop, as they can't communicate; On this edge, the S and R inputs act on the master flip-flop, determining the corresponding switching
- when the clock signal goes from '1' into '0', on the falling edge, the slave RS inputs are disconnected from the master; the outputs of the master drive the state of the slave.

This way, only one single flip-flop is active at a given moment, the outputs of the master-slave flip-flop being completely isolated from its inputs.

Using this circuit, logic uncertainty for a sequence of flip-flops is avoided.