SEMICONDUCTOR MEMORIES

Semiconductor Memories

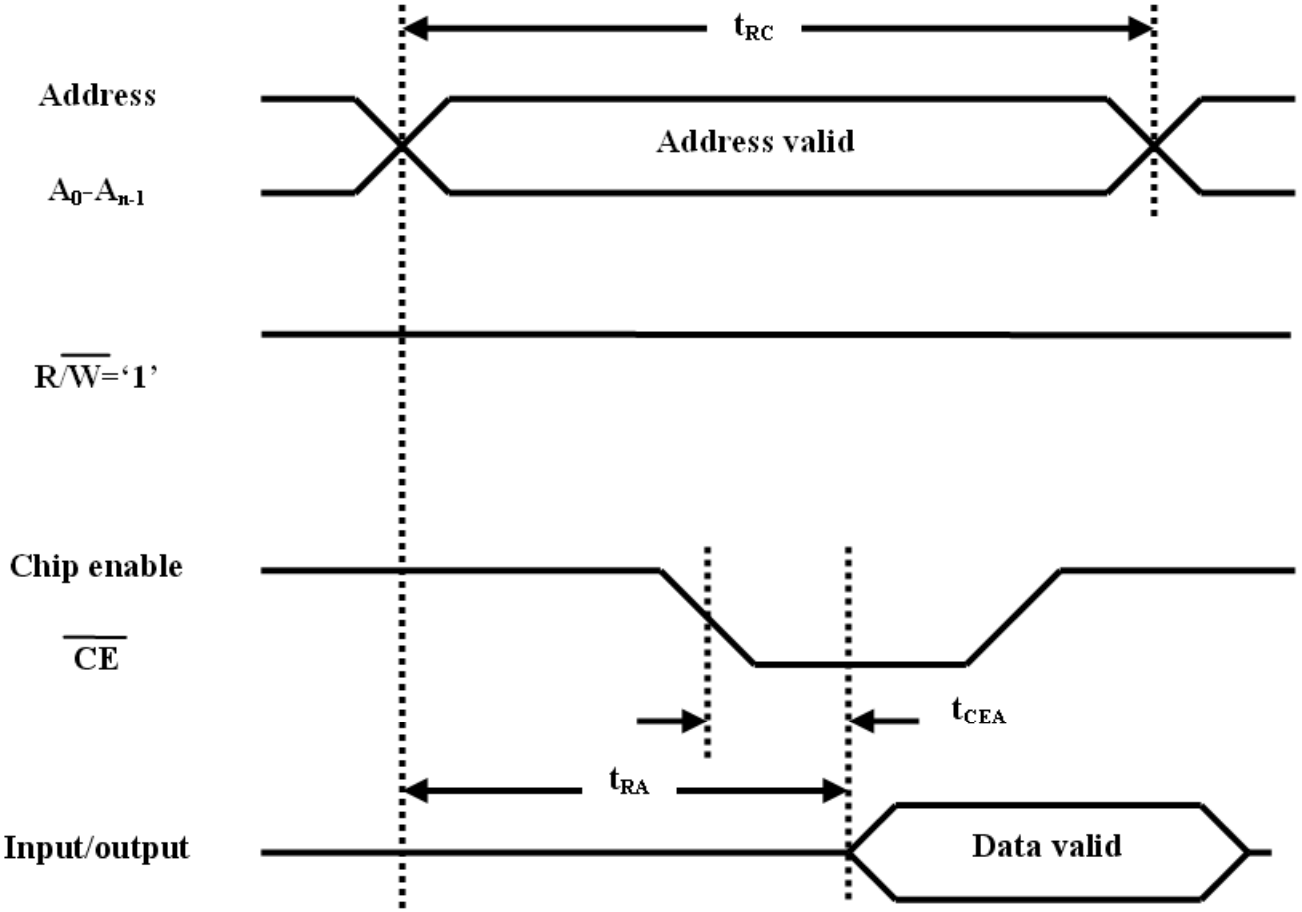
- Memory circuit - based on a memory cell, defined as a device which stores (memorises) an information bit
- A logical sequence of memory cells (usually as a bidimensional array) gives the concept of memory circuit
- Integrated memory circuits composed of:
  - Memory cells array
  - decoders for addressing each cell
  - Amplifiers for read data lines or data to be written in each cell
  - Control circuits (control of all operations over the memory circuit)

- There are two main memory circuit categories:
  - Volatile memory, maintaining information only that period the power supply applied
    - Read/write memories (RAM *Random-Access Memory*), allow for read/write operations over each cell; cells are accessed in similar way, doesn't matter cell position within array; two types:
      - static (SRAM Static Random Access Memory)
      - dynamic (DRAM Dynamic Random Access Memory)
    - Content addressable (CAM Content-Addressable Memory)
  - Non-volatile memory, maintaining information after the power is off
    - Read/Only memory (ROM *Read-Only Memory*), content can not be modified by an usual read/write operation; classified as:
      - permanent (ROM *Read-Only Memory*)
      - programmable (PROM Programmable Read-Only Memory)
      - reprogrammable (REPROM REProgrammable Read-Only Memory)
        - » X rays erasable (UVEPROM Ultraviolet Erasable Programmable Read-Only Memory)
        - » Electric erase (EEPROM Electrically Erasable Programmable Read-Only Memory)

Read/Write Memory (Random Access Memory)

- Each RAM circuit has specific diagrams giving the timing needed for correct read/write operations (*read and write cycle timings*)
- Read cycle
- Write cycle

Read cycle



Address information is prior to data info; so address lines are firstly activated (enabled)
Address info must be valid for $\mathbf{t_{RC}}$ (time of read cycle)

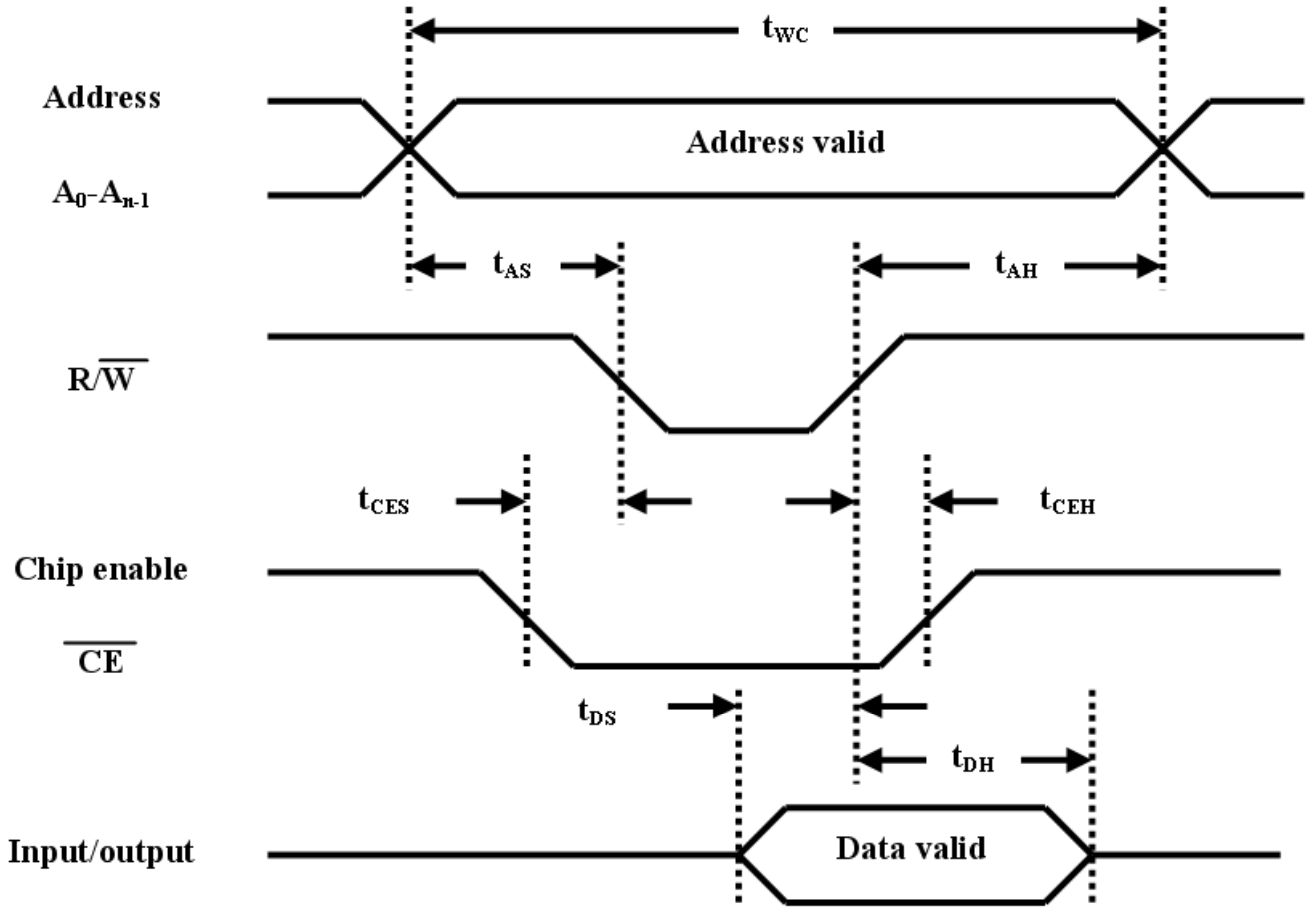
Shortly after address lines enabled, the circuit must be selected: CE- (chip enable signal, active low)

At $\mathbf{t_{CEA}}$ moments from circuit enabled, data are read being available at the data pins of that circuit

Another inportant time $\mathbf{t_{RA}}$, access time for read operation, gives the time needed by that circuit for the read operation, being the time difference between address enabled moment and data available at circuit pins

Write Cycle

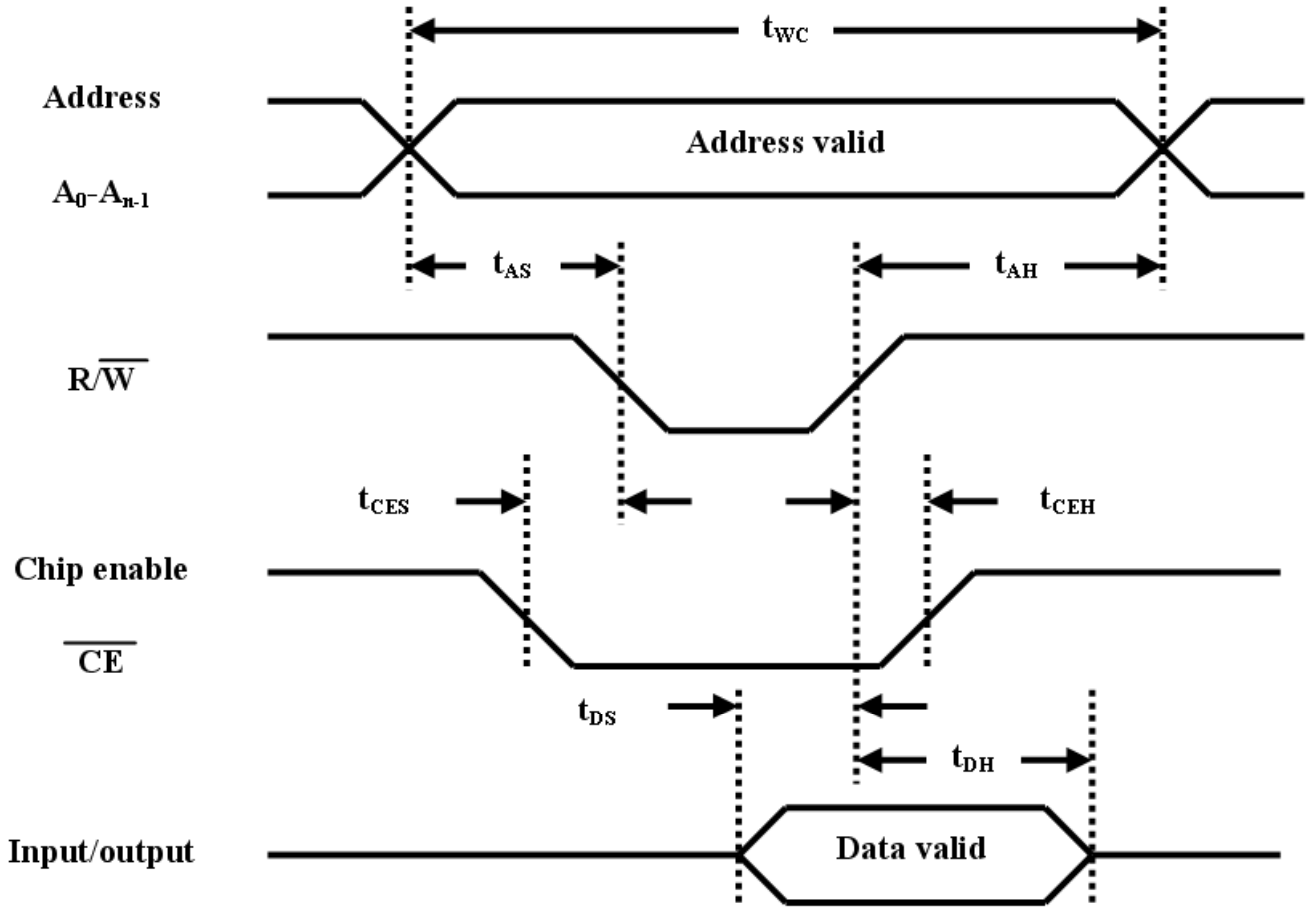
Also, address lines are firstly valid, and must be valid for $\mathbf{t_{WC}}$ (time related to the write cycle)



Circuit is enabled CE- signal generated; at $\mathbf{t_{CES}}$ after, the write command signal R/W- is generated; this signal is delayed with the set-up $\mathbf{t_{AS}}$, from address enabled moment: time needed for a correct setup of address lines

Another set-up time, $\mathbf{t_{DS}}$, gives the difference between start of data availability and disable moment of read/write command signal

Typical parameters for memory circuits (given by data books, by their minimum values):



Data Hold-up time, $\mathbf{t_{DH}}$ or the time needed to maintain data for a correct write operation

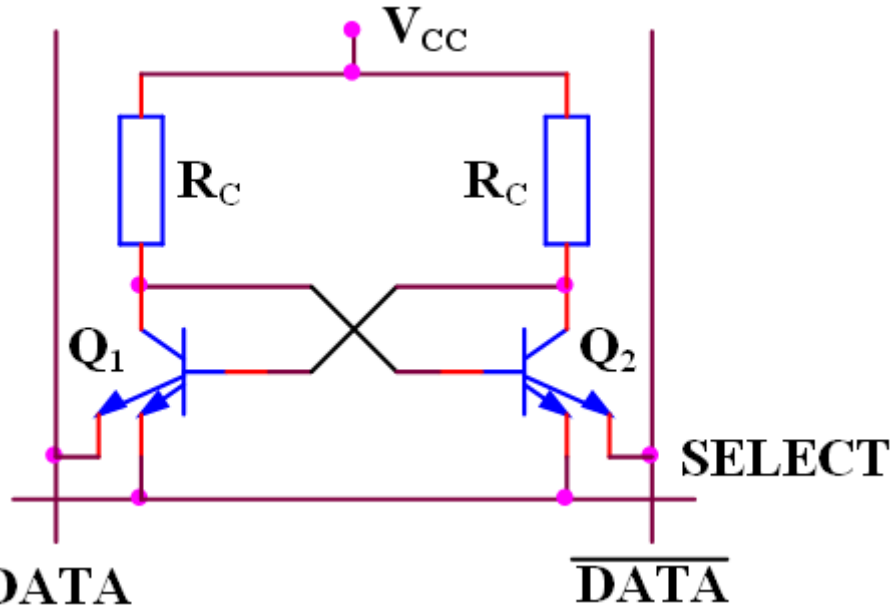
Hold up time for cheap enable signal, $\mathbf{t_{CEH}}$ or how long time to maintain CE- signal after the write command signal is no more valid

Address hold-up time $\mathbf{t_{AH}}$, or how long to maintain addresses valid, after the write command is off

- For DRAM circuits, CE (*Chip Enable*) signal is replaced by two specific enabling signals: one enabling access to the lines of cell array (signal **RAS** - *Row Access Strobe*) and respectivelly to the memory array columns (signal **CAS** - *Column Access Strobe*); signals are used also for information refreshing logic
- DRAM circuits need an extra cycle (refresh cycle)
- DRAM circuits offer higher integration capacity, but higher access time, compared with SRAM circuits
- A typical memory module looks like an array of LSI circuits, designed to offer the needed storage capacity (expressed in bits, or bytes); number of bits given by number of memory words multiplied with the word's length.
- A memory word is considered by those cells connected at the same address selection line; word's length may vary, but is multiple of octets (*byte*).
- Beside addressing, read/write operations are to be considered
- These three elements: memory cell structure, addressing scheme and read/write oparations are offering full info about the memory system

Bipolar SRAM memory cell

Based on a latch (flip-flop with multi-emitter bipolar transistors). One emitter is connected to data lines (complementary Data or ¬Data lines), the other emitter connected to the common selection line (SELECT) of the memory word



Read operation of cell content is done on a high level for SELECT signal; this allows transfer of a current flow by the emitter circuit of the conducting transistor to corresponding line DATA or ¬DATA (depending on the conducting Q); an amplifier will sense this current flow.

Write operation done by raising up the SELECT line and forcing to Low level one data line (DATA or ¬DATA, depending on written info bit) to turn on that corresponding transistor

When SELECT line is at the Low level, the cell is not selected; the transistors will generate current flow through the corresponding emitters tied to SELECT line; so the DATA and ¬DATA lines will not present current flows, and the associated amplifiers will not detect any current flow. Even if the binary state of DATA and ¬DATA lines is modified but line SELECT line is still low, the memory cell stored data will not be changed.

Access time depends mainly on the load resistance R_C.

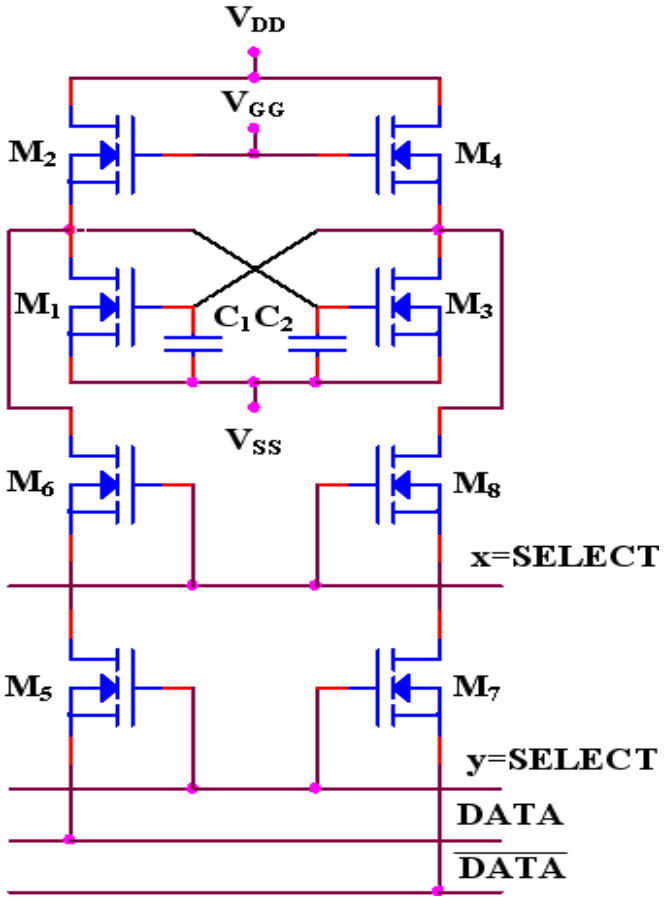
SRAM cell with NMOS circuits

Based on a latch made up by transistors M_1 and M_3 with associated load resistances as transistors M_2 & M_4. Within the array of memory cells, there are selection lines for array's line and column selection; the cell is selected by coincidence.

DATA & ¬DATA lines are used for info read and write operations.

Power dissipation may be tempered by control of the V_{GG} power supply (used by the load transistors).

When this power is off, transistors T_2 and T_4, are off (present a high impedance); this implies that the stored info is kept by the parasitic capacitances of transistors M_1 & M_3.



Characteristic to the dynamic circuits is the need for info refreshing, due to discharge of capacitors used to keep info. That's why periodically V_{GG} is brought on, activating transistors M_2 & M_4.

Cell read operation is achieved by pushing SELECT high, opening transistors M_5, M_6, M_7 & M_8 , so stored info is available on data lines.

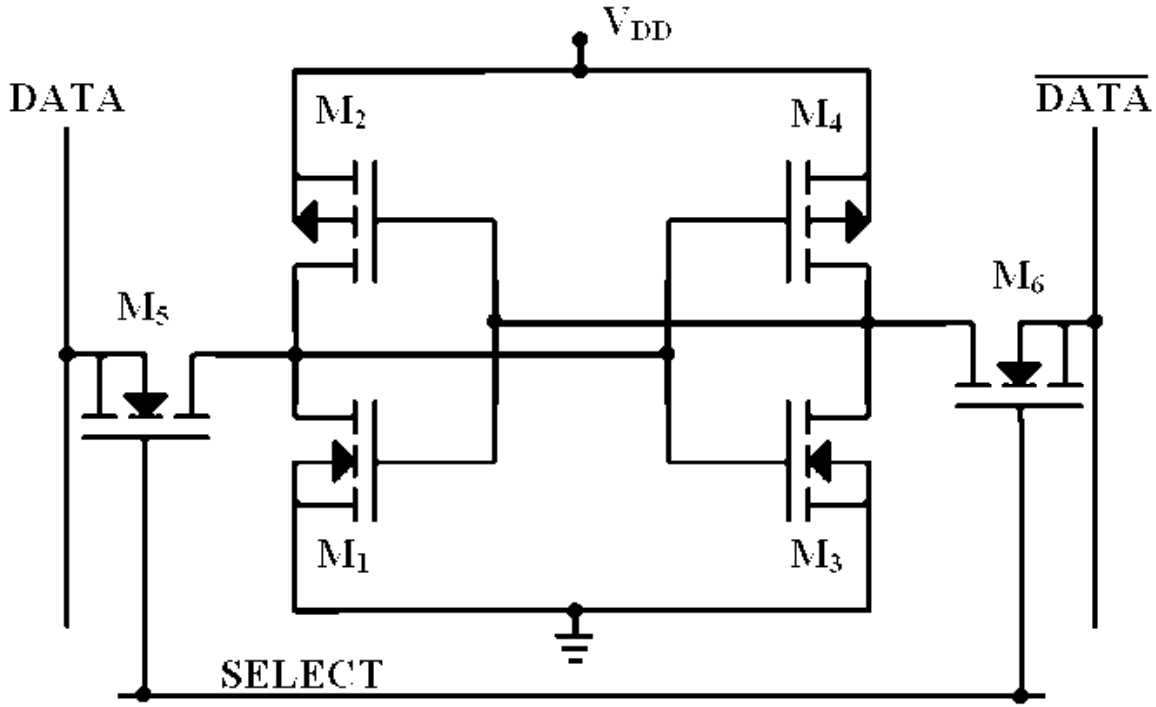
Cell write operation is done making High the SELECT line, opening transistors M_5, M_6, M_7 & M_8 and setting them according to the state of data lines

SRAM cell with CMOS circuits

Based on a latch made up by transistors M_1, M_2, M_3 & M_4.

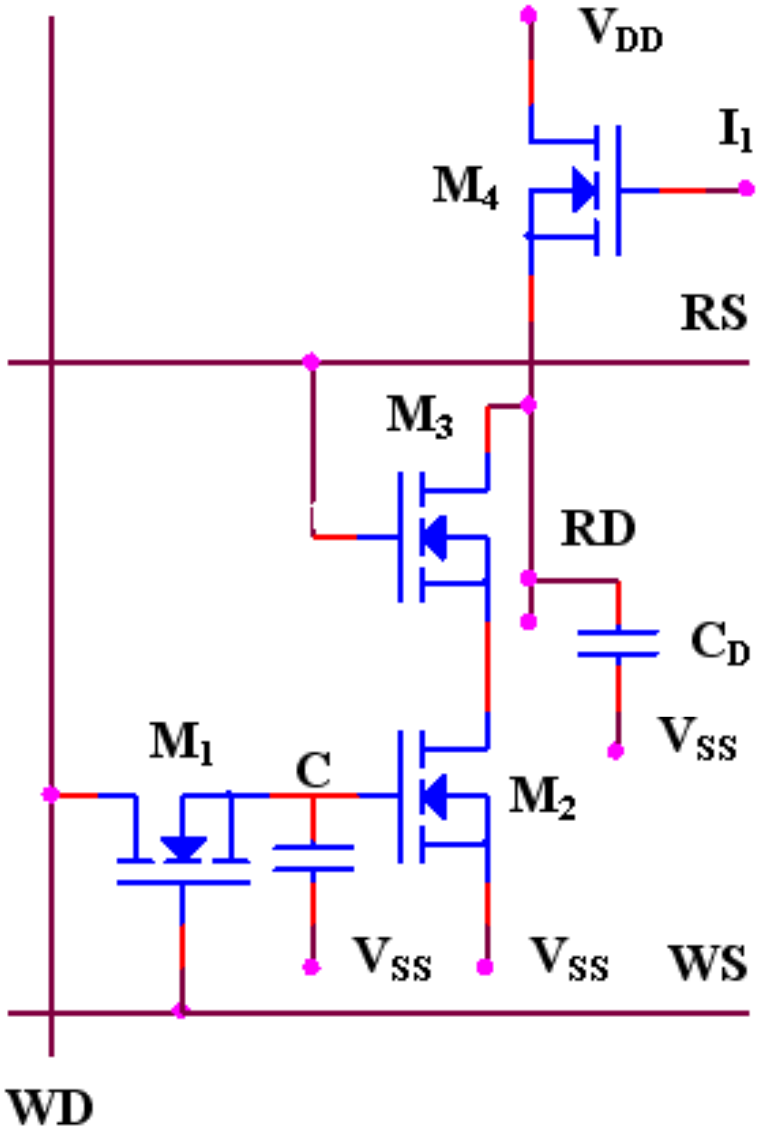
Cell read operation: High state for SELECT line, opening transistors M_5 & M_6 making possible to find state of latch (read info stored there).

Cell write: making High the SELECT line, opening transistors M_5 & M_6 so accessing the latch and setting its state according to state of data lines (writing info).



DRAM MOS memory cell with three transistors

Read cycle: initially capacitance C_D from the read data line R_D, is pre-charged at a potential approx. V_{DD} (using transistor M_4 and input I); read selection line RS, is activated; if potential of capacitance C was initially over threshold voltage, transistors M_2 & M_3, forming a NAND gate will be on, discharging capacitance C_D to low potential V_{SS}; if capacitance C was initially with a potential under threshold level, transistors are off, and potential of C_D remains unchanged; this way, on the RD line there will be the complementary info of that stored by capacitance C, and it will further amplified



Write cycle: write selection line WS made High, makes possible transfer of logic info from write data line WD onto capacitance C

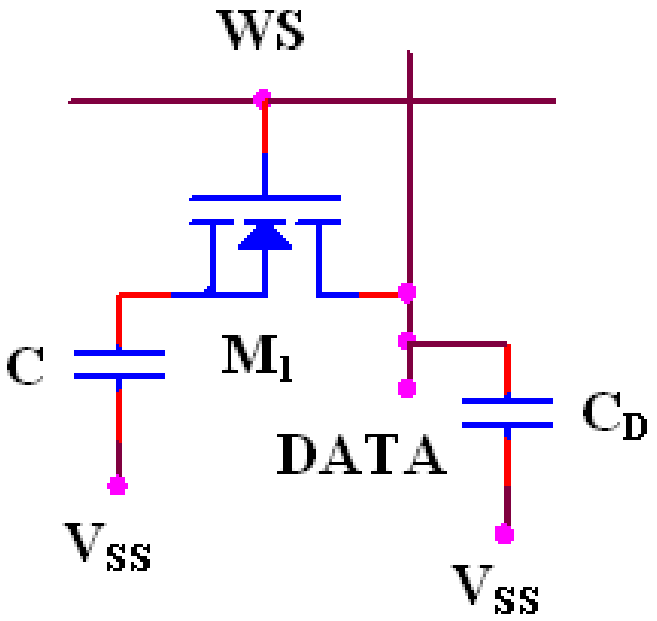
Refresh cycle: periodically the cell is read, info from RD line is amplified and complementary info is re-written onto cell

DRAM memory cell with one MOS transistor

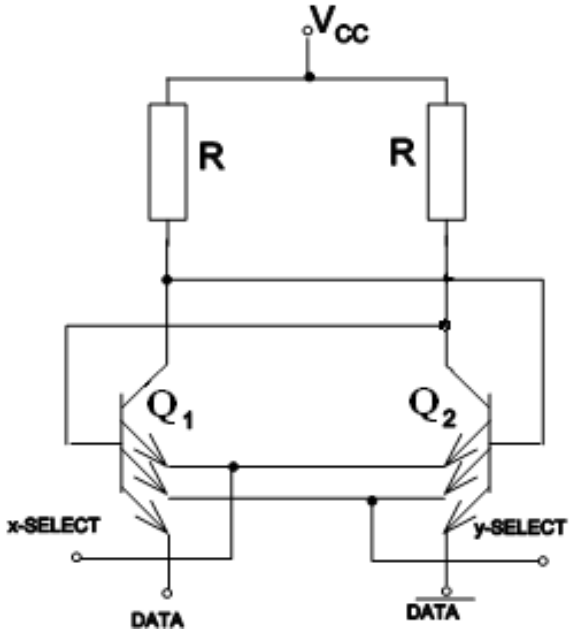
Read cycle: word selection line WS on, charge stored on capacitance C will modify info on DATA line, an amplifier will sense it

Write cycle: WS line activated on, capacitance C will charge from potential of DATA line, through open transistor M_1

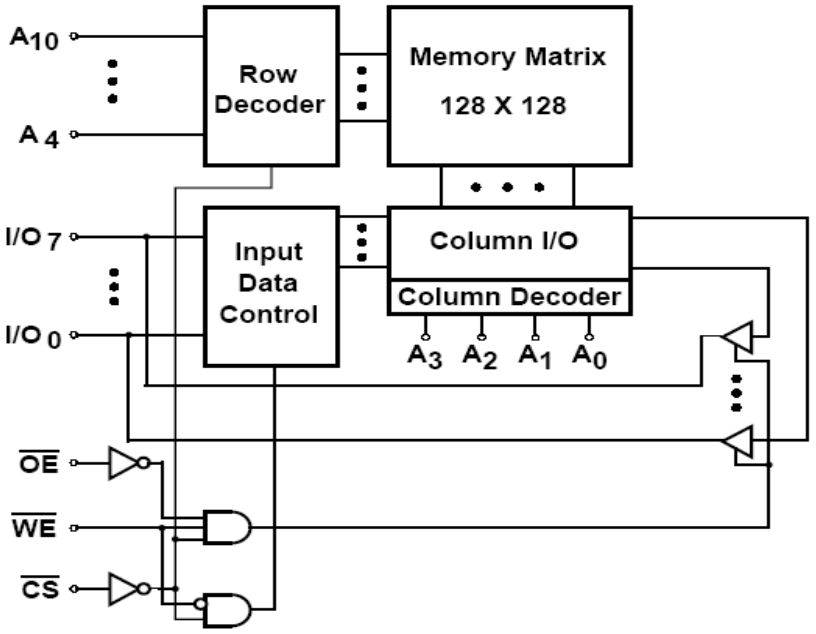
Read operation is destructive and cell must be re-written after each read cycle; it implies additional circuits and extra timing



Structure of the integrated memory circuit



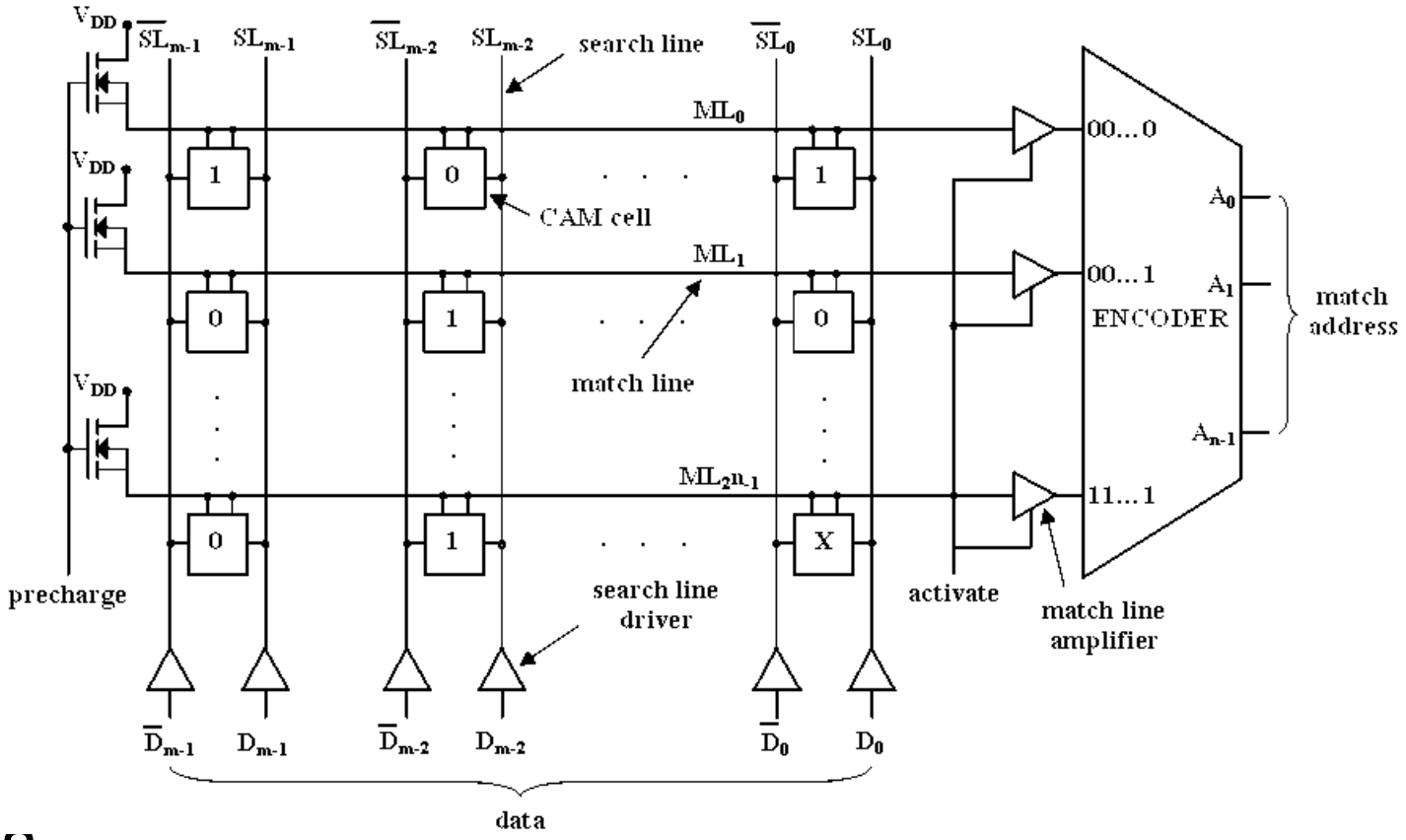
- Operational blocks:
  - Address decoding circuits, for cell selection; usually selection coincidence is used: vertical and horizontal selection within the array of memory cells; a possible layout for simple selection is shown by the right figure
  - CS signal (*chip select*), for selecting the integrated circuit, activating the internal circuits for selection and read/write operations
  - Amplifiers for read/write operations
  - Output buffers, open collectors or three state type, offering interconnectior
  - Refresh circuits, for dynamic MOS based memories
- A memory chip consists of many cells, grouped in an array. Number of external pins limits the extensions; usually an integrated circuit contains many memory words, but a word has small length (one, two bytes).



Content Addressable Memory: Introduction

- Hardware devices having as characteristics: on the data lines a word is given, and memory gives back the location address where word is
- Structure:
  - RAM memory
  - Comparator circuits
- Usefulness:
  - Computer networks devices
  - cache processors
  - Data base accelerators
- Classification:
  - binary (search and store ‘0’ and ‘1’ states)
  - ternary (search and store ‘0’, ‘1’ and ‘X’ states)

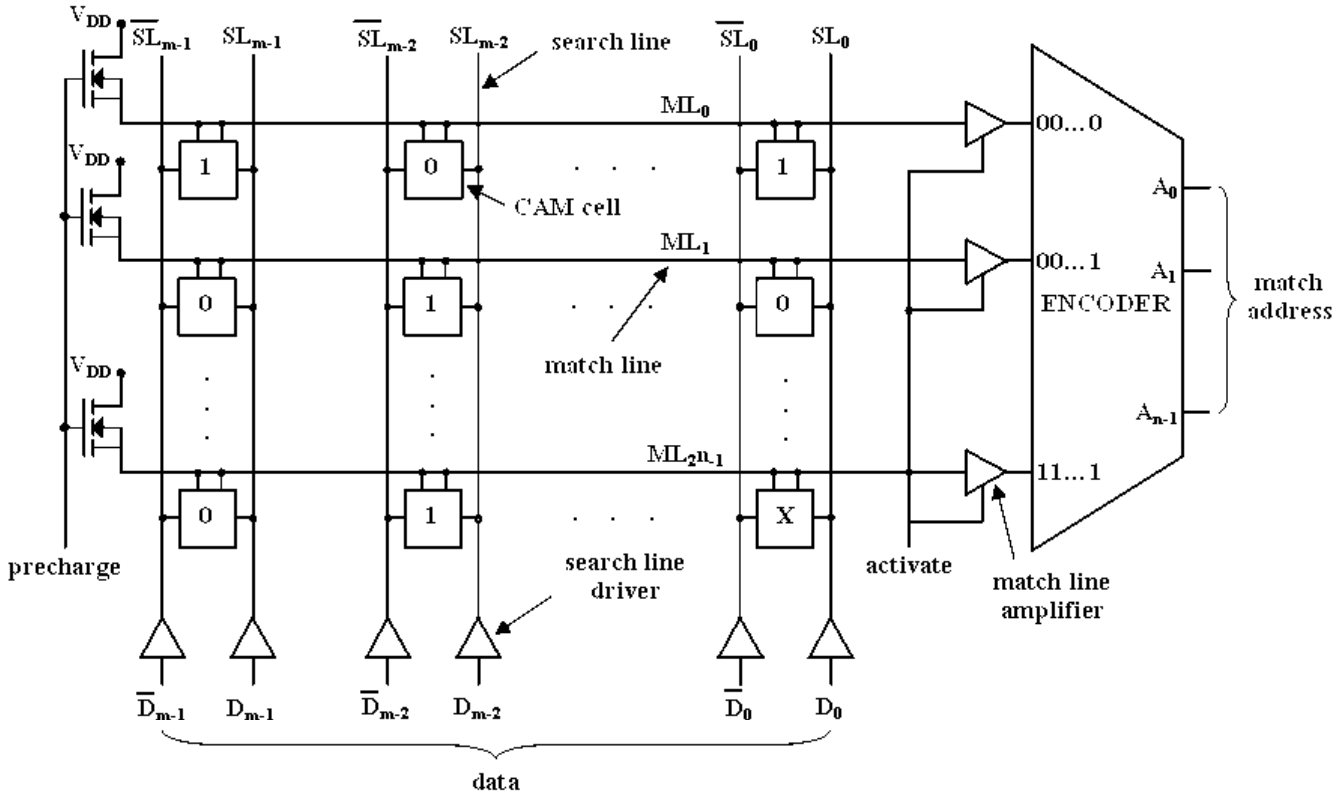
CAM Architecture



- $2^n \cdot m$ CAM cells
- CAM cell contains circuits for storing and comparing info
- *Search* lines transmit to CAM cells the word to be compared
- *Match* lines show if a coincidence was or wasn't found (between transmitted word and content of current address)

Logic state ‘1’ for *match* line defines the coincidence;

no coincidence is represented by logic state ‘0’



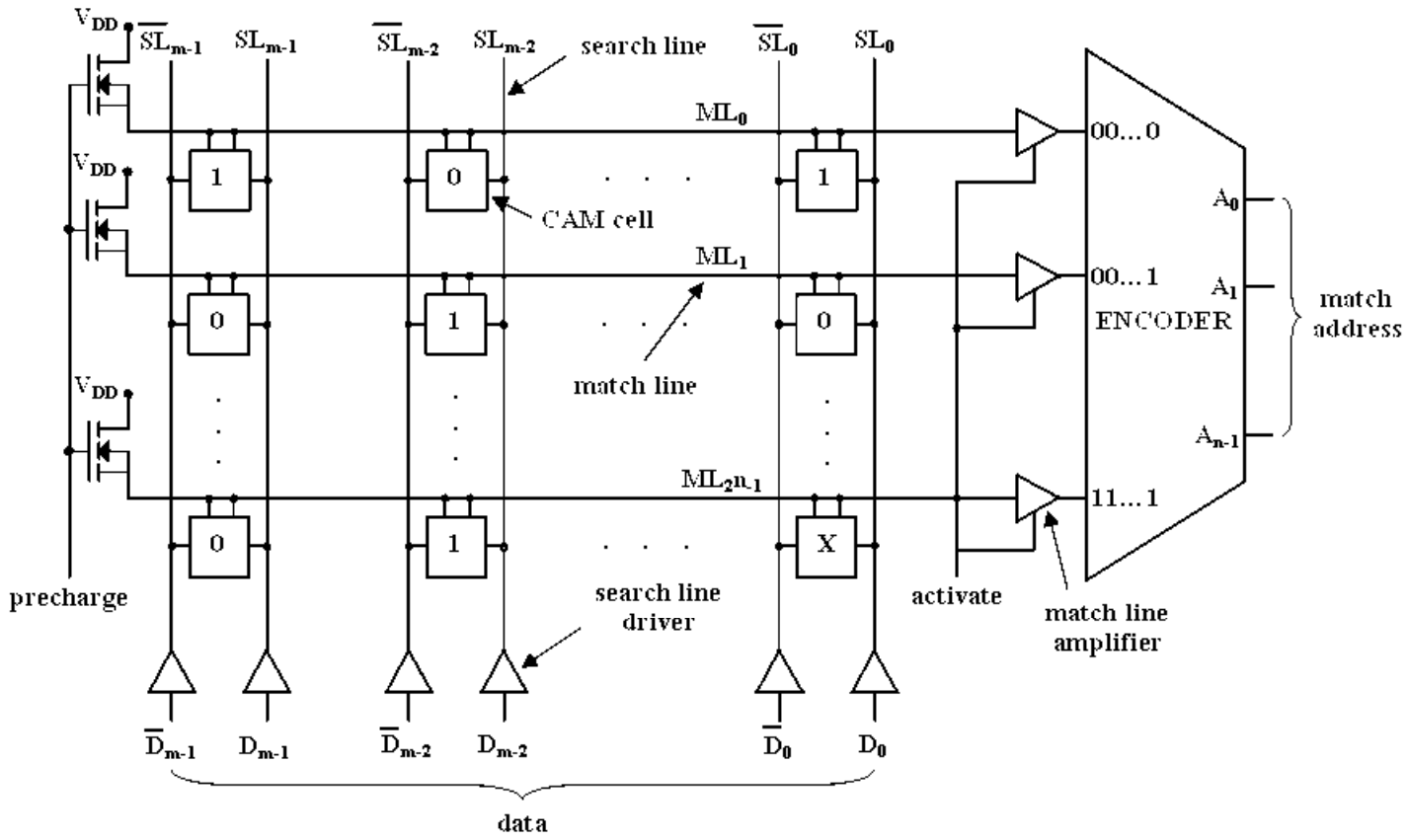
Encoder circuit generates address of memory location where a coincidence was found

For *search* & *match* lines specific drivers and amplifiers are used

Precharge signal sets all match lines to ‘1’

Signal *activate* allows transmission of line state to encoder

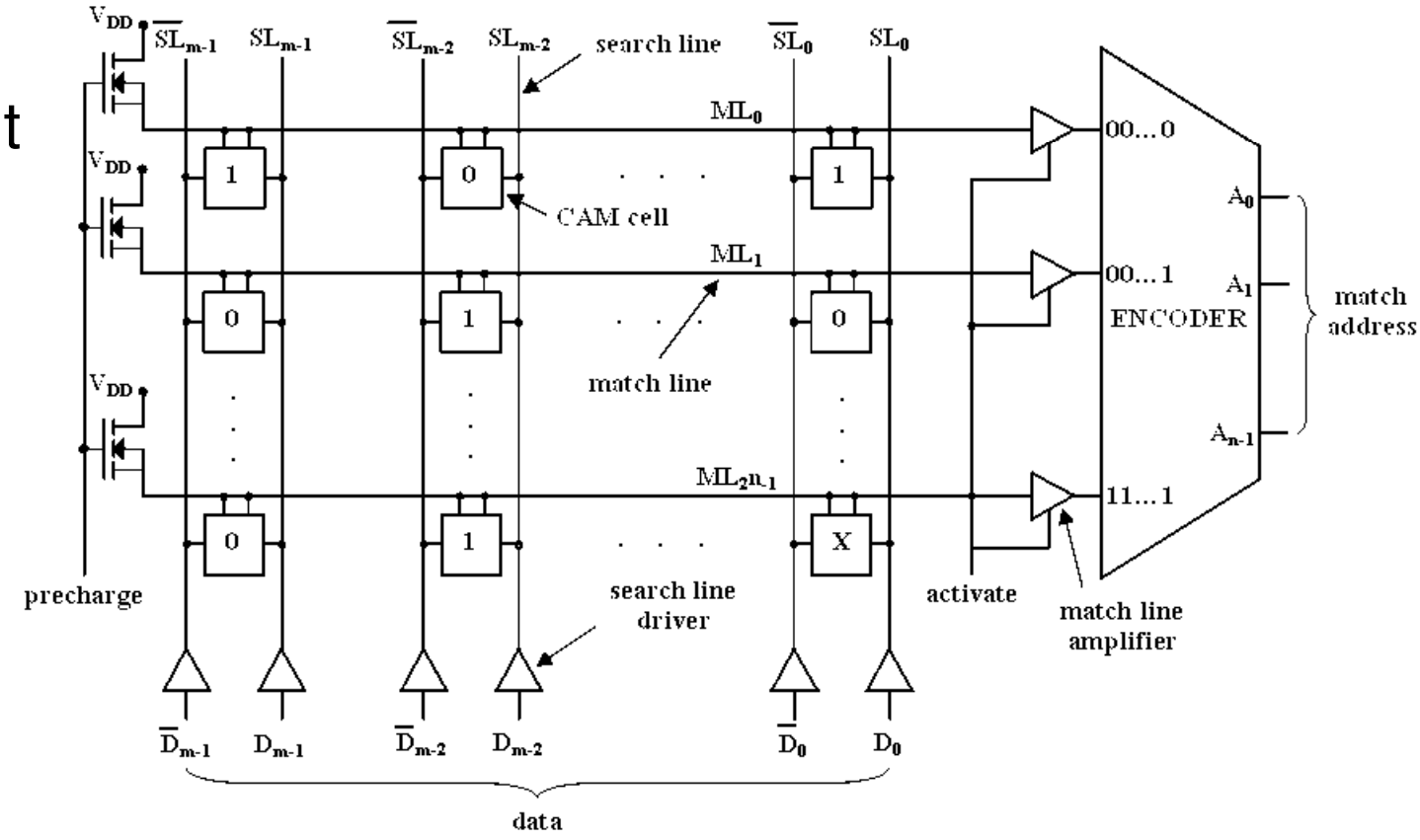
CAM memory operations



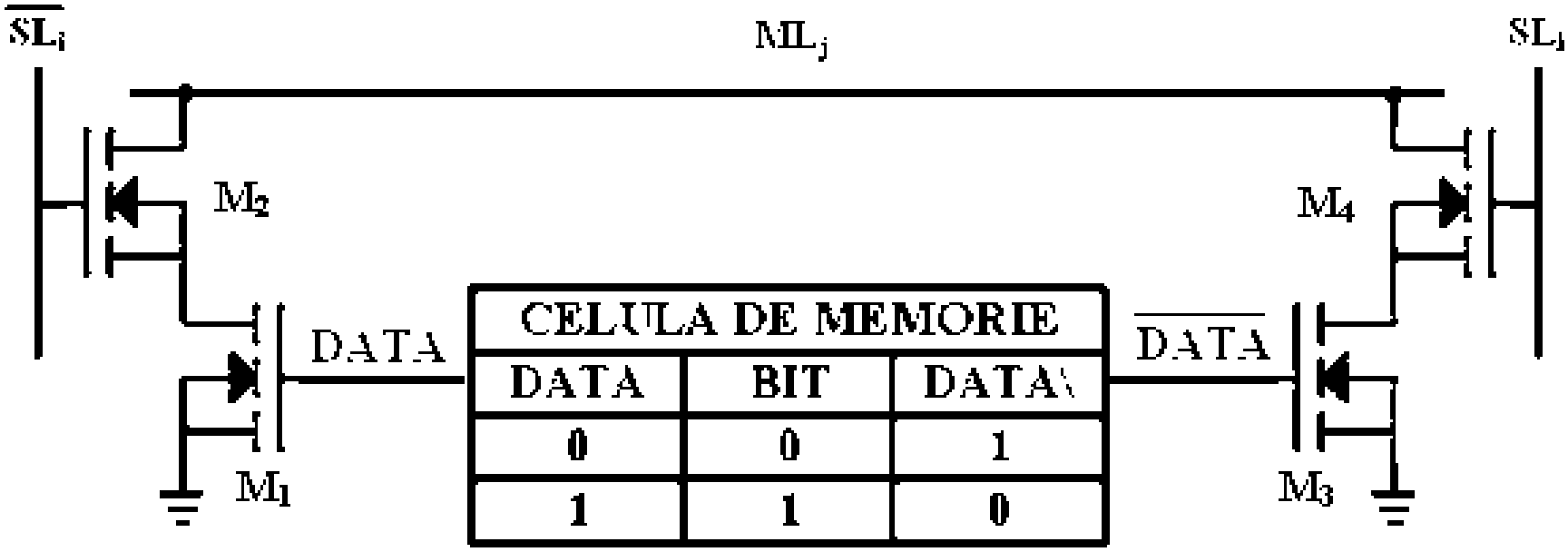
1. All *match* lines are precharged to '1' by activation of *precharge* signal, opening transistors and raising potential of *match* lines to V_{DD}
2. *search* line drivers transmit info to be searched onto *search* lines

3. CAM cells where exists coincidence between info from *search* lines and their content, or are storing ‘X’ state will not affect the logic state of *match* lines; CAM cells not presenting coincidence will switch *match* lines into ‘0’. *match* lines will be effective only if all are in ‘1’, activating encoder circuit; so there is coincidence with the word from the *search* lines

4. Encoder will give at output the address of that location containing the desired word



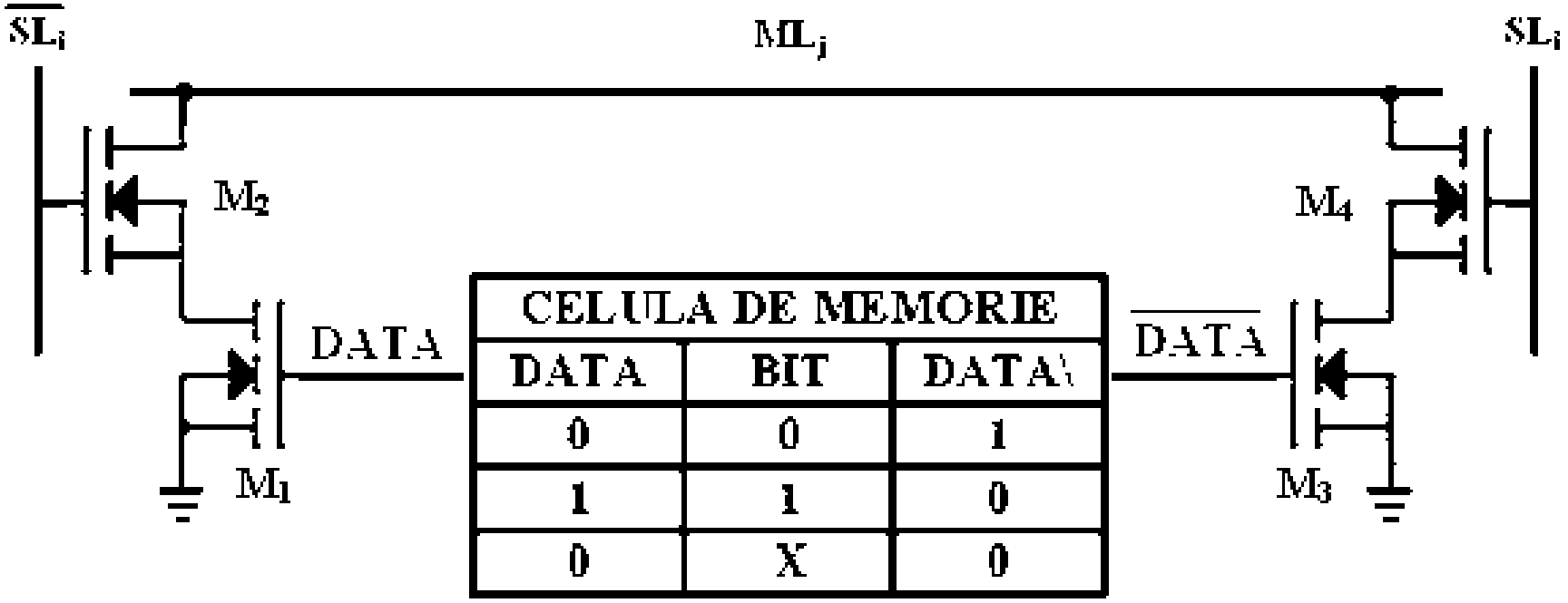
Binary CAM memory cell



CELULA DE MEMORIE		
DATA	BIT	DATA\
0	0	1
1	1	0

- Composed by a memory cell and comaparator circuits
- If DATA='0' and SL='0', M_1 & M_4 off, ML='1'
- If DATA='1' and SL='1', M_2 & M_3 off, ML='1'
- If DATA='0' and SL='1', M_3 & M_4 on, ML='0'
- If DATA='1' and SL='0', M_1 & M_2 on, ML='0'
- ML = DATA **XNOR** SL

Ternary CAM memory cell

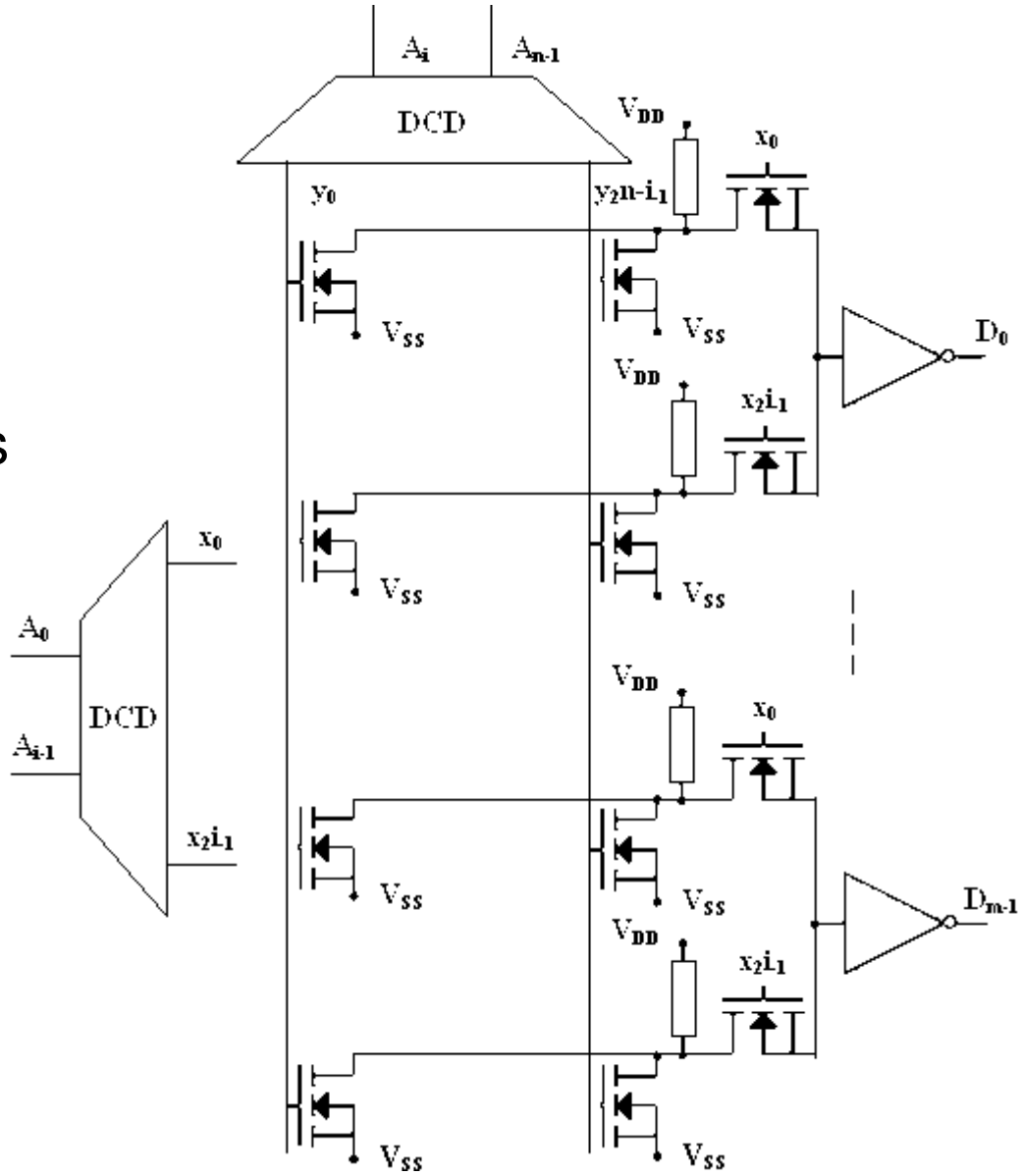


CELULA DE MEMORIE		
DATA	BIT	DATA\
0	0	1
1	1	0
0	X	0

- Extra state ‘X’, meaning that ML line will stay ‘1’ no matter the state of *search* lines; this is done having ‘0’ on both DATA & DATA\ ; transistors M_1 & M_3 will stay off, making ML line high

ROM memory circuit using MOS transistors

- Composed from an array of **n** rows and **m** columns, all outputs of address decoders
- Array with the lines made up by semiconductor devices (**p** or **n)**, connected to V_{SS}, or to a potential derived from a horizontal selection line
- Array columns are metalic layers connected to a vertical selection line
- At each cross of a line with a column may or not may be generated by epitaxial growth a dioxide gate, as a ‘1’ or ‘0’ info must be stored
- Circuit outputs form a wired OR between cells that may be selected for that output bit

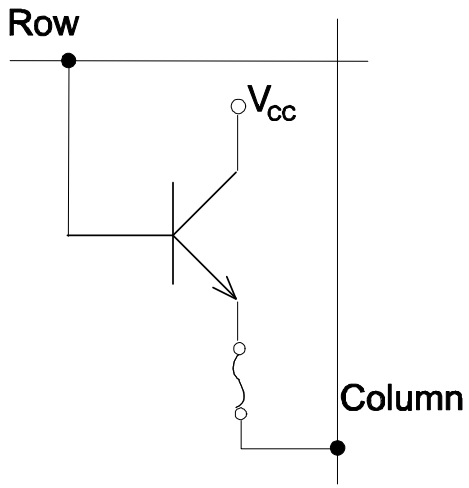


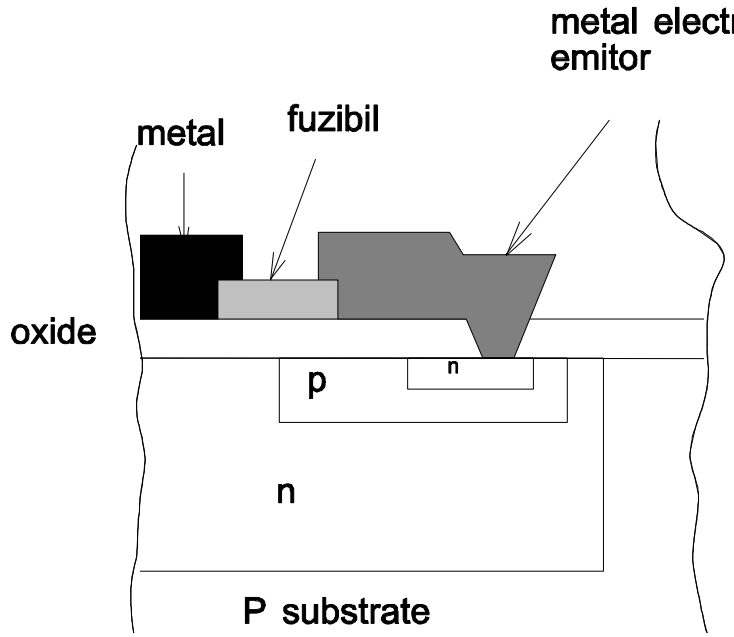
Programmable ROM circuits

- Two basic methods to program the memory cells:
- Each cell incorporates a metalic fuse at one of the electrodes. During the programming process, this metalic layer may (or not) be burnt if a high power pulse is applied for a determined period. Each possibility defines a possible logic state for the memory cell.
- Each cell has an electrode, initially not connected to structure. During programming, applying or not applying a current flow, an avalanche induced migration of carriers is generated (or not), having (or not) a conductive path from the structure to that electrode. This defines the possible state of that cell.

PROM memory with bipolar transistor

Layout and cross section of a PROM memory cell using a bipolar transistor.

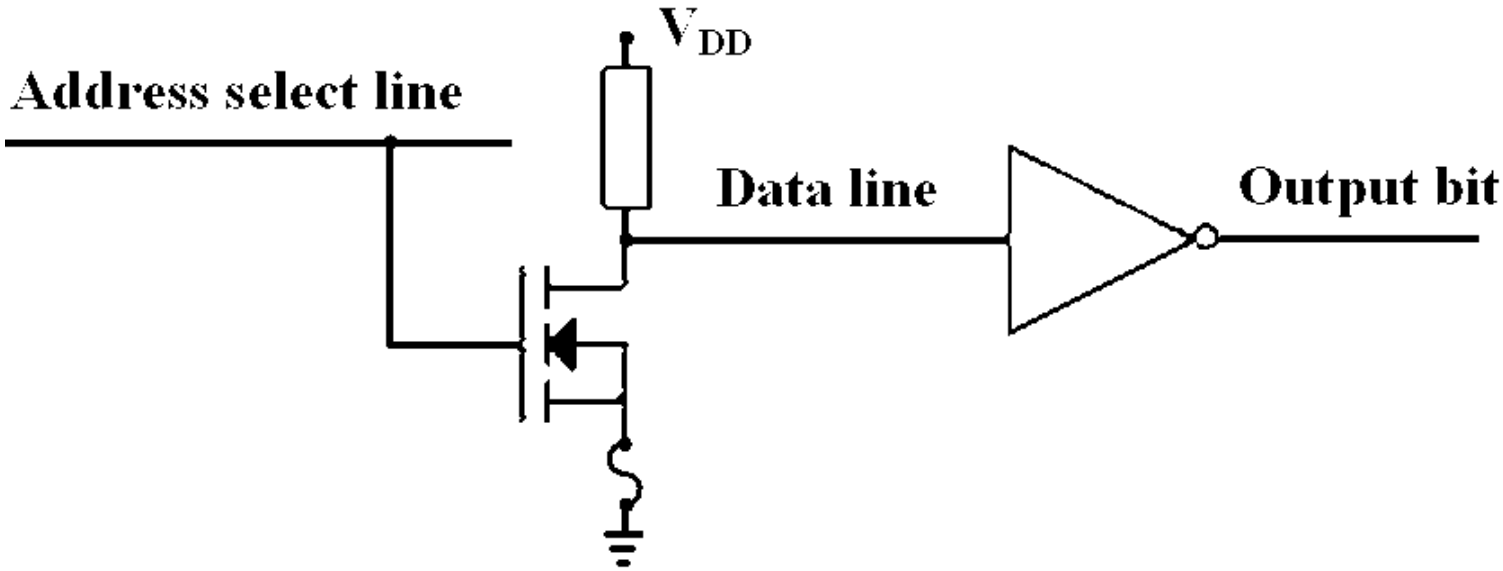




Transistor basis is connected at the line (array's row) selected by addressing, collector connected to power supply V_{CC}, and emitter is connected through fuse to array's column (data line). Fuse resistivity is controlled by the dopping process, so at an emitter current of 25mA, fuse is being burnt (pierced), and an insulator area appears making impossible to reconnect.

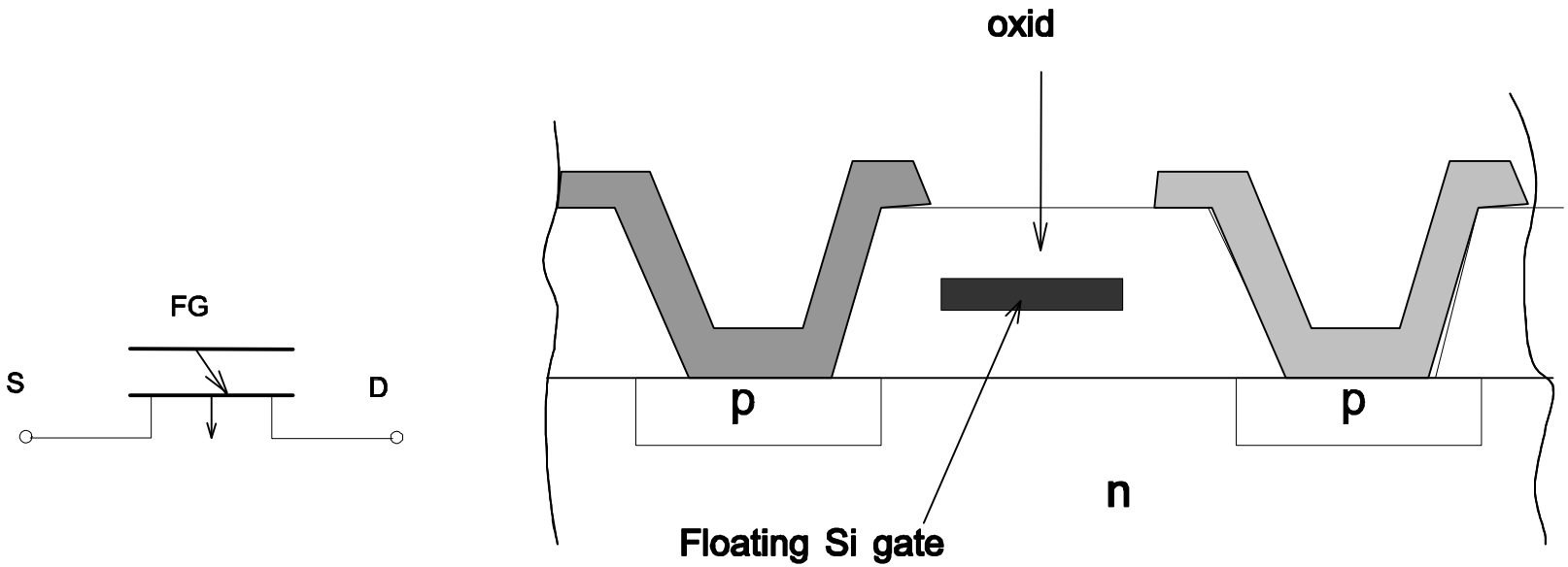
Conducting transistor implements a '1', and transistor off (burnt fuse) means '0'

PROM memory with MOS transistor



- Gate connected at horizontal selection line, drain connected at data line (vertical line in the array), and source connected at ground through fuse
- transistor on implements ‘1’, transistor off represents a ‘0’

REPROM memories

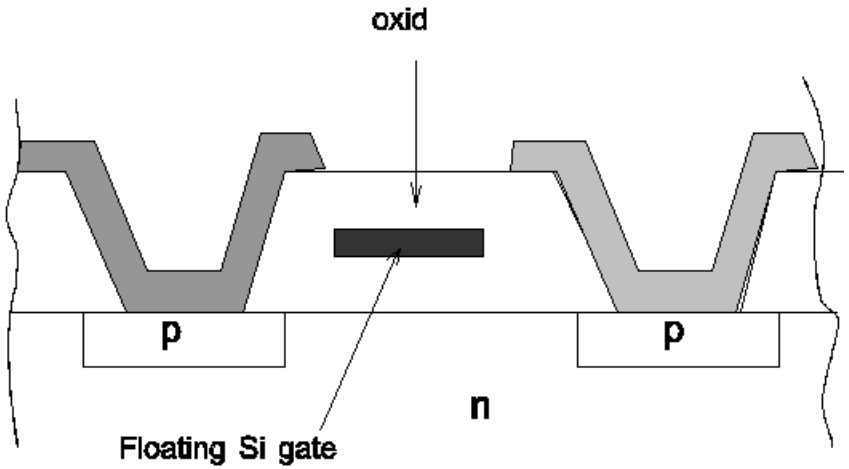


REPROM memory cell may be built up with a MOS device called *floating-gate avalanche-junction MOS charge-storage device*.

Figure represents floating gate p-channel device symbol and a cross section (REPROM cell)

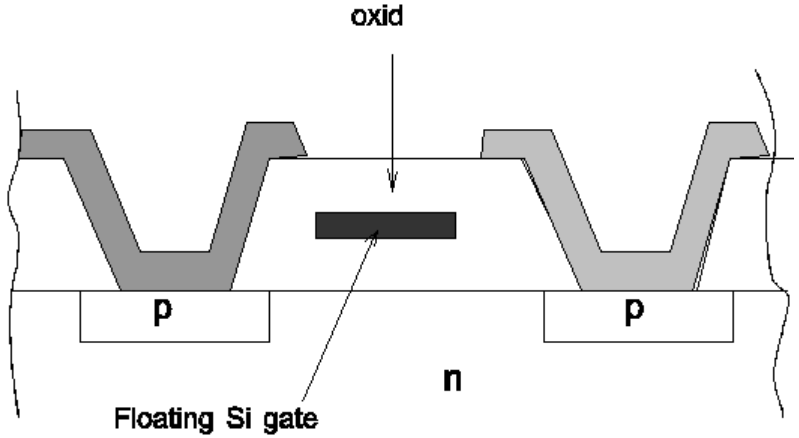
Initially there is no connection toward the silicon gate, it being insulated by a dioxide layer.

If from outside is applied for a determined period a negative electric field between drain and source electrodes, the drain-substrate junction will be strongly biased and will produce an avalanche of electrons from substrate toward the p-type drain



Part of these electrons will pierce (go through) the thin insulating layer between gate and substrate, bringing in gate a negative charge. When bias field is stopped, this stored charge will remain into gate, due to the insulating layer. So a reverse layer between source and drain is created, changing the state of conductivity between source and drain. Charge accumulation into gate means ‘0’, and charge absence means ‘1’. Electron leakage from gate to substrate (in time) is a slow process, so accuracy of stored info is guaranteed for years.

Info erase process may be:



X rays based (Ultra Violet Erasable PROM). Memory integrated circuit presents a quartz window, so exposing circuit at a UV light source, a photo-current is generated, discharging the floating gate of the negative charge. Number of erasing operations is bounded, because the UV rays influence the crystal structure.

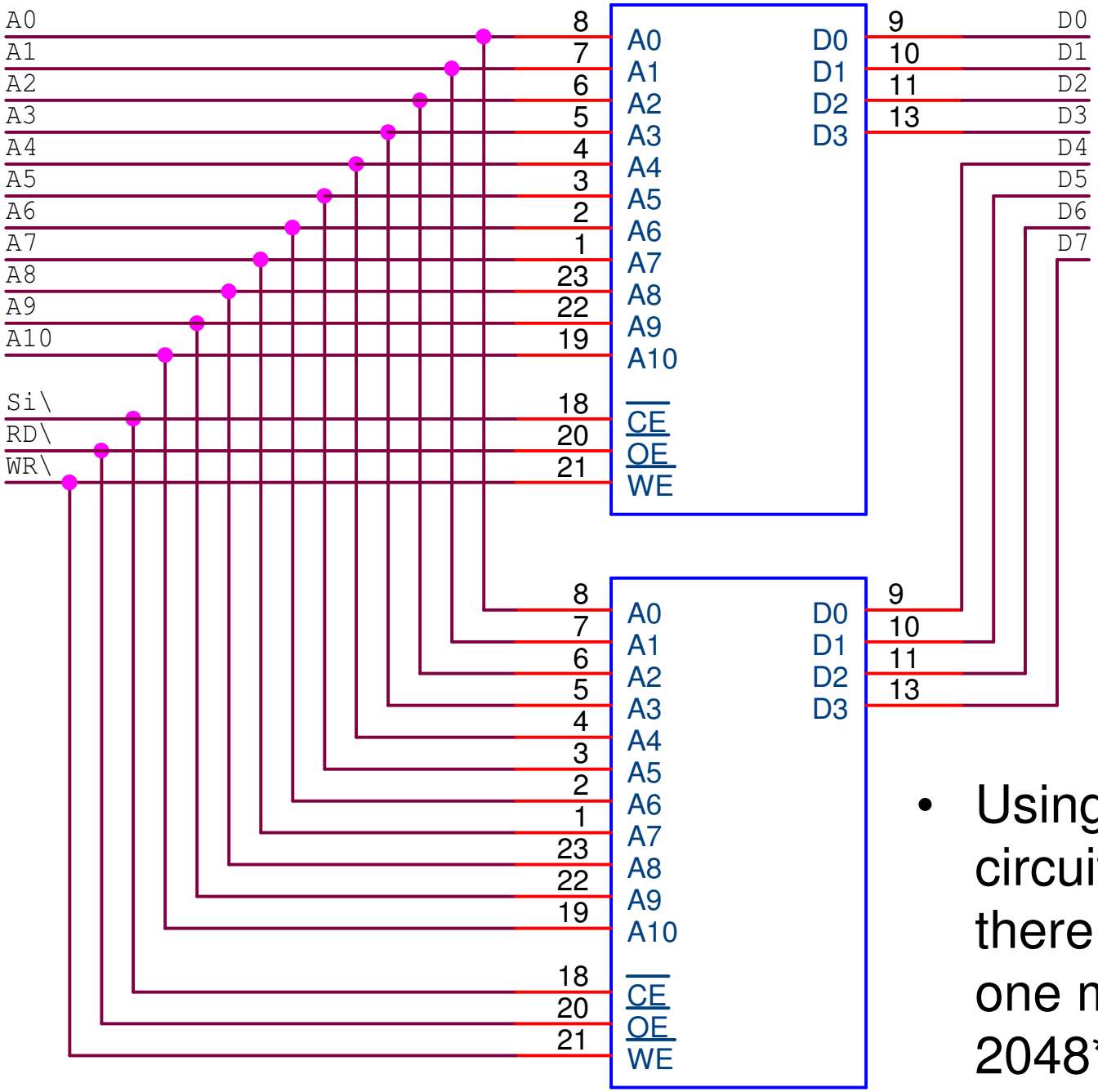
Electric erasable REPROM (called EEPROM), caracterized by an additional metalic layer (a second gate), above the floating gate. When programming, applying a positive potential here, more electrons will be accumulated. For erasing, at this second gate a negative potential is applied, generating positive carriers which will combine with the existing electrons, discharging flaoting gate.

Proposed Problems

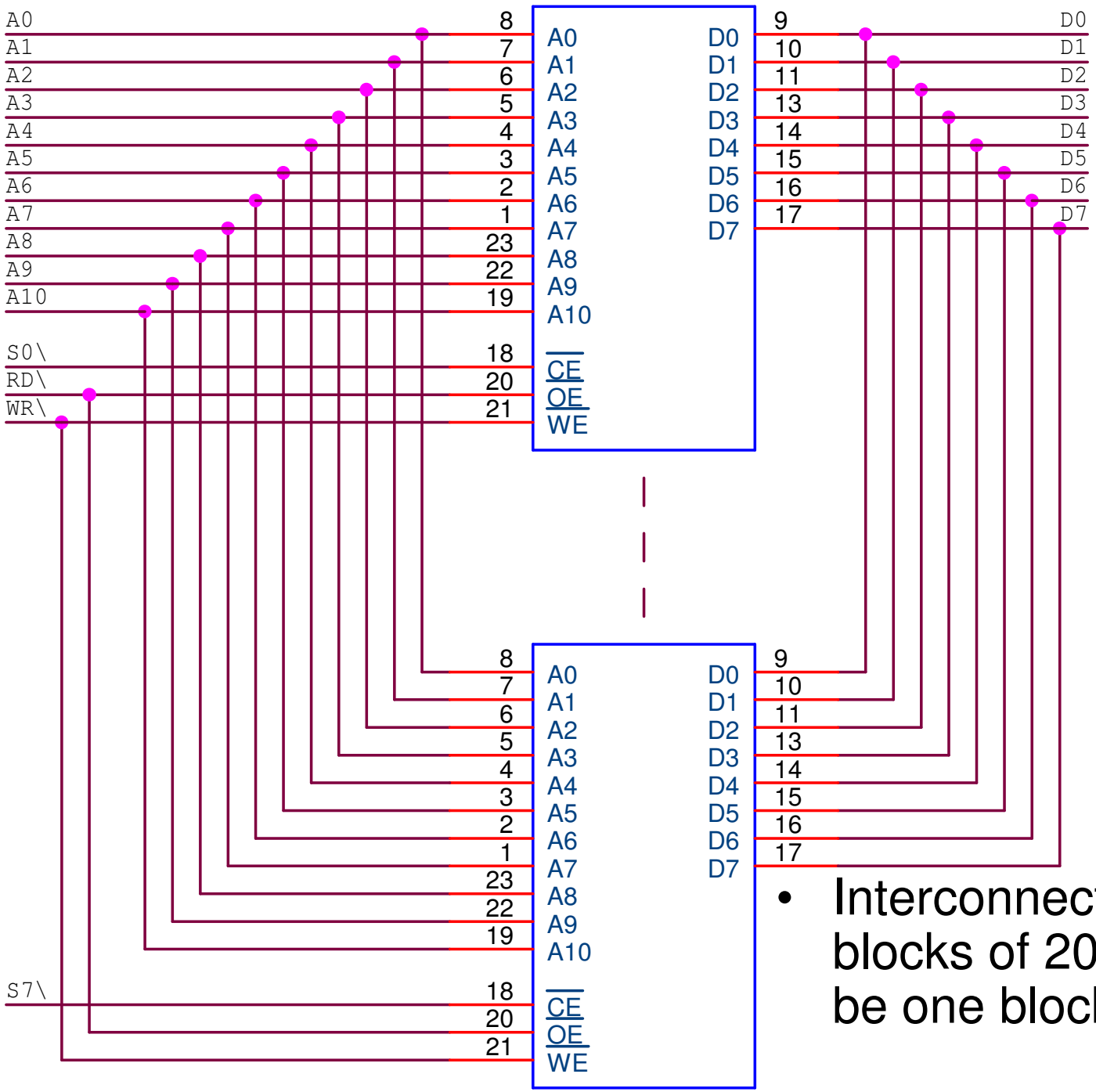
Design a SRAM memory block with the following characteristics:

- Storage capacity: 16384*8 bits
- structure: 8 bits
- Low address: C000H
- Memory circuit capacity: 2048*4
- System buses: 16 lines address bus, 8 lines data bus, RD\, WR\

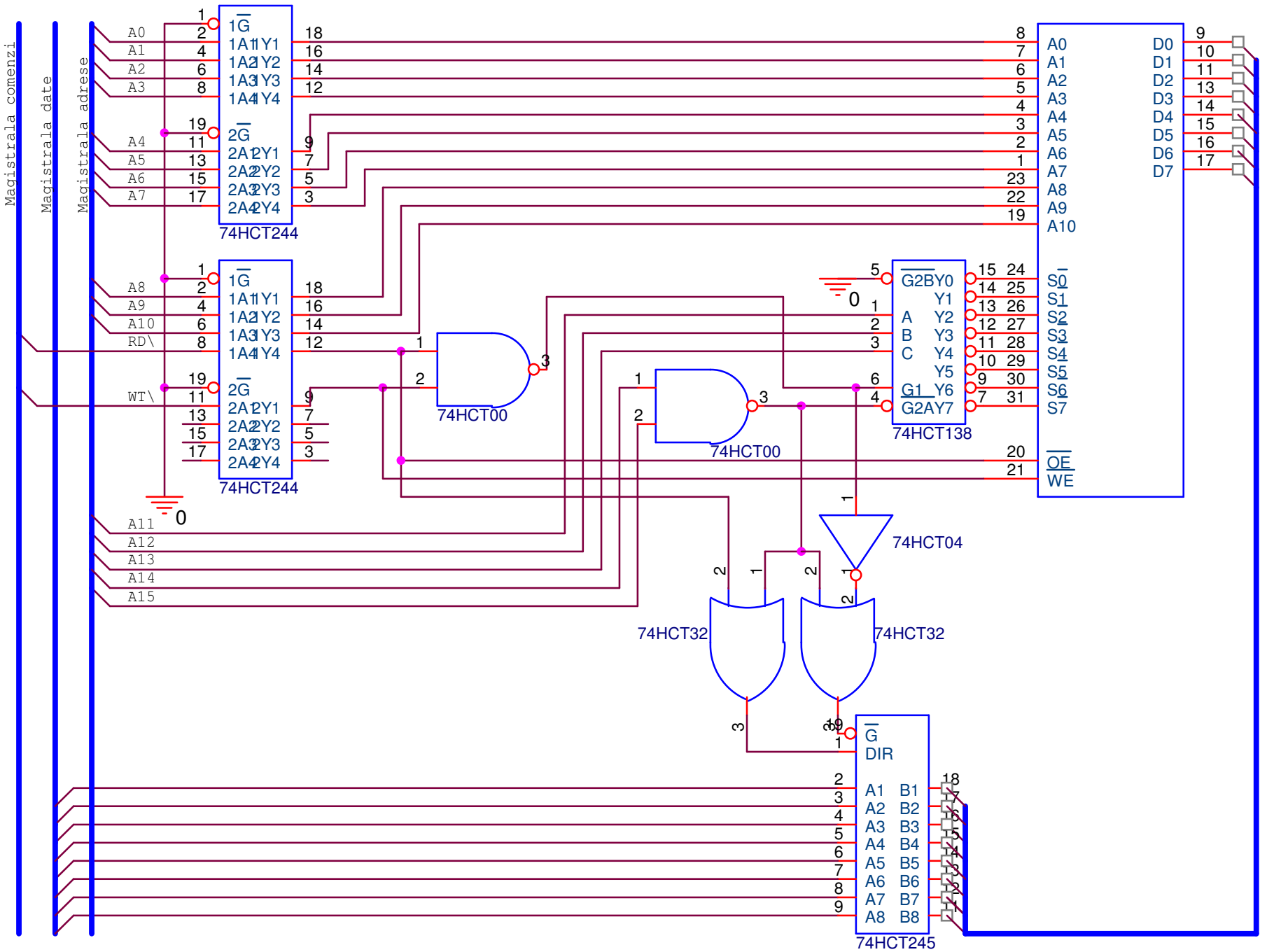
Memory block adds a HCT load to the system's bus



- Using two memory circuits of 2048*4, there will be obtained one memory block of 2048*8



- Interconnecting 8 memory blocks of 2048*8 there will be one block of 16384*8


Magistrala comenzi
Magistrala date
Magistrala adrese
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
RD\
WT\
A11
A12
A13
A14
A15
1G
2G
1A1
1A2
1A3
1A4
2A1
2A2
2A3
2A4
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
2Y3
2Y4
74HCT244
74HCT244
74HCT00
74HCT00
G2BY0
A
B
C
G1
G2AY7
Y1
Y2
Y3
Y4
Y5
Y6
74HCT138
74HCT04
74HCT32
74HCT32
G
DIR
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
74HCT245
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
S0
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S2
S3
S4
S5
S6
S7
OE
WE
D0
D1
D2
D3
D4
D5
D6
D7

Design a SRAM memory block with the following characteristics:

- Storage capacity: 32768*16 bits
- structure: 16 bits
- Low address: 8000H
- Memory circuit capacity: 4096*4
- System buses: 16 lines address bus, 16 lines data bus, RD\, WR\

Memory block adds a HCT load to the system's bus