CMOS Logic Integrated Circuits

Introduction

CMOS Inverter

Parameters of CMOS circuits

Circuits for protection

Output stage for CMOS circuits

Buffering circuits

Introduction

- Symetrical and complementary metal-oxide-semiconductor structures
- Present parameter values close to ideal ones
- Reduced power dissipation (100 nW in static regime, per gate)
- Broad range for power supply voltage: 3-15V sau 3-18V and less (for future)
- Huge fan-out (over 100 in static regime)
- in dynamic regime, because each CMOS input presents a 5pF load capacity, there is a trade-off between delay (speed) and number of driven loads
- Broad range of allowed ambiental temperatures (-40˚C ÷ +85˚C)
- Output voltage levels very close to 0V for logic '0' state, and respectively close to power supply voltage for logic '1'

CMOS Inverter
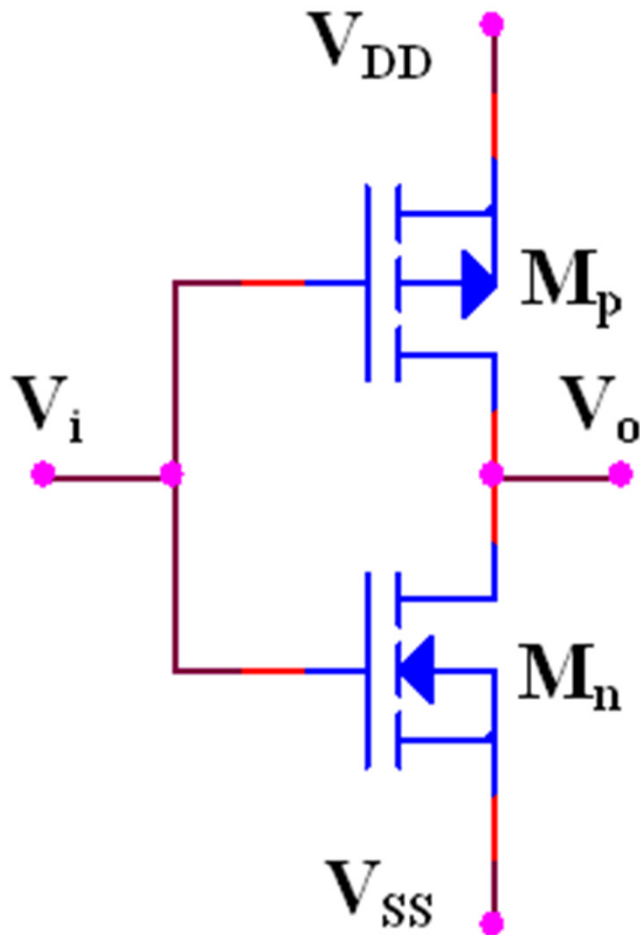
- Pair of MOS transistors, one with **n** channel and one with **p** chnnel

- $V_i = V_{DD} = $ '1', M_n open, M_p off, $V_o = V_{SS} = $ '0'

- $V_i = V_{SS} = $ '0', M_n off and M_p open, $V_o = V_{DD} = $ '1'

Static Transfer Characteristic
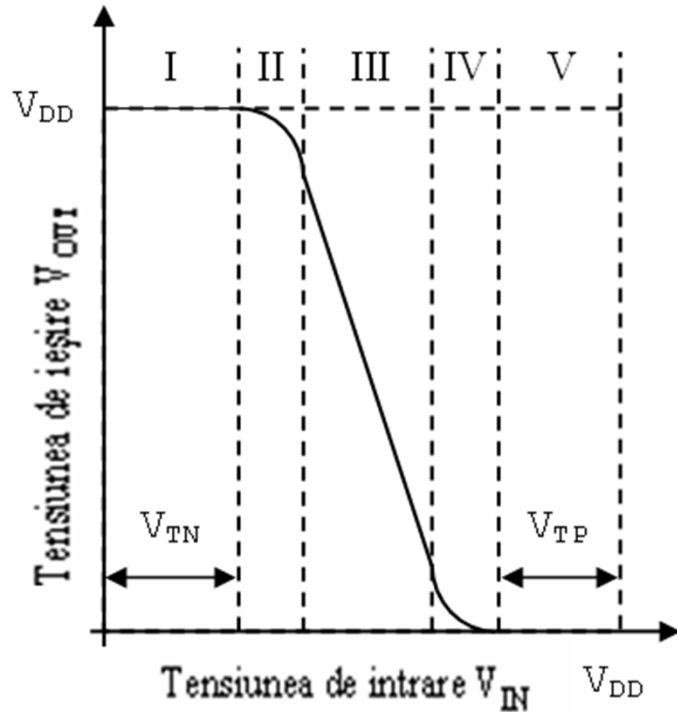
- depends on power supply V_{DD}
- Five operation regions
- V_{TN} threshold voltage for M_n
- V_{TP} threshold voltage for M_p

| TENSIUNEA DE INTRARE V_{IN}	REGIUNEA	M_P	M_N
$0 \leq V_{IN} \leq V_{TN}$	I	LINIAR	BLOCAT
$V_{OUT} - \lvert V_{TP} \rvert \geq V_{IN} \geq V_{TN}$	II	LINIAR	SATURAT
$V_{OUT} - \lvert V_{TP} \rvert \leq V_{IN} \leq V_{OUT} + V_{TN}$	III	SATURAT	SATURAT
$V_{OUT} + V_{TN} \lvert \leq V_{IN} \leq V_{DD} - \lvert V_{TP} \rvert$	IV	SATURAT	LINIAR
$V_{DD} - \lvert V_{TP} \rvert \leq V_{IN} \leq V_{DD}$	V	BLOCAT	LINIAR

Minimum power supply voltage
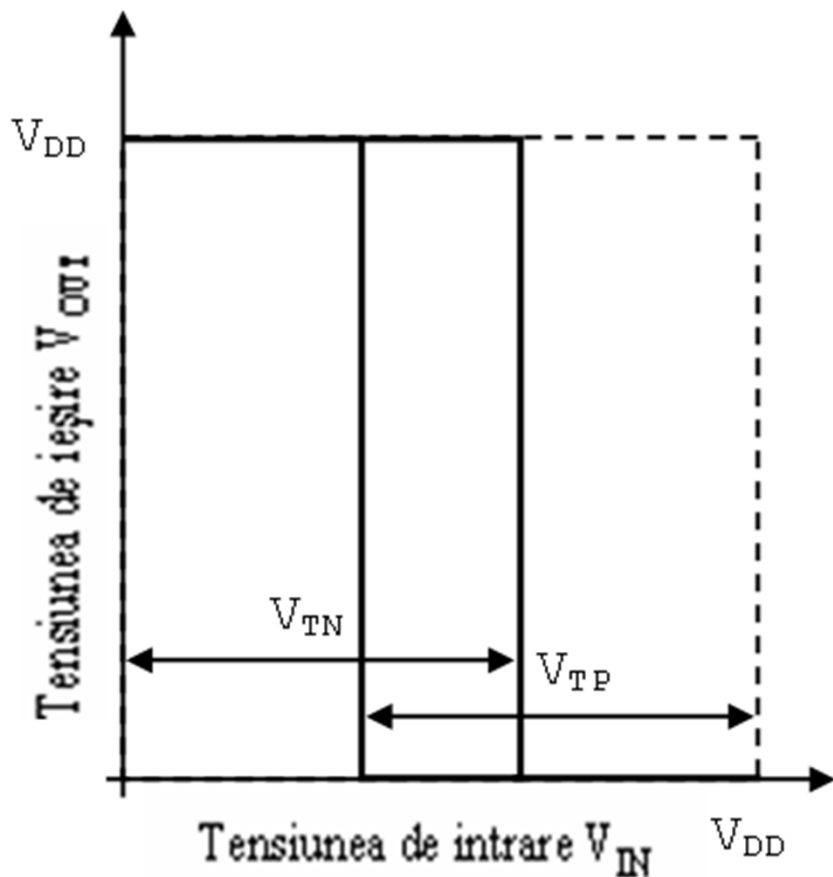
- If V_{DD} lower than: $V_{DDmin}=V_{Tn}+|V_{Tp}|$, inverter will present a hysteresis like transfer characteristic and the gate will NOT behave as a logic gate

- Typical threshold voltage value for standard CMOS: $V_{Tn} = |V_{Tp}| = 1{,}5V$

- $V_{DDmin}=3V$

Voltage Levels and Noise Margins

- $V_{0Hmin}=V_{DD}-0.5V$ (typical: $V_{DD}-0.01V$)
- $V_{0Lmax}=0.05V$ (typical: $0.01V$)
- $V_{IHmin}=70\%V_{DD}$
- $V_{ILmax}=30\%V_{DD}$
- $M_{ZL}=V_{ILmax}-V_{OLmax}=30\%V_{DD}$
- $M_{ZH}=V_{OHmin}-V_{IHmin}=30\%V_{DD}$
- Practically, noise immunity is 45…50% from power supply voltage

Circuit Response at an Ideal Pulse
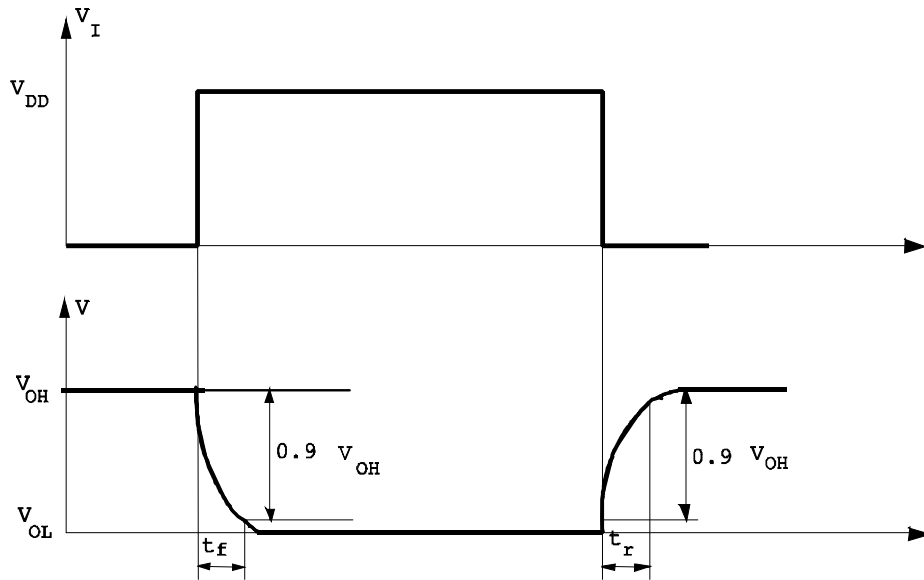
- Circuit has a load capacitance C_S
- t_f and t_r : duration of fall down and raise-up edges for output

- Factors influencing the switching speed:
  - Power supply voltage
  - Circuit configuration (with or without separation circuits for outputs)
  - technology
  - Load capacitances

Power Dissipation

- In static regime, one out of two transistors are off; no power consumption, exept due to stray currents flowing through megaohms resistors (resistance equivalent to blocked transistors)

- During the dynamic regime, each transition will increase consumption, due to:
  - Both complementary MOS transistors are in conduction
  - Parasitic capacitances from circuit's output present charge/discharge cycles

Power Dissipation

- $P_t = P_{cc} + P_{dc} + P_{df}$
- P_{cc} means static power, dissiped by circuit during a steady state, and is due to residual (stray) currents of a locked transistor
- P_{dc} means dynamic power, due to charge/discharge process of parasitic output capacitances
- P_{df} means dynamic power dissiped during transistions, on raising and falling edges, when both transistors are in transitory states
- P_{cc}, is small (nW), because the stray currents are small; they depend on the power supply and temperature (double for any 10 Cgrades)
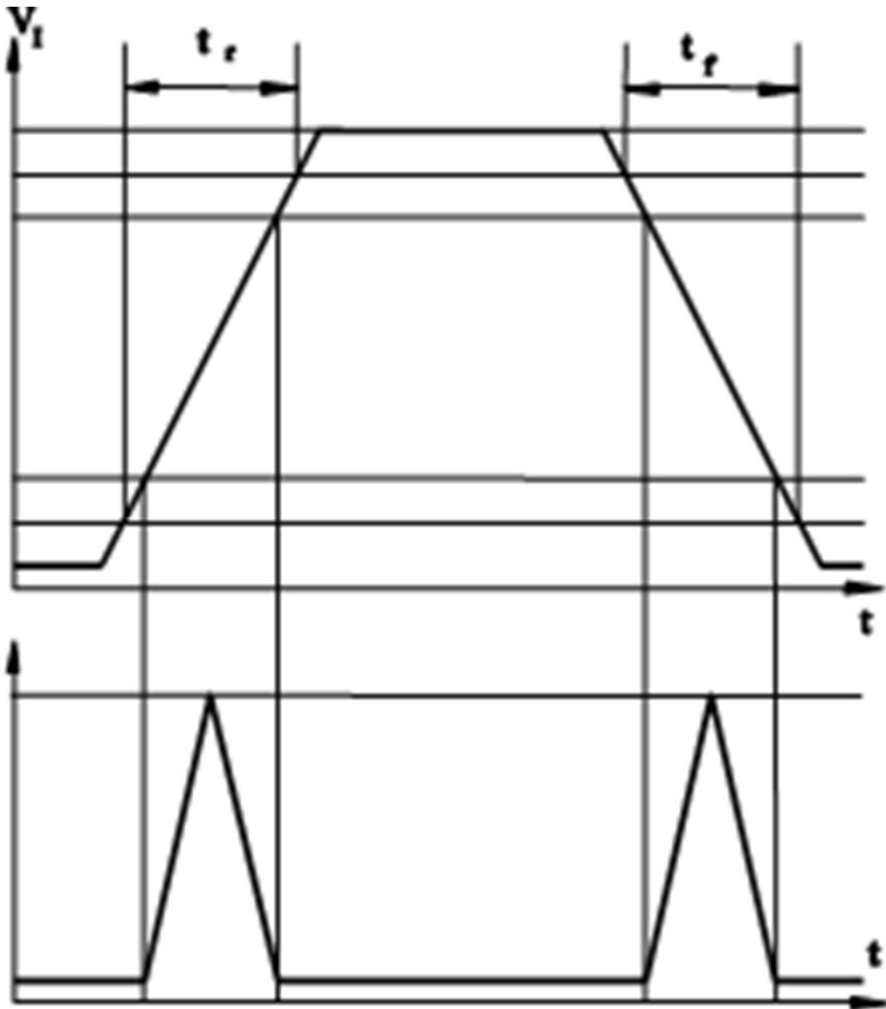
Power Dissipation

$$P_{df} = V_{DD} \cdot \frac{1}{2} \cdot I_{DDmax} \cdot \frac{Durata\ frontului}{Perioada\ semnal}$$

I_{DDmax} current due to circuit switching, not considering the charge/discharge currents on parasitic capacitances

Transistors are on simultaneously during a time period given by moments when signal varies between V_T and V_{DD}-V_T, where V_T is the threshold voltage:

$$\frac{Durata\ frontului}{Perioada\ semnal} = \frac{V_{DD} - 2 \cdot V_T}{V_{DD}} \cdot \frac{t_r + t_f}{T}$$

$$P_{dc} = \frac{C_{PD} * V_{DD}^2}{T} = C_{PD} \cdot V_{DD}^2 \cdot f$$

Power Dissipation

- For a simpler calculus, P_{df} may be considered equal with power absorbed during charge/discharge process of an equivalent capacitance C_{PD}, being summed with the parasitic capacitance from the circuit output, i.e.:

$$P_t = C_{sarcina} \cdot V_{DD}^2 \cdot f + C_{PD} \cdot V_{DD}^2 \cdot f + P_{CC} = (C_{PD} + C_{sarcina}) \cdot V_{DD}^2 \cdot f + I_{rezidual} \cdot V_{DD}$$

- dynamic power-dissipation capacitance, defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance: C_{PD} taken from data book

- $C_{sarcina}$ represents the external (load) capacitance

Fan-in, Fan-out

High input impedance, low input current (10pA)

One important component of input current is given by the charging/discharging process for CMOS structures input capacitances; during switching the static input capacitance (typical 5pF) is enhanced 5 to 10 times, due to reactions through parasitic capacitances

I_{OL}=0,44mA, I_{OH}= -0,5mA for V_{DD}=5V; I_{OL}=0,9 mA, I_{OH}=-0,9 mA for V_{DD}=10V

Output currents may drive many similar CMOS gates.

Because of capacitive load, depending on number of driven gates, and this affecting performance (propagation delay, power dissipation), in practice the fan-out value is bounded to 50

For each output the typical maximum capacitance is 8pF

When connecting a higher external capacitance (over 1μF), the peak of output currents may reach high values; recommended a maximum of 30mA for standard CMOS gates and 100mA for buffers at circuit outputs

Quality (merit) factor

- Quality factor, Q_f, defined as product between propagation delay and power dissipation, being expressed in pJ or in mW·ns
- Important element for performance estimation
- CMOS-SOS: 3 pJ; CMOS: 60 pJ; NMOS: 300pj; PMOS: 1000 pJ; TTL: 100pj; Schottky-TTL: 60pJ
- Quality factor depends on working frequency and power supply; worsening as power supply increases, due to V_{DD} that influences dynamic power dissipation

Circuits for protection

Because gate electrode is separated from basic substarte by a high resistance and the thickness of the insulating dioxide layer between gate and substrate is thin (less than 1000 Å) there is possibility for destroying the dioxide layer, when applying certain voltages (70-100V)

Electrostatic voltages from human body, manifesting at circuit terminals may have important values, more than allowed by input protection circuits; it may damage the input circuits

An option would be to insert a Zener diode (breackdown voltage of 25V), between V_{DD} and V_{SS} protecting circuit when power supply not applied

Due to this protection, when switching off CMOS based circuits, is compulsory to deactivate first the input signals and after the power voltage V_{DD}.

Contrarly, some power voltage amount is injected through diode on the power supply bar, damaging diode or other components or having a wrong power supply for CMOS components

CMOS circuits output specificity

May have different output impedances, function of number of connected inputs, and transfer characteristics are shifted

Transitions between steady states will not happen at around $V_{DD}/2$, but, as number of connected inputs grows, between $V_{DD}/2$ and V_{DD} (for NAND circuits) and between $V_{DD}/2$ and V_{SS} for NOR gates

Shift of transition level damages noise immunity for the far state and enhances the noise margins of the nearer state

For the short circuits at CMOS outputs, some are admitted

For longer periods the admitted value of short current may reach 10mA

For CMOS structures with output impedances more than 500Ω, at V_{DD}=5V it may be accepted short circuits

For short time intervals, CMOS circuits are self protected against current peaks by increasing drain-source resistance, as a result of increasing the applied voltage for that channel; power dissipation is increasing too, may damage circuit; that's why for V_{DD}>5V is recommended to avoid short-circuits at CMOS outputs

Buffer circuits

For avoiding arising problems with serial or parallel connection of transistors within the output stages of various CMOS circuits, special buffer circuits are inserted at outputs and sometimes at circuit inputs. These circuits are essentially inverters, allowing for a separation of the output/input circuits from the rest of layout circuits.

The output buffers provide firm signals, not depending on the next driven input number, keep transition region within standard limits; also same for noise margins.

At circuit input, buffer circuits impose a better noise immunity and lower values for input capacitances.

As a drawback of using suplementary buffer circuits for input/output stages there is a higher propagation delay. Despite this, the allowed operating speed isn't suffering, because the output buffer allows for a lower output impedance, and for independance on number of driven inputs; it means a faster speed for charge/discharge process of load capacitances; same for input capacitances, being lower due to the new input buffer circuit

HCT Logic Circuits
High-speed CMOS TTL compatible

Power Supply

$V_{CC}=4,5V \div 5,5V$

Voltage levels

$V_{OHmin}=V_{CC}-0,1V$
$V_{OLmax}=0,1V$
$V_{IHmin}=2V$
$V_{ILmax}=0,8V$

Noise Immunity

$V_{CC}=4,5V$
$M_H=V_{OHmin}-V_{IHmin}=2,4V$
$M_L=V_{ILmax}-V_{OLmax}=0,7V$

Input/output currents

$I_{OH} = I_{OL} = 4mA$

I_{IH}, I_{IL} – negligible (≈10pA)

Fan-out/Fan-in

As for CMOS circuits, HCT gate output currents are able to drive a lot of similar circuits

Practically, fan-out is bounded, to keep a high value for the cut-off (maximum) operating frequency

One HCT gate may drive maximum 2 TTL gates

Propagation Times

$t_{pHL} = t_{pLH} = t_{pd} = 7ns$

Static Power Dissipation

$P_{cc} ≈ 10nW$

Proposed Problems

- How many 74 series TTL gates may be driven using a HCT gate?
- What is the maximum value for the resistor mounted between two CMOS gates without modifuing the circuit behaviour? Is this affecting the noise immunity?
- Design a circuit using CMOS gate to drive a LED. Following values are considered for this LED:

V_{LED}=1,6V and I_{LED}=20mA.

Building a Bus Using Logic Circuits

- Introduction
- Open Collector Logic Circuits
- Three State Logic
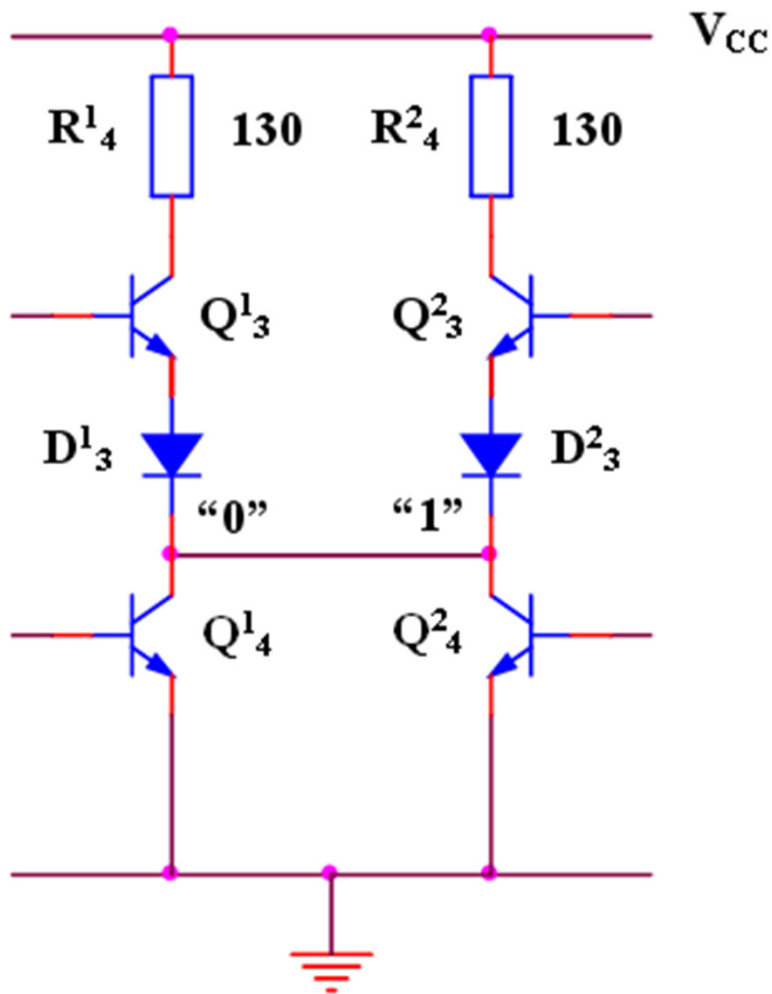
Introduction

Use of normal TTL or MOS logic circuits present drawback: to NOT allow the cabled AND function, i.e. the connection of all outputs together for achieving the AND logic function.

Important issue for building up numeric systems: design of system buses

See figure left: two standard TTL NAND gates have outputs connected together in parallel

If both outputs are simultaneously "0" or "1" circuit is well operating

If one output is "0" and the other "1", practically transistor Q_3^2 is tied to ground, current through it being limitedby diode D_3^2 and resistance R_4^2 (of 130Ω). It involves a huge power dissipation on transistors Q_4^1 şi Q_3^2 and through R_4^2.

Gate parameters are modifying or transistors are damaged by thermal excitement

In figure (circuit diagram):
R_4^1 130 R_4^2 130 V_{CC}
Q_3^1 Q_3^2
D_3^1 D_3^2
"0"   "1"
Q_4^1 Q_4^2

If outputs of two MOS gates are connected in parallel, for one output '1' and the other '0', the output voltage level is given by the voltage divider achieved by transistors with **n** channel and **p** channel being simultaneously in conduction
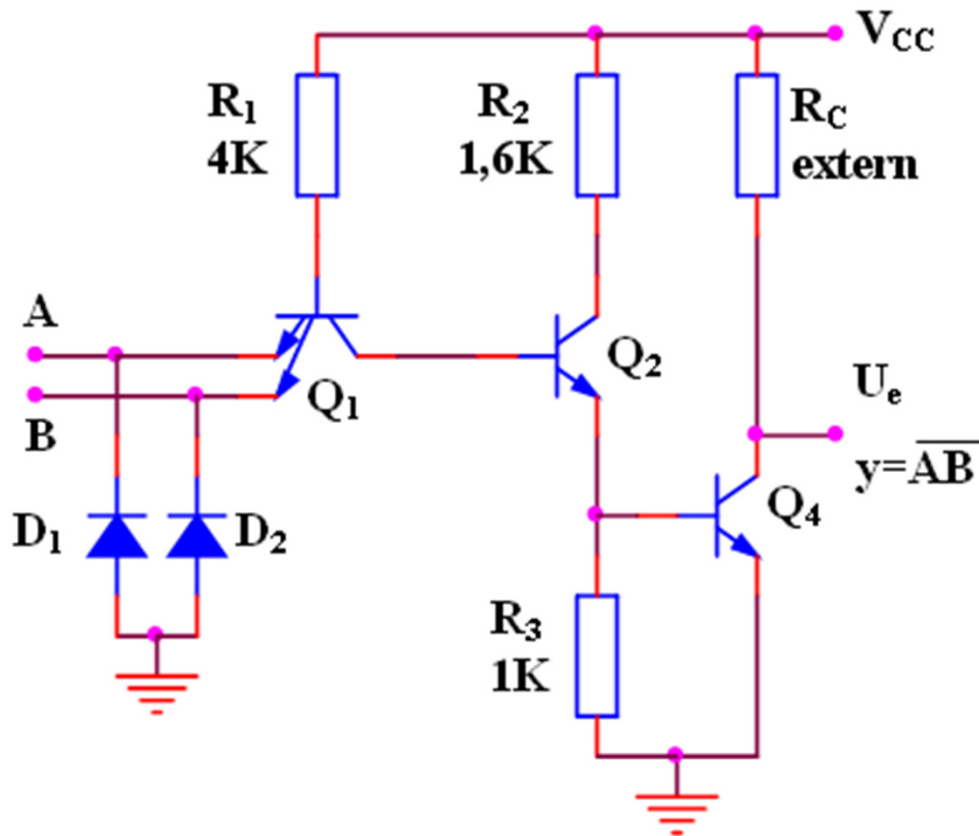
For coupling more gates in parallel, special circuits are used, like:

    open collector circuits

    open drain circuits

    three state circuits

TTL Gate with Open Collector

Open collector TTL gate has similar structure with standard TTL for input stage and medium stage (driving transistor Q_2); Output stage keeps only transistor Q4

Collectors of Q4 transistors from different gates may be tied together, the common connection being tied to power supply using a common external resistance

Power supply voltage may present different values, not only 5V, making possible to generate at outputs other logic levels for '1'

Common external resistance R_C isn't an integrated one, but is designed as a function of number of TTL gates connected together and number of inputs to be driven by this common output

A great value for R_C reduces power dissipation but affects propagation delay and noise immunity

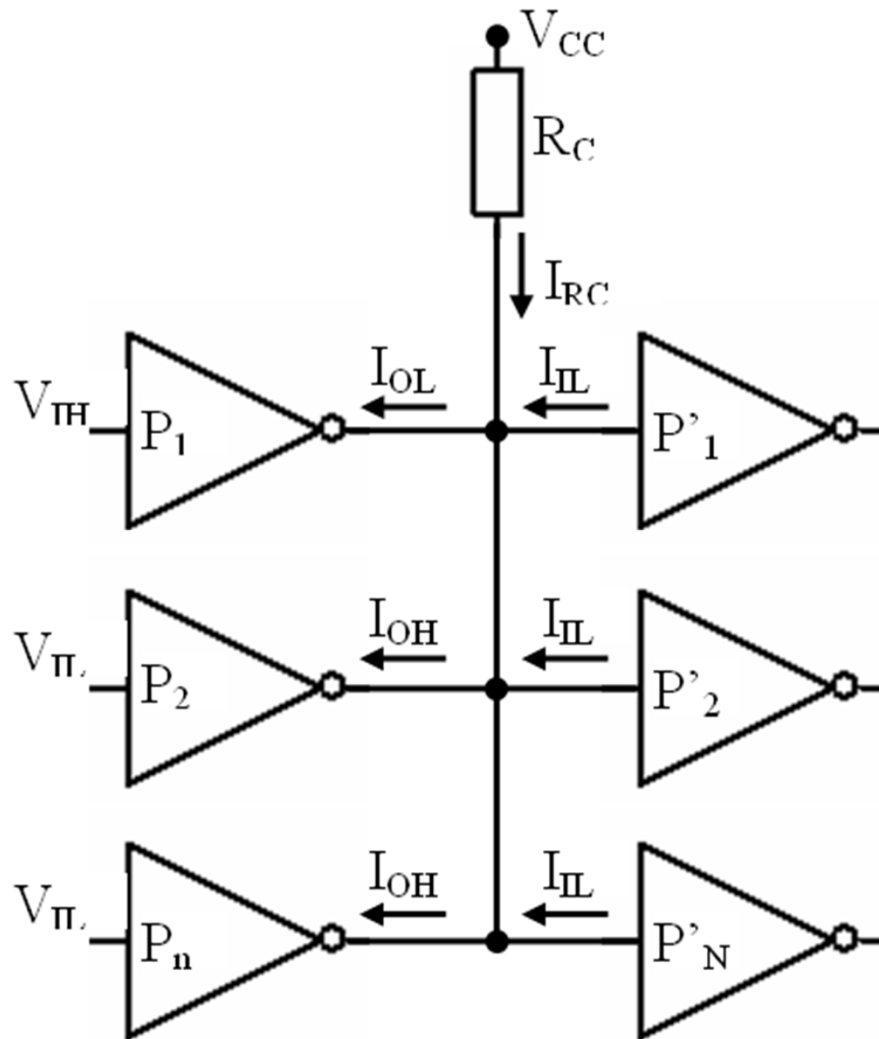There is a trade-off between designed power dissipation and delay

Calculus of R_C
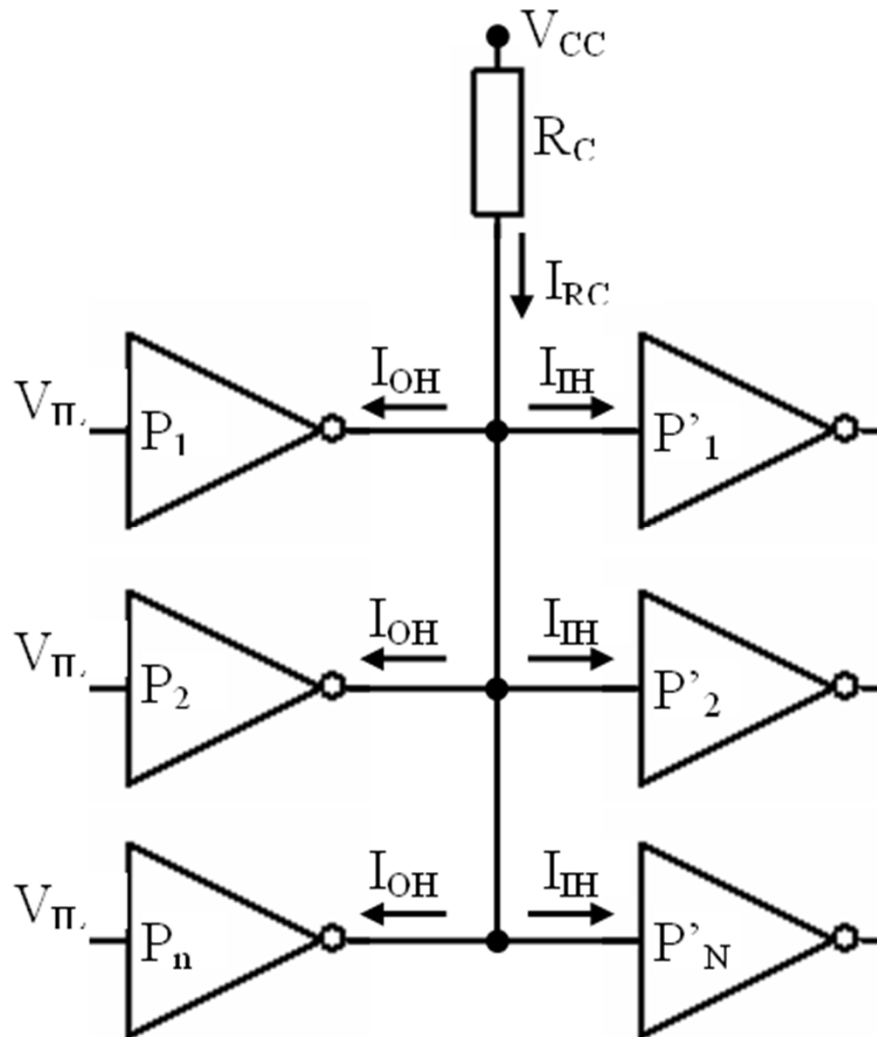
- Function of logic level from common output, sunk (output) currents of connected gates and source (input) currents of driven gates

- For '1' logic there will be:

$$R_{c\,max} = \frac{V_{cc\,min} - V_{OH\,min}}{n \bullet I_{OH} + N \bullet I_{IH}}$$

Calculus of R_C

- For '0' logic at output:

$$R_{c\,min} = \frac{V_{cc\,max} - V_{OL\,max}}{I_{OL} + (n-1)I_{OH} - N \bullet I_{IL}}$$

- $V_{CC} = 5V \pm 5\%$
- $I_{OH} = 250\mu A$
- $I_{OL} = 16mA$
- $I_{IL} = 1.6mA$
- $I_{IH} = 40\mu A$
- $V_{OH} = 2.4V$
- $V_{OL} = 0.4V$
- $P_D = 20mW$
- $t_{pd} = 13ns$
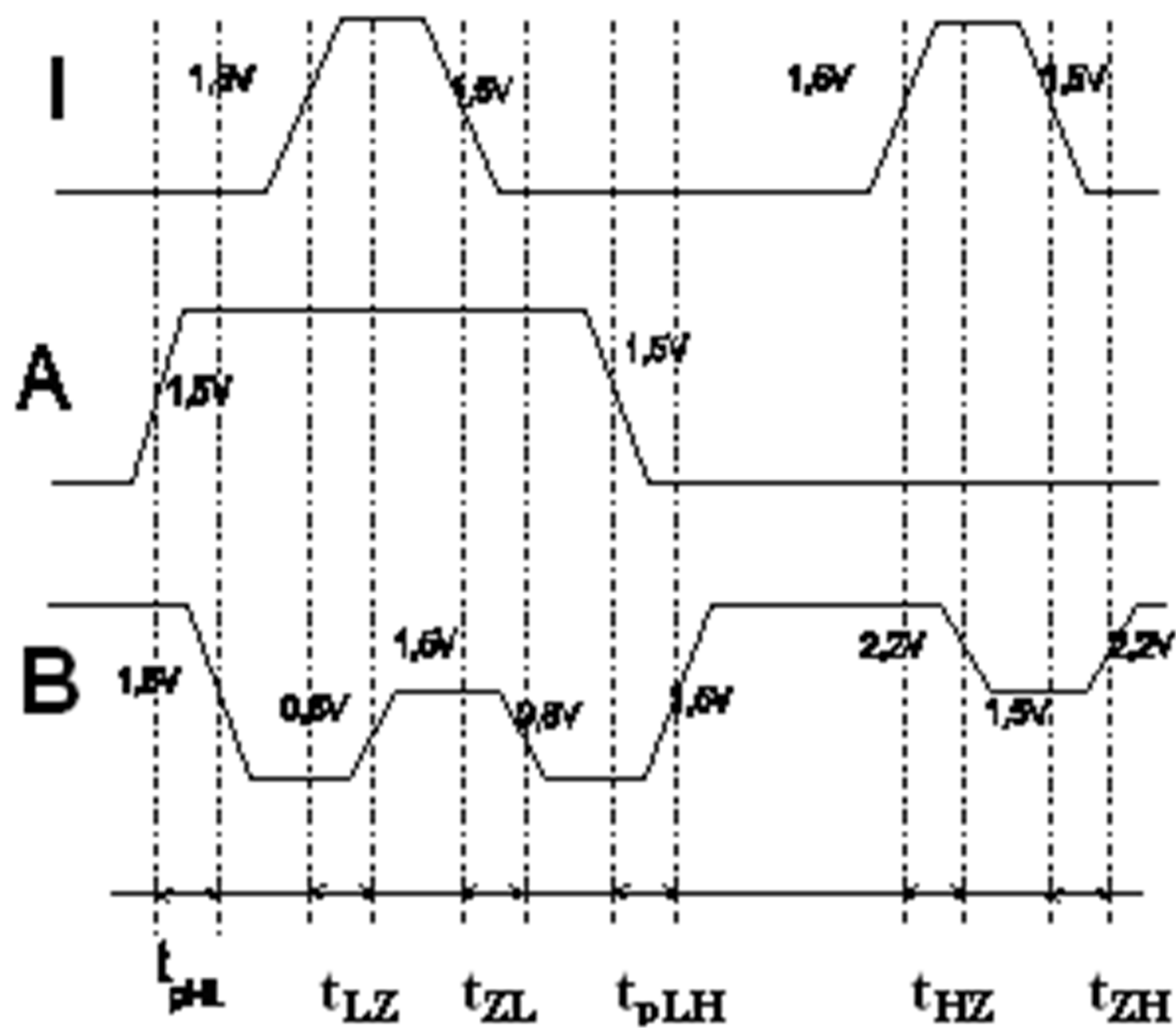
Three State TTL Logic Gates

- Both transistors of output circuit are locked
- Output circuit is separated
- From outside, TTL gate behaves as a high inpedance
- Circuit presents three states: "0", "1" and high-impedance state (state with both output tarnsistors off)
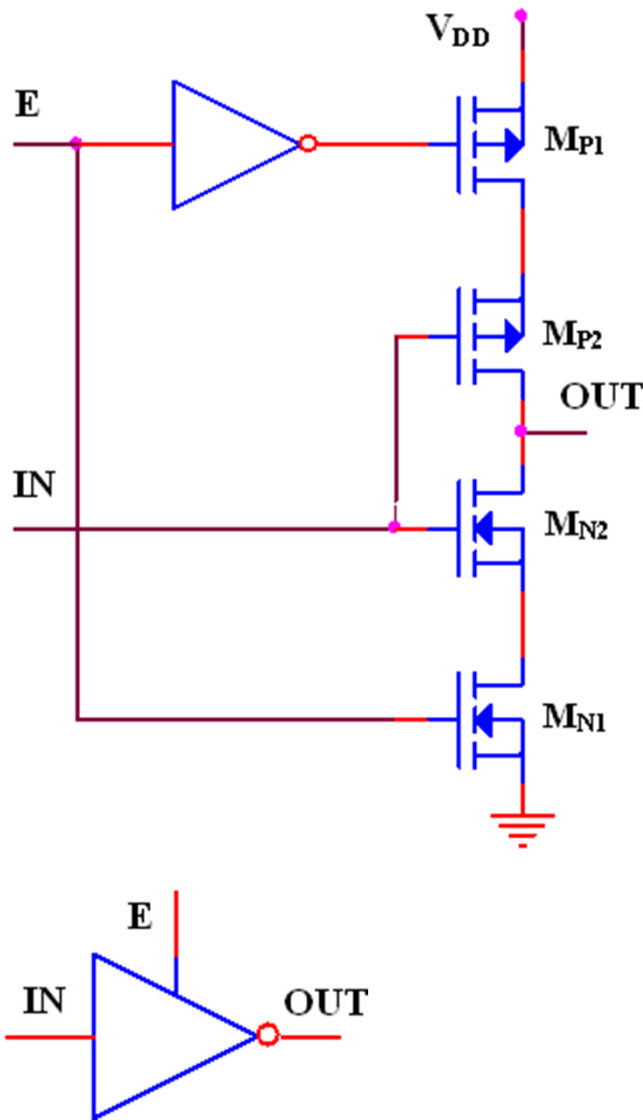
Three state Inverter
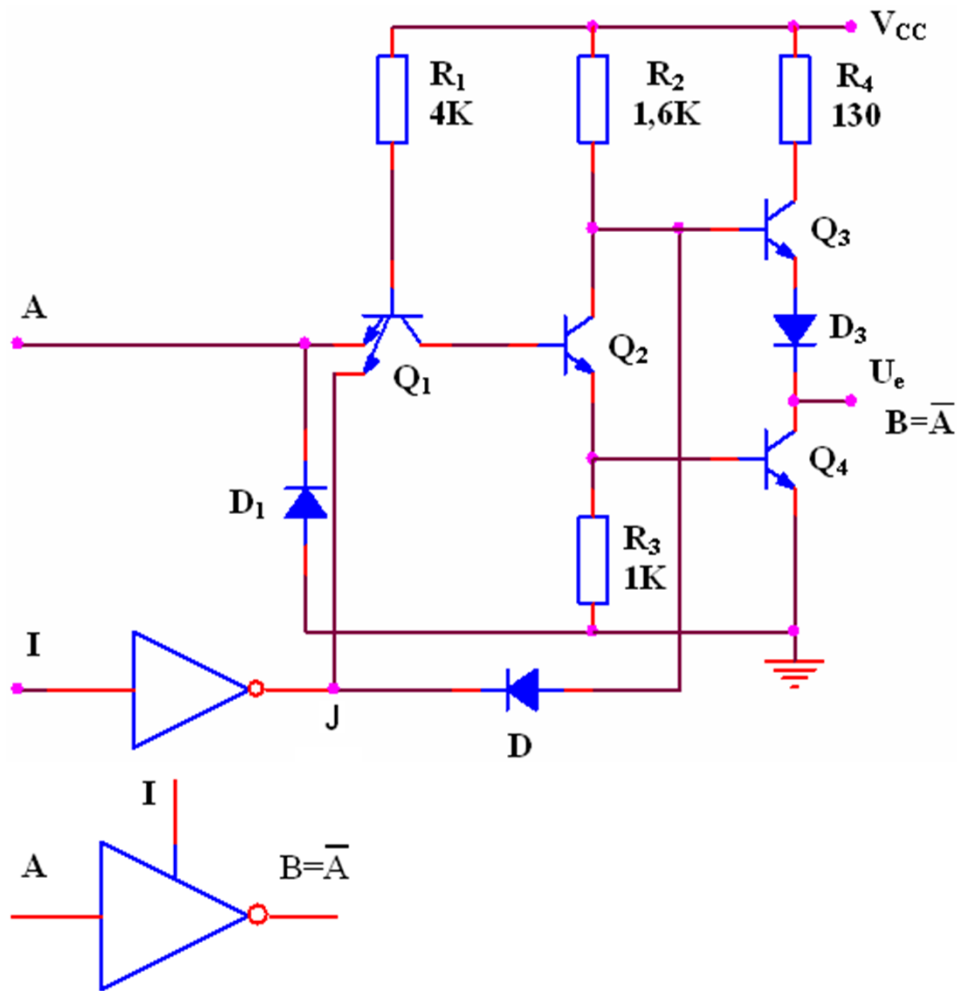
- I="0" – normal inverter, no influence
- I="1", J="0", D open, Q_1 saturated, Q_2 and Q_4 off, Q_3 off, because through open diode D its base potential drops at 0.7V
- Circuit will present at output a state of high impedance (HZ state)
- During dynamic regime, besides t_{pLH} and t_{pHL} there are more parameters:
- Establishment of HZ from "0", t_{LZ}, and from "1", t_{HZ}
- Get-out times from HZ to "0", t_{ZL}, respectively in "1", t_{ZH}

- Total propagation delay is approx. 25 ns: greater than standard TTL, but less than TTL open collector
- P_D=16mW

I

1,5V   1,5V   1,5V

A

1,5V   1,5V

B

1,5V   0,5V   1,5V   0,5V   1,5V   2,2V   1,5V   2,2V

t_{pHL} t_{LZ} t_{ZL} t_{pLH} t_{HZ} t_{ZH}

Three state MOS inverter

- Two **n** channel transistors and two **p** channel transistors
- One pair p-n transistors (denoted with 2) operates as standard inverter
- Second pair (denoted with 1) behaves as a switch (on/off), driven by input E (enable)
- If input E is "1", M_{N1} and M_{P1} are open and circuit output presents logic level given by normal input IN
- If input E is "0", M_{N1} and M_{P1} are off, and, no matter the input logic levels, the output presents high impedance state (higher than $10^{10}\Omega$ at 25°C).

Connecting circuits to buses

- A circuit connected at a bus presents a behavior of both receiver or sender (or is said that circuit is reading information from bus, and is writing info on that bus)
- There is need for a command signal RD to read info from processor and put it onto bus, and a write signal WR to put info from bus into circuit

When bus is idle (no activity) all connected lines are tied through a pull-up resistance to a high potential (usual power supply). If only TTL lines connected, instead of pull up resistance there are used bus terminators (mounted at end of bus, to avoid reflections)