Monostables

Astables

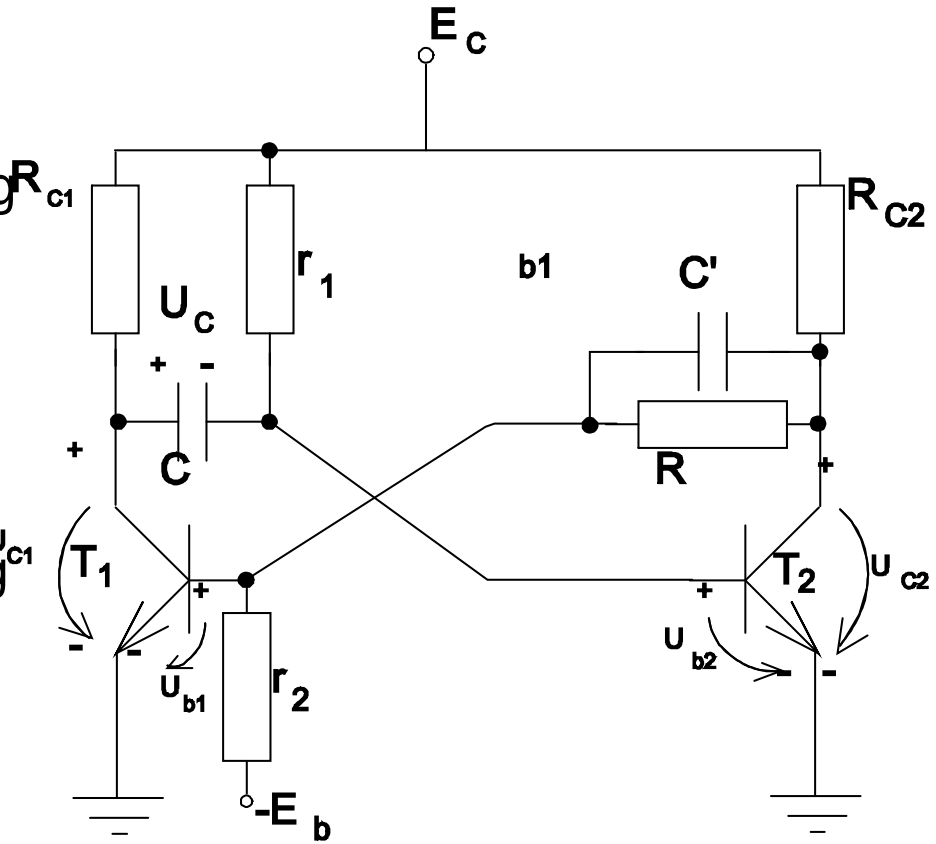
Monostables

Monostable switching circuits (MSC) present a stable and an unstable state; are used especially for obtaining some fixed time intervals, precisely marked by voltage swings

Most important condition for these circuits is the **duration** for the unstable state

Collector-base Coupled MSC

Positive reaction is assured by coupling circuits, but at MSC the resistive coupling between the collector of T_1 and the base of T_2 is replaced by a capacitive coupling.
The different nature of states is due to the asymmetry of the coupling



Stable state: the transistor T_1 is cut off, because its base is connected through r_2 to $-E_B$, and the transistor T_2 is saturated, because its base is connected trough r_1 to E_C.

The condition that T_1 be cut off can be written analogically with CBB: $r_2 \le \frac{E_B}{I_{C0\max}}$

Condition for T_2 to be saturated is: $\beta_{\min} I_{B2} \ge I_{C2}$ or

$\beta_{\min} \frac{E_C}{r_1} \ge \frac{E_C}{R_{C2}}$ resulting value: $r_1 \le \beta_{\min} R_{C2}$

Voltage fall on the capacitor C, U_C will be for this sable state $\approx E_C$

Unstable state:

By applying a negative pulse on the base of the transistor T_2, it is initialized a switching process, which can be described like this:

- the voltage U_{B2} decreases
- the collector current I_{C2} decreases
- the potential in the collector of T_2 (U_{C2}) increases, same for the potential U_{B1}
- the collector current I_{C1} increases
- the potential in the collector of T_1, U_{C1}, decreases, same as U_{B2}

In this way the circuit passes to the opposite state:

T_1 is saturated and T_2 is cut off

Due to the fast fall down of the voltage U_{C1} from E_C to approximately 0V, it will make the capacitor C to transmit a negative voltage swing, of amplitude E_C, to the base of T_2

After this transition: $U_{C1}(t_1) \approx 0$, $U_{C2}(t_1) \approx \frac{R}{R + R_{C2}} E_C$

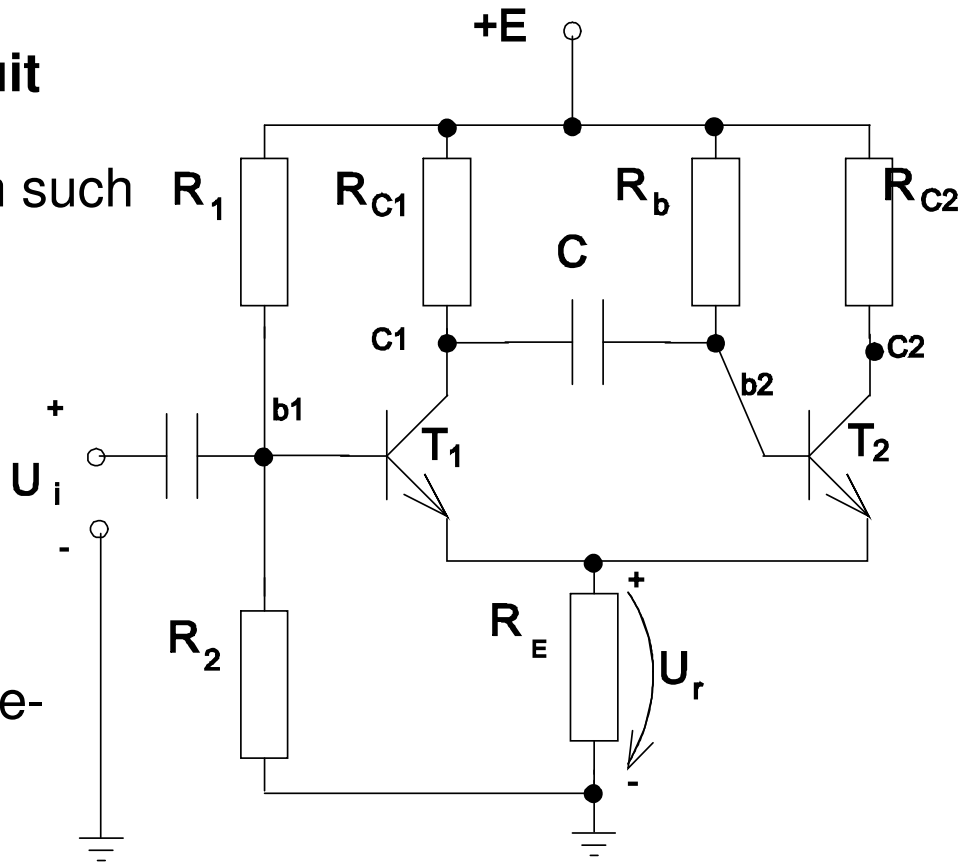
$U_{B2}(t_1) \approx U_{B1}(0) - E_C \approx -E_C$

During the unstable state, capacitor C starts discharging from initial value: E_C to final value: $U_C = -E_C - I_{C0} r_1$ and voltage U_{B2} will grow exponentially to $-U_C$ This positive voltage will open T_2 and due to positive reaction, circuit will be back in the stable state

Duration of the unstable state, given by analysis of the blocking condition of transistor T_2 and the saturation condition of T_1.
Results the dimension of the resistance R: $$R \leq \frac{\beta_{\min} E_C}{\frac{E_C}{R_{C1}} + \frac{2 E_C}{R_B} + \frac{E_B \beta_{\min}}{r_2}} - R_{C2}$$

Simplified time duration for unstable state: $T_{si} \approx \tau \cdot \ln 2 = 0{,}69 \cdot r_1 \cdot C$

Emitter coupled Monostable Circuit



Resistances R_1, R_2 and R_B are chosen such the stable state is: transistor T_1 off and T_2 saturated.
Circuit switches to the unstable state if a positive impulse is applied at the input, such that the transistor T_1 goes on

This way the positive reaction loop is re-established. The steps are:
- the base voltage of T_1, U_{B1} increases
- the basis current I_{B1} increases
- the collector potential, U_{C1}, decreases, so the base potential U_{B2} decreases
- the emitter current I_{E2} decreases
-the potential drop on the resistance R_E, decreases, so the potential of the basis of T_1 becomes more positive and the positive reaction loop closes.

After the transistor T_1 opens, the discharging process of the capacitor C begins, so the voltage fall U_C decreases and the base voltage of T_2 increases; the moment when U_{BC2} reaches the threshold voltage, T2 unlocks and a reversed cumulative switching process appears, which ends with the blocking of the transistor T_1 and the saturation of T_2.

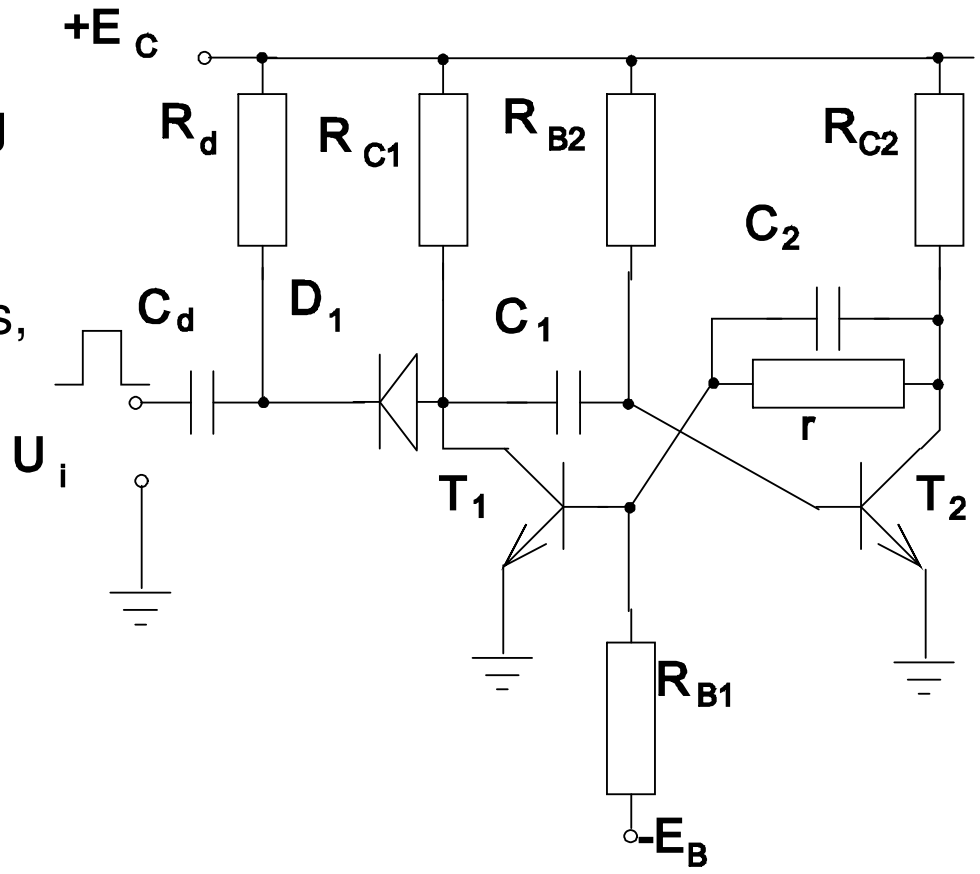
The duration of the unstable state is given by the values of an RC circuit:

$T_{si} \approx 0{,}69 \cdot R_B C$.

At the end of the unstable state a switching process is taking place, through which the circuit returns to the stable state

Collector-driven monostable using a common path

Identical driving circuit as for flip-flops, made up with differentiating circuit $R_d C_d$ and diode D_1



Monostable realized with TTL gates

Circuit built up with two TTL NAND gates and a RC circuit

The switching will be triggered by low active enable signal E

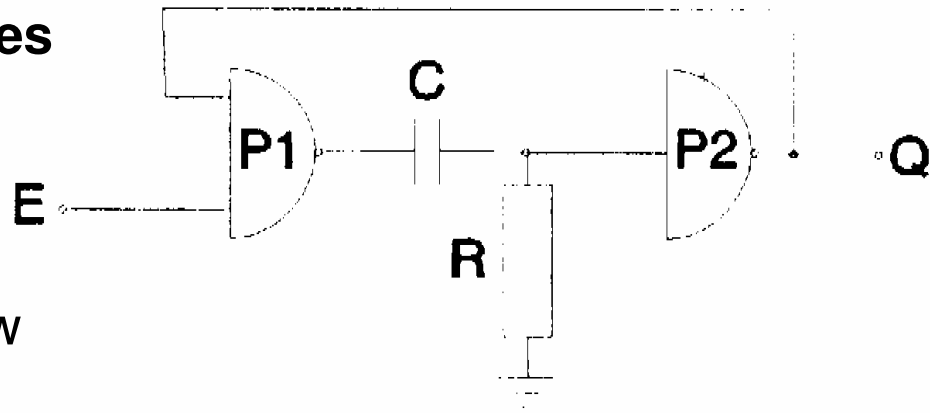


Figura 11.35 CBM cu porti TTL

When applying E, at the output of the first gate P1 will exist a positive jump which will be transmitted through the capacitor C to the input of gate P2, which initially was biased at the stable state through the resistance R, connected to ground. When the positive jump appears on the input of the gate P2 this will switch, the negative voltage jump from its output will be transferred to the input of the gate P1, which will remain in '1' logical level;
in time, through gate's output transistor, the capacitor C will discharge from V_{CC} to the ground.
When on the input of the gate P2 the potential will reach the threshold, the gate will switch back to '1' level, and together with the end of the negative pulse, will make the gate P1 to pass into '0' logical level, the stable state.

The approximate duration of the unstable state is:

$$T_{si} \approx RCln\frac{V_{OH} + V_{IL} - V_{OL}}{V_T}$$

Monostable circuit using CMOS gates

Circuit built up with two CMOS NOR gates and a RC circuit

The switching will be triggered by high active enable signal I
Stable state will make output Q at '0' due to R connected to V_{DD}

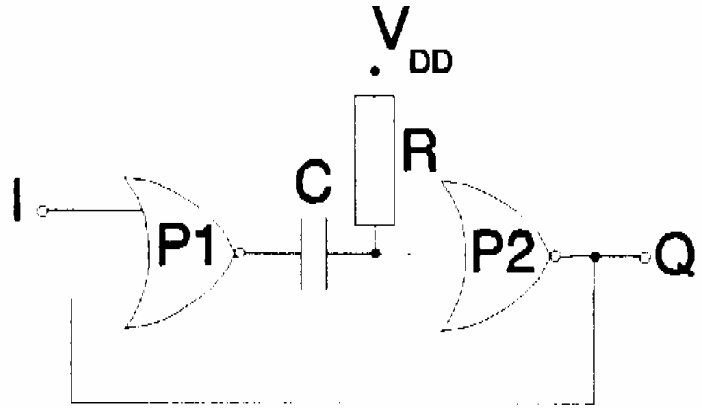


Figura 11.36 CBM cu porti CMOS

When at the input I is applied a positive triggering pulse, the gate P1 will present at the output a negative voltage jump, which will reach the input of the gate P2 through the capacitor C, producing the switch of this to '1' logical level.
Then the capacitor C will charge up from V_{DD} and when the potential on its terminals will reach the switching threshold value, the gate P2 will switch back to '0', the stable state of the circuit.
The duration of the unstable state can be determined with the formulae:

$$T_{si} \approx RC\ln\frac{V_{DD}}{V_{DD} - V_T}$$

Astable Circuits (ASC)

ASC with discrete components

Existence of two unstable states.
The switching is executed in a very short time and appears with a sudden variation of the electrical quantities.
Switching is triggered without applying any signals from outside;
Duration of states defined by the circuit's parameters.
The ASC is an oscillator,
which produces at the output a square signal.
The duration and the period of the impulses are determined by some elements of the circuit.

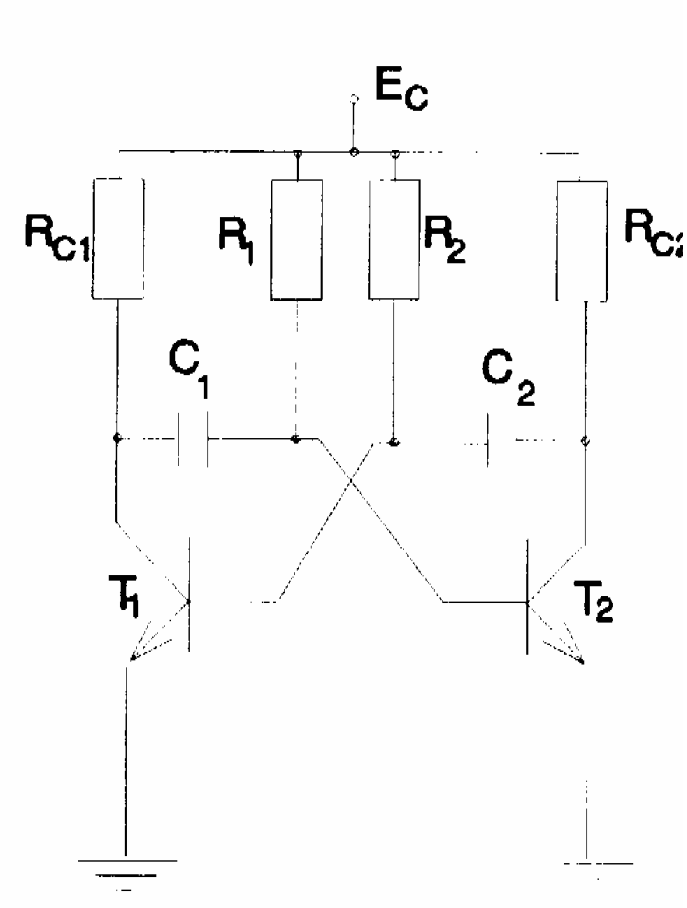


Figura 11.38 Schema de principiu a CBA

ASC with collector-base coupling illustrated

Fact that the R_1 and R_2 resistances are tied to the source $+E_C$, assures that transistors in stationary regime will not remain blocked for an undefined period of time

Let be the state where the transistor T_1 is blocked and the transistor T_2 is on; it implies that the voltage on capacitance C_2 decreases, the capacitor discharging through the circuit E_C, R_2, C_2 and open transistor T_2.
During the decrease of the current on R_2, the base potential of T_1,increases and when U_{B1} will reach the threshold voltage of the transistor T_1, this will open and its collector potential will start to decrease. This will make the base potential of T_2 to decrease and it will get out of saturation. The positive reaction loop will impose an avalanche process, which at the end will block T_2, and the circuit will pass like this in the second unstable state.
The transistor T_1 is now conducting, now the capacitor C_1 will discharge through the circuit E_C, R_1, C_1 and T_1. This state will last until the base voltage of T_2 will pass over the opening threshold value, and the transistor T_2 will open, reestablishing the positive reaction loop, which will launch the switching to the other unstable state.

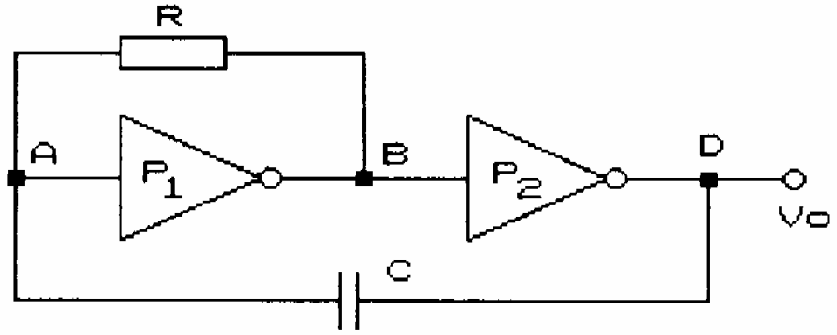
In the first state, near the discharging of the capacitor C_2, the charge up of the capacitor C_1 will take place, through the circuit E_C, R_{C1}, C_1 and the input resistance of the transistor T_2. The charging time constant is:
$\tau_{1i} \approx R_{C1} \cdot C_1$.
For the second state the capacitor C_2 will be charged up through the chain E_C, R_{C2}, C_2 and the saturated transistor T_1, with a time constant
$\tau_{2i} \approx R_{C2} \cdot C_2$.

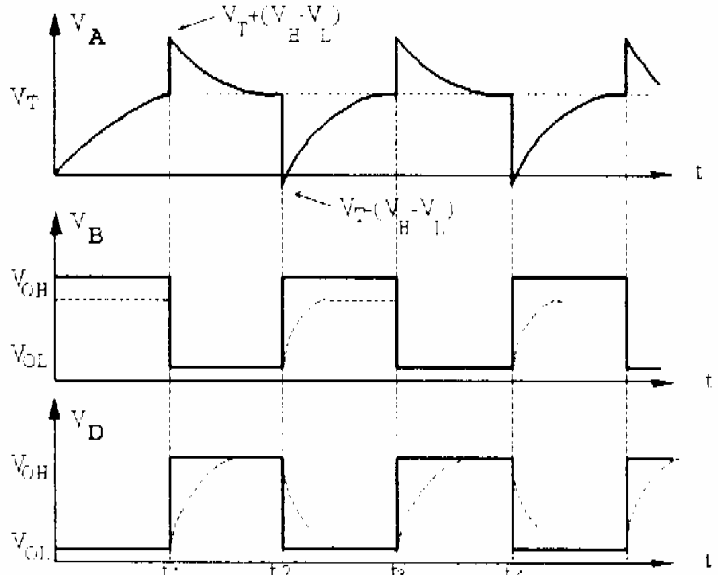
The duration of the two unstable periods will be determined with the formulae:

$$T_{si1} \approx 0{,}69 \cdot R_1 \cdot C_1$$
$$T_{si2} \approx 0{,}69 \cdot R_2 \cdot C_2$$

For a symmetrical ASC, for which $R_1 = R_2 = R$, and $C_1 = C_2 = C$,
will be generated a square signal (a rectangular voltage) in the collectors of the transistors, having the period
$T \approx 1{,}4 \cdot RC$
and a filling factor of 1/2.

ASC implemented with TTL gates





Operation: if at moment $t<t_1$ at the input of the gate P_1 (A point) there is logical '0' signal, at its output (point B) will be logical '1', and at the output of the gate P_2 will have logical '0'. So, potential of the point A tends to increase to V_H, due to capacitor C charging up through resistance R from high voltage in B.
At the moment $t=t_1$ when $V_A=V_T$, (threshold potential of P_2), the voltage in D goes high; this jump will be transmitted through capacitor C to point A.
The voltage from point A will start decreasing exponentially to the low value from the output of the gate P1, during the discharge process of the capacitor C through R toward low potential of B.
At the moment $t=t_2$, $V_A=V_T$ which determines again the two gates to switch.

The voltage jump from the point D will be transmitted through the capacitor C to A. Then the capacitor will charge up through the resistance R, and the potential from A will increase…
The phenomenon will continue until the circuit is under voltage (see diagrams previous slide).

ASC using Schmitt Trigger

Capacitor C is charging up and discharging through resistance R, tending to the output voltage value, but when it reaches the switching threshold V_{T1} and V_{T2} the circuit switches from one state to another
The duration of the states are:

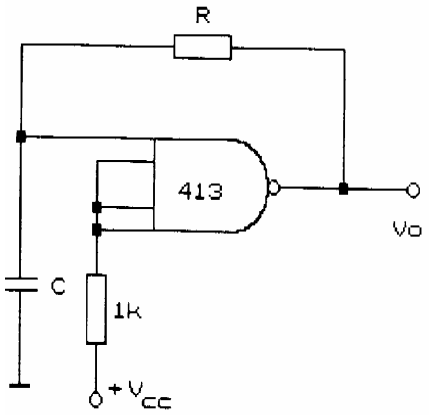


Fig.1.41 CBA cu TS

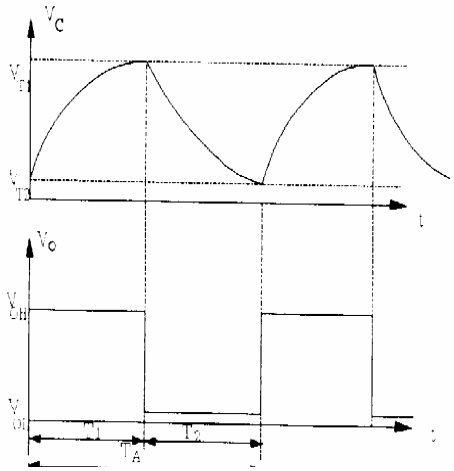


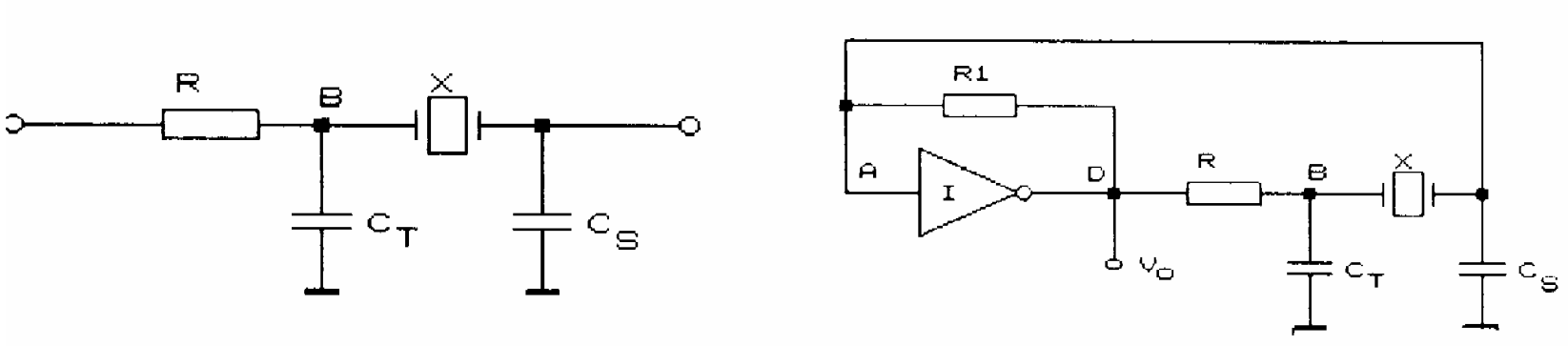
Fig.1.42 Diagrama de semnale

$$T_1 = RC \cdot \ln \frac{V_{0H} - V_{T2}}{V_{0H} - V_{T1}} \qquad T_2 = RC \cdot \ln \frac{V_{0L} - V_{T1}}{V_{0L} - V_{T2}}$$

For integrated circuit 413: $T_1 \approx 0{,}86 \cdot RC$ & $T_2 \approx 0{,}83 \cdot RC$

Astable realized with quartz crystals and logical gates

Oscillators with quartz realized with CMOS circuits assures the advantage of the low power consumption and the stability of frequency on a large scale.



Fundamental oscillator contains an amplifier and a network with reaction. The circuit presented in figure, also called π network with quartz, is indicated to be used together with an amplifier, which assures a 180˚ phase shift.

Proposed Problems

Design a monostable circuit with CMOS gates, presenting an unstable state of 0,1ms.

Determine the unstable state duration for a monostable circuit based on TTL gates, if: R=220Ω and C=47nF.