

# DIGITAL DEVICES

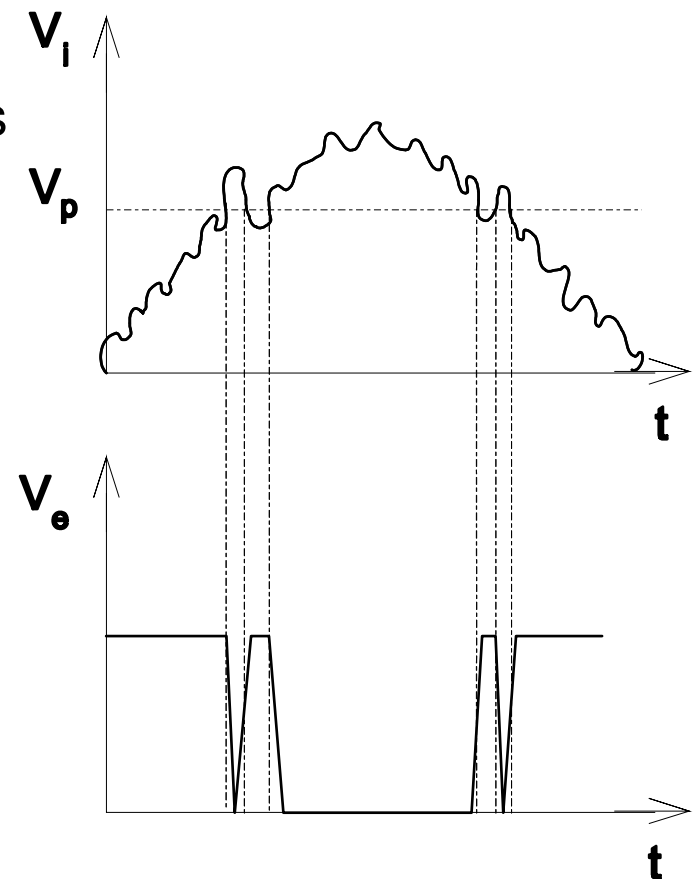
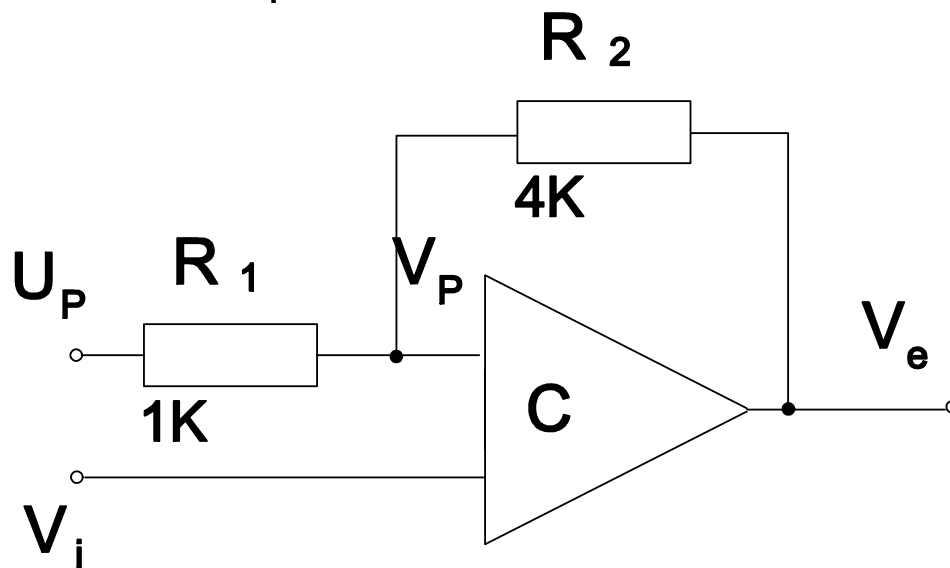
## Schmitt Trigger Circuits

# Schmitt triggers (pulse generators)

Used for adapting the logical levels and for generating steep (firm) pulse edges

Use: if at the inputs of some gates are applied signals with slow variation, together with disturbing (false) pulses: when connecting, in a numerical system the electromechanical parts (relays) with the logical ones, made of TTL or CMOS gates (see right example of distortion)

Fundamental layout of a Schmitt trigger consists of a comparator with a positive reaction loop, made of two resistances

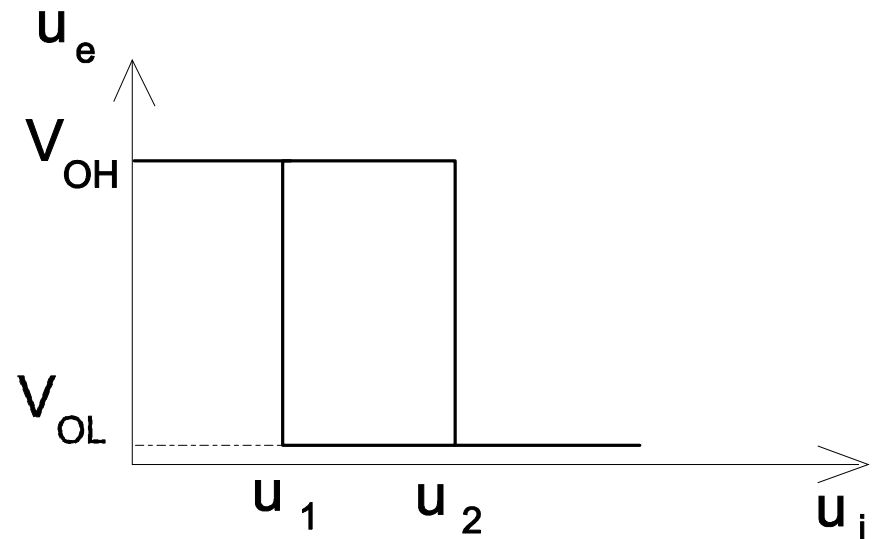


Instead of the comparator there can be other active elements

The transfer characteristic: it presents two states, being a hysteresis characteristic

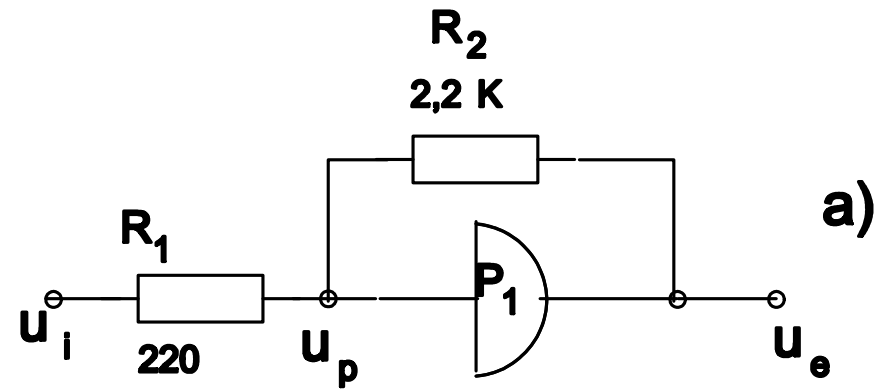
Two positive consequences:

- the transition between the two states is fast, even if the input signal has a slow variation
- as long as the noise signal amplitude, which affects the input is smaller than the hysteresis, there will be only one transition for the rising front of the input and only one transition for the falling front of the input signal

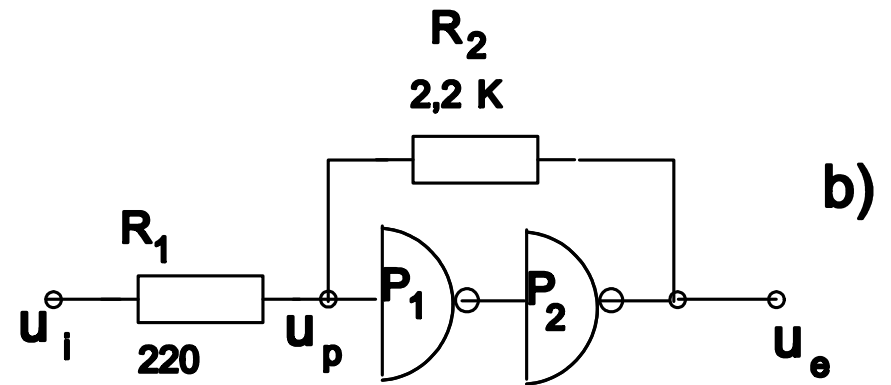


# Schmitt Triggers realized with TTL gates

Schmitt trigger made of AND gate



Schmitt trigger made of NAND gates



Consider negligible values of the input and output currents of used TTL gates, in comparison with the current that passes through the  $R_1$  and  $R_2$  resistances, Voltage in point P, denoted by  $U_p$

$$U_P = U_i - \frac{R_1}{R_1 + R_2}(U_i - U_e)$$

For input voltage  $U_i$  of 0V, the output voltage is null as well

If  $U_i$  grows,  $U_p$  grows too, and there will be  $U_p$  equal to threshold voltage of TTL gate  $U_T$

Consider  $U_P=U_T$ ,  $U_i=U_1$  and  $U_e=U_{OL}$  : 
$$U_T = U_1 - \frac{R_1}{R_1 + R_2}(U_1 - U_{OL})$$

Corresponding input voltage, when  $U_p$  equals threshold level:

$$U_1 = U_T \frac{(R_1 + R_2)}{R_2} - U_{OL} \frac{R_1}{R_2}$$

When the input voltage exceeds the level  $U_1$ , at which  $U_P=U_T$ , the switching of the gate takes place. The output voltage grows producing a positive reaction through the resistance  $R_2$  and passing rapidly on high logical level,  $U_e$  taking the value  $U_{OH}$  regardless of the continuous increase of the input voltage

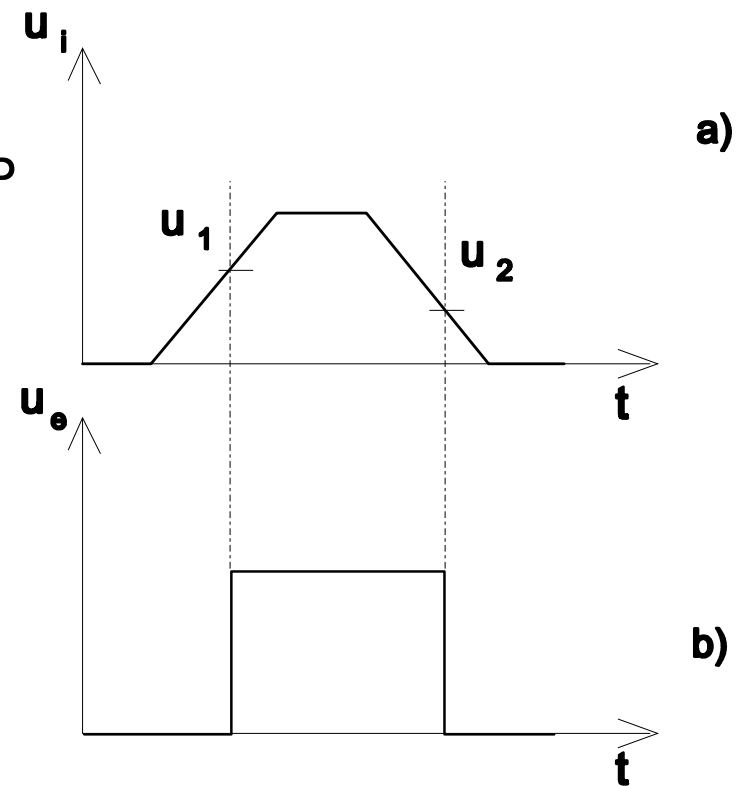
When decreasing the input voltage, phenomenon is similar: when reaching at point P the threshold voltage of the TTL gate, output voltage begins dropping due to the positive reaction through the  $R_2$  resistance, going to low logical level,  $U_{OL}$ . The input voltage that determines the switching is calculated similarly:

$$U_2 = U_T \frac{R_1 + R_2}{R_2} - U_{OH} \frac{R_1}{R_2}$$

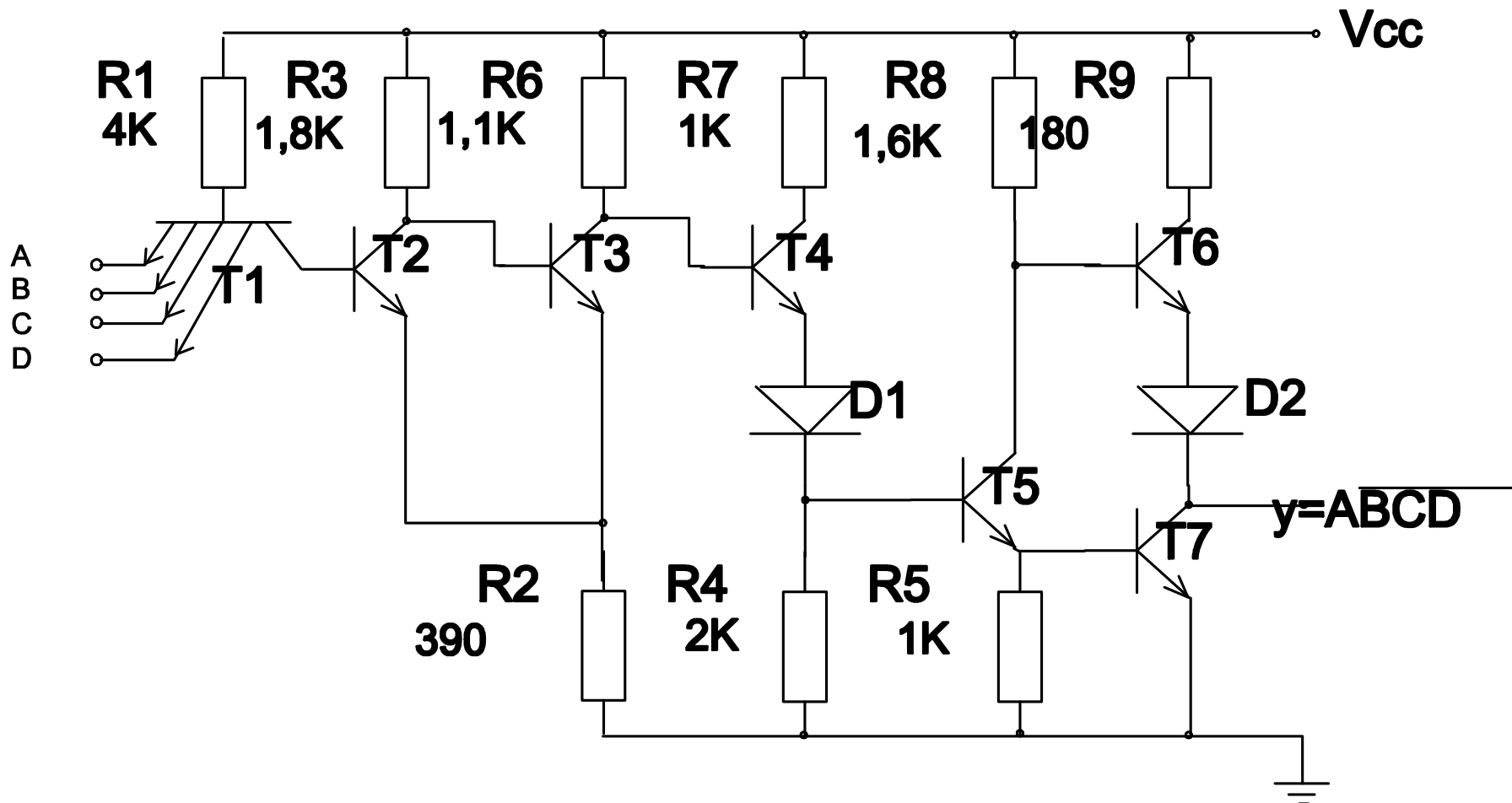
It results the hysteresis voltage:

$$U_{HIS} = U_1 - U_2 = \frac{R_1}{R_2} (U_{OH} - U_{OL})$$

Modifying the ratio between  $R_1$  and  $R_2$  the hysteresis cycle can be modified, noting that  $R_1$  has the upper boundary at the value of 390 ohms



# Integrated TTL Schmitt Triggers



The TTL integrated circuit with Schmitt trigger function is the circuit CDB413, whose fundamental diagram is shown behind; besides the role of generating pulses, fulfills the NAND logical function ( 4 inputs)

The circuit layout shows identical input/output circuits as for every TTL gate; the trigger itself is made of  $T_2$  and  $T_3$  transistors. The electronic layout of the integrated Schmitt trigger contains compensation circuits for avoiding temperature influence, the threshold voltages being set in the prescribed temperature and supply voltage range.

The switching thresholds for a supply voltage  $V_{CC}=5V$  are:  $U_1=1,7V$  and  $U_2=0,9V$ , determining a hysteresis voltage of  $0,8V$

Other typical values for the circuit:  $I_{IL} = -1,6mA$ ,  $I_{IH} = 40\mu A$ ,  $V_{ILmax}=0,7V$  and  $V_{IHmin}=2V$ .

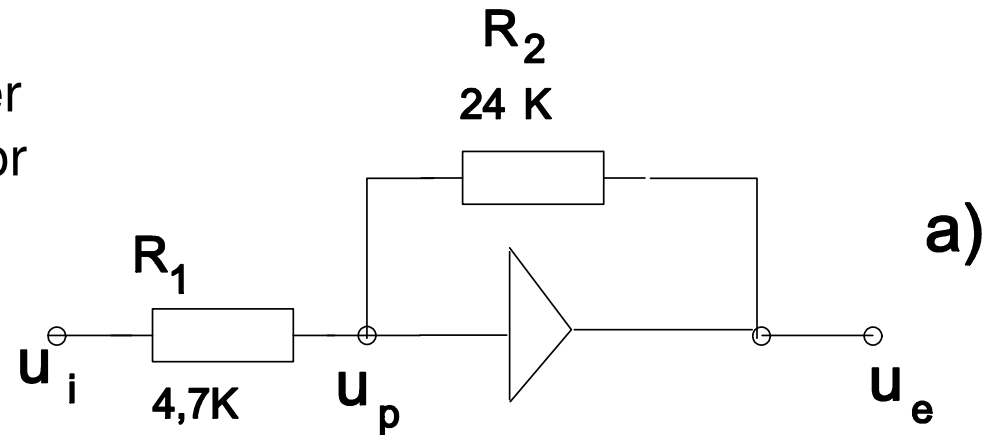
The maximum propagation delays for the integrated circuit CDB413 are:

$t_{pHL} = 30ns$  and  $t_{pLH} = 35 ns$ .



# Schmitt triggers made of CMOS gates

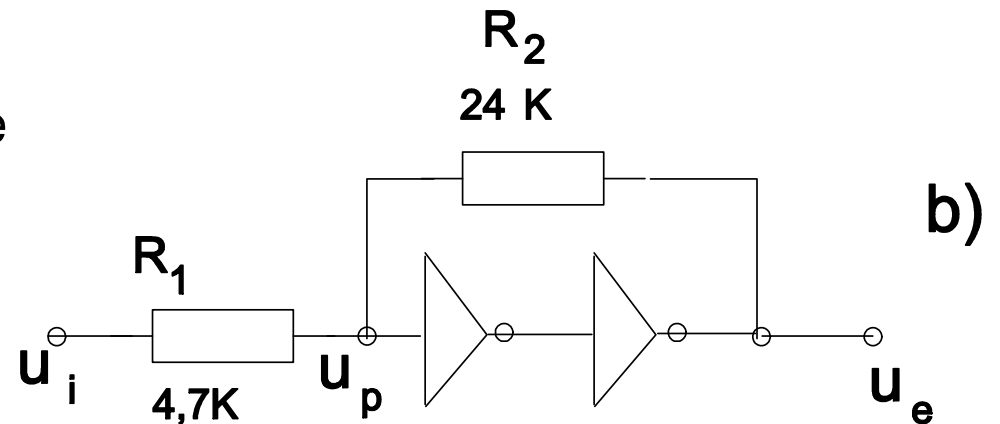
Schmitt trigger can be obtained either with non-inverter CMOS circuits (a) or with inverter circuits (b)



The functioning of the trigger with CMOS gates is identical with the one with TTL gates; calculus formulae of the threshold voltages are directly obtained:

$$U_1 = U_T \cdot \frac{R_1 + R_2}{R_2} - U_L \cdot \frac{R_1}{R_2}$$

$$U_2 = U_T \cdot \frac{R_1 + R_2}{R_2} - U_H \cdot \frac{R_1}{R_2}$$



If we consider  $U_L = 0V$ ,  $U_H = V_{DD}$  and  $U_T = V_{DD}/2$ , we obtain:

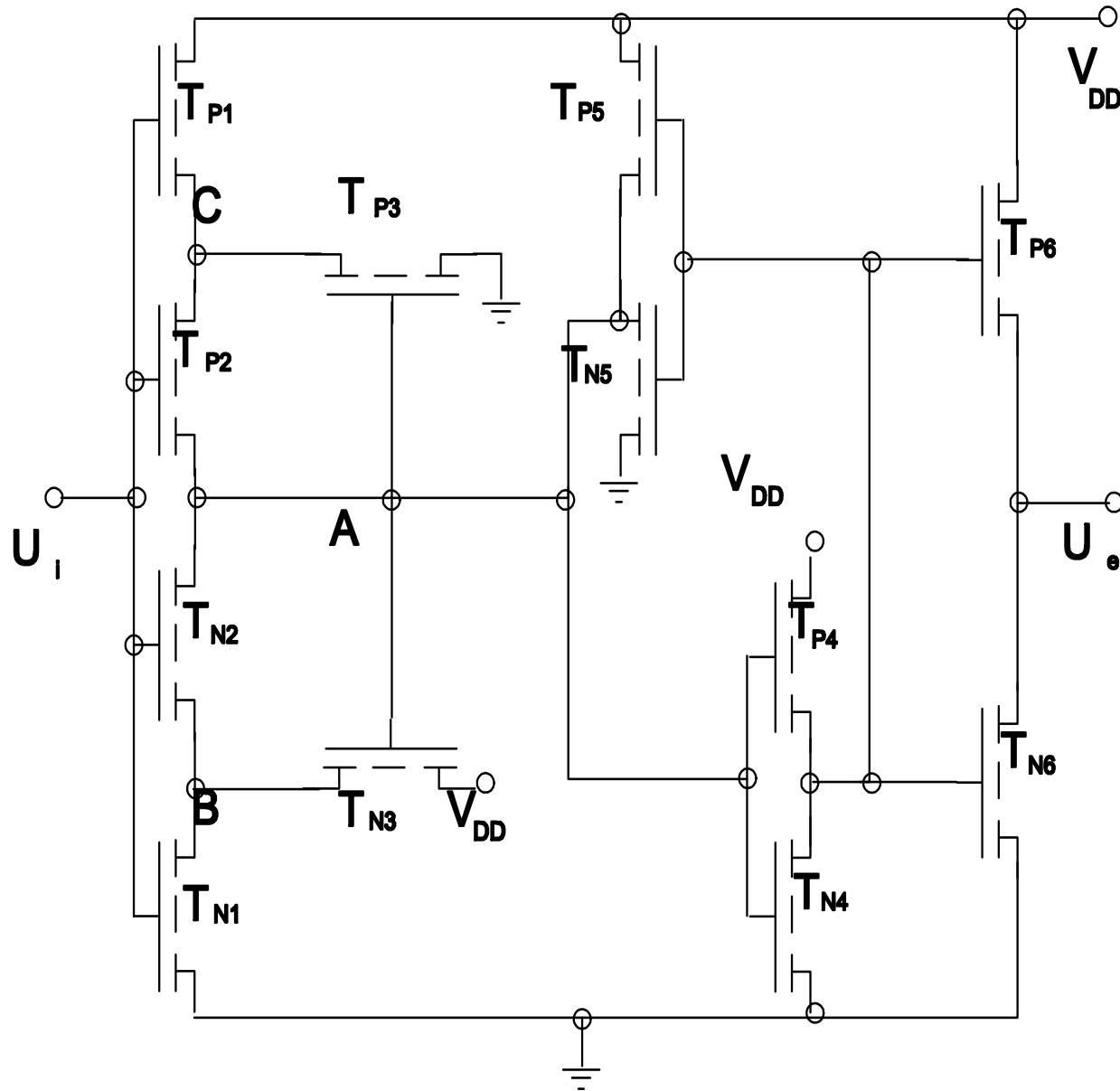
$$U_1 = \frac{R_1 + R_2}{2R_2} \cdot V_{DD}$$

$$U_2 = \frac{R_2 - R_1}{2R_2} \cdot V_{DD}$$

Results a hysteresis voltage:

$$U_{HIS} = U_1 - U_2 = \frac{R_1}{R_2} \cdot V_{DD}$$

# Integrated CMOS Schmitt trigger circuits



Layout  
integrated circuit  
MMC 4093

Figure behind presents the electrical diagram of an integrated Schmitt trigger with CMOS transistors.

The input circuit is made of six transistors, three with inductive channel **p** and three with inductive channel **n**.

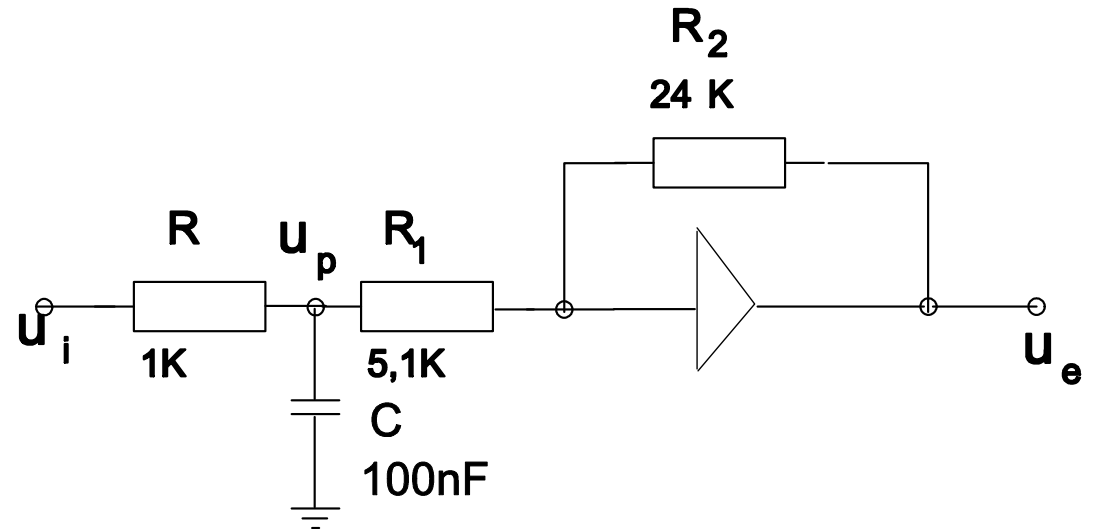
The two CMOS inverters obtained through the pairs  $T_{P4}$ ,  $T_{N4}$ , respectively  $T_{P5}$ ,  $T_{N5}$  form a RS type circuit (latch) for stabilization and detainment of the voltage in point A.

The output circuit is obtained from the CMOS inverter with the transistors  $T_{P6}$  and  $T_{N6}$ .

The transfer characteristics of a TS integrated CMOS depends on the voltage supplies. For  $V_{DD}=5V$ , the integrated circuit presents a typical hysteresis voltage  $U_{HIS}= 0,9V$ , and for a supply of  $V_{DD}=10V$ , it presents  $U_{HIS}=2,3V$

# Applications of the Schmitt trigger

## Delay Circuit



Delay circuit obtained with a TS and a low-pass RC circuit

For joining circuits, necessary respecting the condition:  $(R_1 + R_2) > 10 \cdot R$ .

This way the time constant of the integrating circuit stays  $\tau = RC$ , and the hysteresis voltage of the TS will not be influenced by the  $R$  resistance

By applying at the input an impulse signal, at the output the signal will be delayed, with  $\delta t_1$  for the forefront and respectively  $\delta t_2$  for the back front.

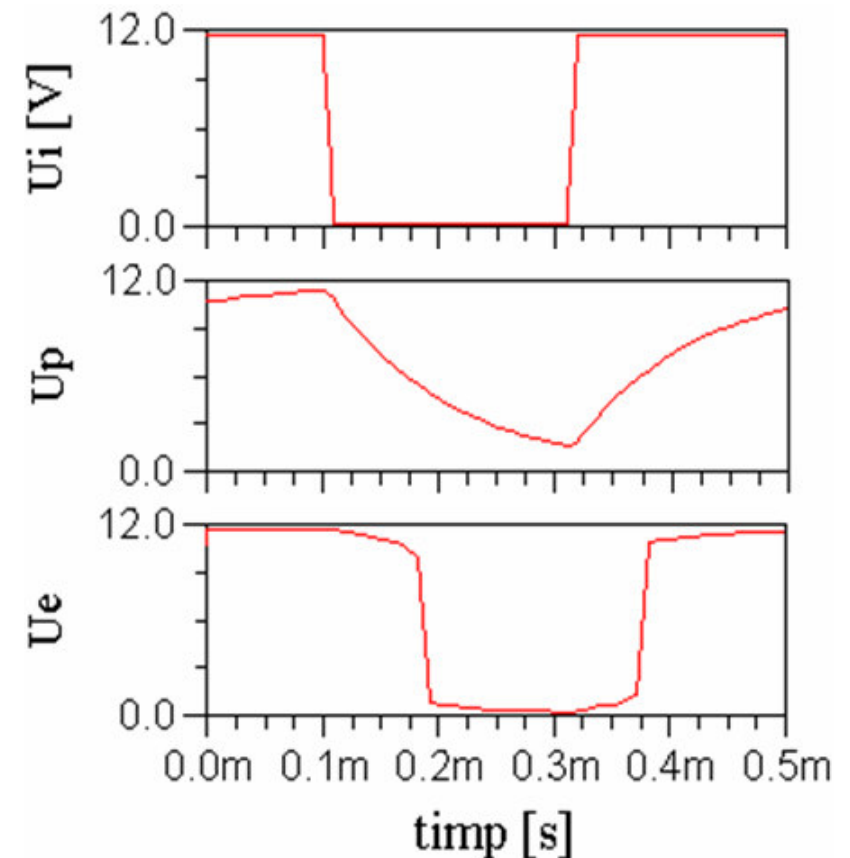
The voltages  $U_1$  and  $U_2$  being the threshold voltages of the TS, the relations for the two delays are:

$$\delta t_1 = RC \cdot \ln \frac{V_{DD}}{V_{DD} - U_1}$$

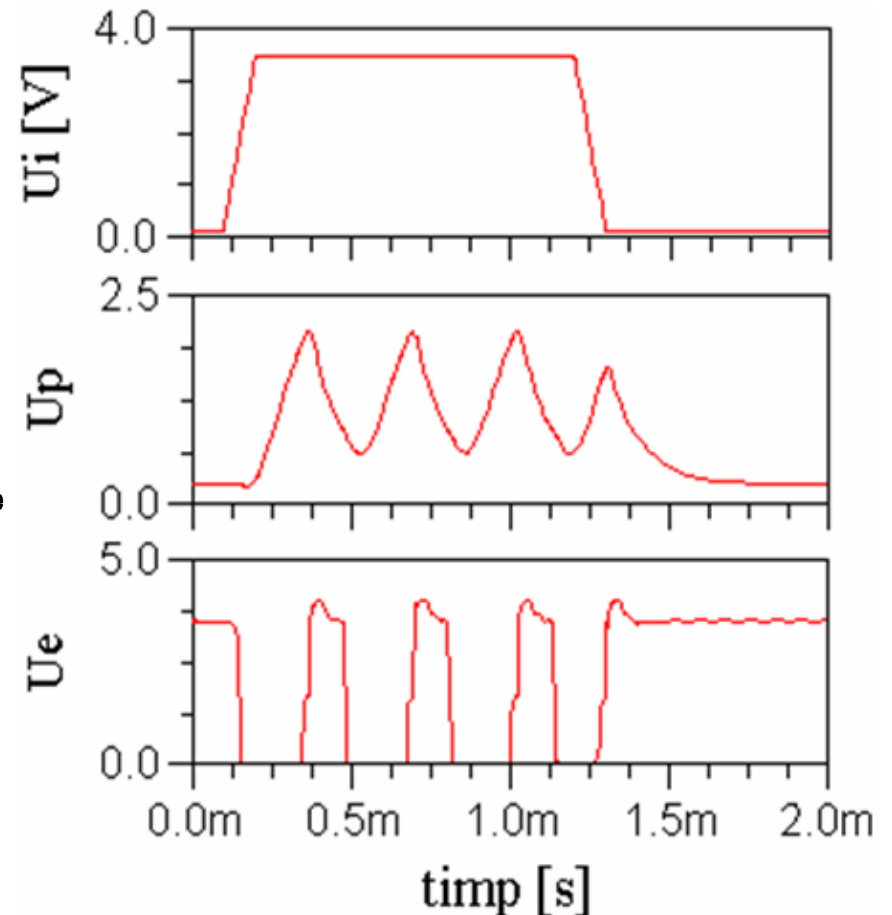
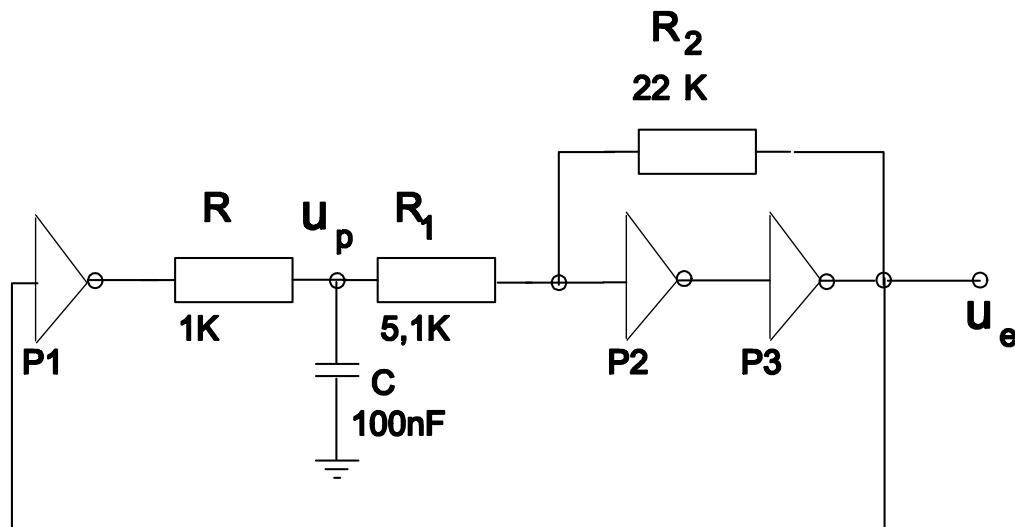
$$\delta t_2 = RC \cdot \ln \frac{V_{DD}}{U_2}$$

For  $V_T = V_{DD}/2$ :

$$\delta t_1 = \delta t_2 = RC \cdot \ln \frac{2 \cdot R_2}{R_2 - R_1}$$



## Front detector circuit using TS



Layout behind represents a front detector circuit, obtained with TS circuit and RC low-pass circuit

If at the output of the circuit from the figure we put a NAND gate, the circuit will do the detection of the positive fronts, if we put a NOR gate, the detection of the negative fronts will be realized, and the XOR gate will allow the detection of both fronts

## Proposed Problems

- Design a delay circuit with a TS circuit using CMOS gates, to provide a delay for the input signal of 0,1 ms. CMOS gates use a power supply source of 5V.

Assuming:

$$R=1K\Omega, R_1=5,1K\Omega, R_2=24K\Omega$$

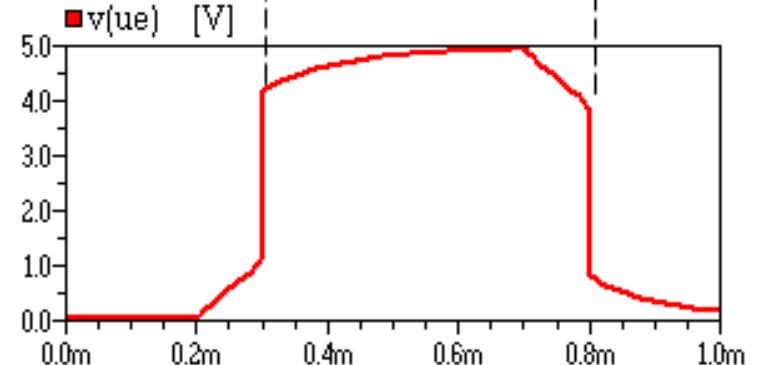
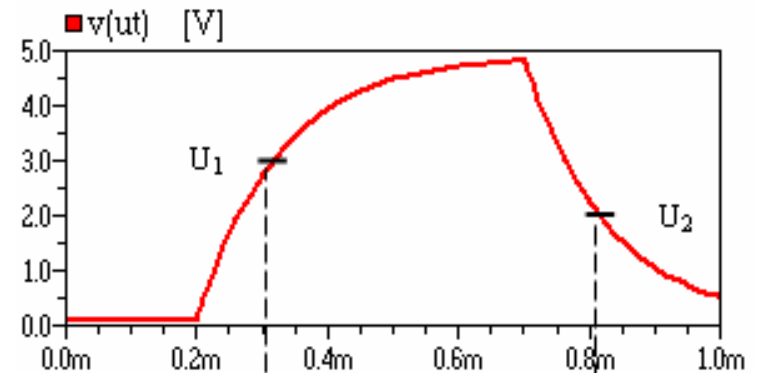
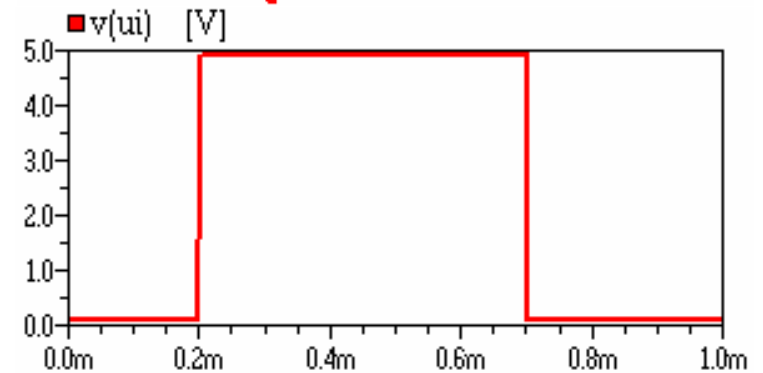
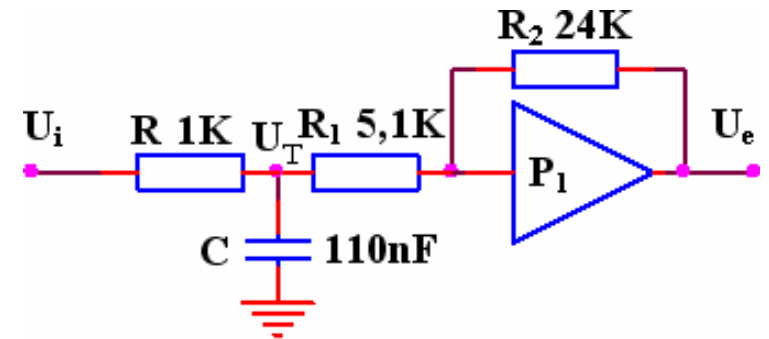
$$U_1 = \frac{R_1 + R_2}{2R_2} V_{DD} = 3V$$

$$U_2 = \frac{R_2 - R_1}{2R_2} V_{DD} = 2V$$

$$U_e(t) = U_e(\infty) + [U_e(0) - U_e(\infty)] e^{-\frac{t}{RC}}$$

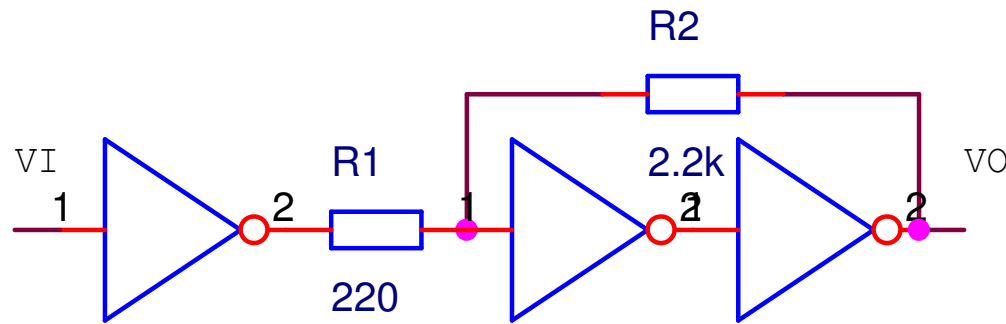
$$C = \frac{t}{R \ln \frac{U_e(\infty) - U_e(0)}{U_e(\infty) - U_e(t)}}$$

$$C = \frac{t}{R \ln \frac{V_{DD}}{V_{DD} - U_1}} = \frac{t}{R \ln \frac{V_{DD}}{U_2}} = 110nF$$





Calculate the needed noise margins for a standard TTL gate driving a trigger Schmitt circuit built on TTL technology, with  $R_1=220\Omega$  and  $R_2=2,2k\Omega$ .



$$U_1 = U_T \frac{(R_1 + R_2)}{R_2} - U_{OL} \frac{R_1}{R_2} = 1.4V \quad U_2 = U_T \frac{R_1 + R_2}{R_2} - U_{OH} \frac{R_1}{R_2} = 0.7V$$

$$M_H = V_{OH \min} - U_2 = 2.4V - 0.7V = 1.7V$$

$$M_L = U_1 - V_{OL \max} = 1.4V - 0.4V = 1V$$

- Design a delay circuit using TS circuit with TTL gates, implementing a delay of the positive edge with 0,1 ms. What's the delay for the negative edge?
- Design an oscillator with a TS circuit using CMOS gates. Oscillator is driven by a zero-active signal; oscillation period is of 2ms. CMOS gates are supplied with a power supply source of 5V.