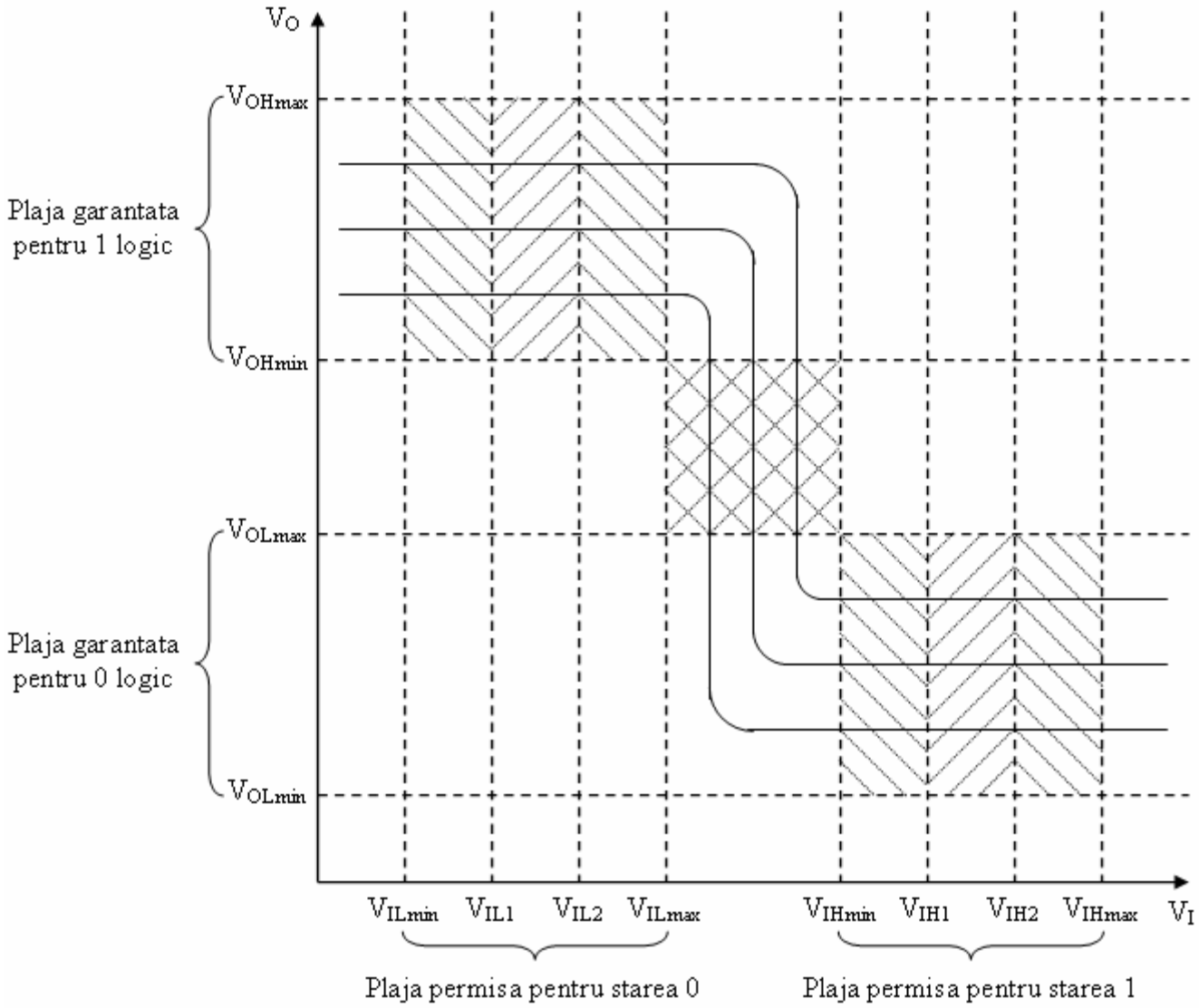
# DIGITAL CIRCUITS
## Parameters of the integrated logic circuits

- Static transfer characteristic
- Noise margins
- Fan-out & fan-in
- Propagation time
- Power Dissipation

# Static Transfer Characteristic

- Output voltage variation function of input dc voltage
- Cann’t be defined an unique voltage value for logic ‘1’ or ‘0’
- Transfer characteristic isn’t unique
- characteristic bounded by two limit curves
- to each input or output variable, two voltage intervals (domains) will be associated: allowed, and respectively guaranteed

# Static Transfer Characteristic for an Inverter




- Four voltage ranges
- Two for inputs
- Two for outputs
- Defined by eight voltage values

# Input/Output voltage values

- $V_{ILmin}$ – minimum voltage level for logic ‘0’ at input
- $V_{ILmax}$ - maximum voltage level for logic ‘0’ at input
- $V_{IHmin}$ - minimum voltage level for logic ‘1’ at input
- $V_{IHmax}$ - maximum voltage level for logic ‘1’ at input
- $V_{OLmin}$ - minimum voltage level for logic ‘0’ at output
- $V_{OLmax}$ - maximum voltage level for logic ‘0’ at output
- $V_{OHmin}$ - minimum voltage level for logic ‘1’ at output
- $V_{OHmax}$ - maximum voltage level for logic ‘1’ at output

Index meaning

I – *input*

O – *output*

L – *low* logic ‘0’

H - *high* logic ‘1’

# Defining the working regions

- A logic circuit will work properly if the input voltage levels will have admitted values (work in allowed regions)
- Obtained output voltage levels will be into guaranteed regions
- Considering that output voltage will become input voltage for driven circuit(s), have five working regions:
  - Normal working region for logic ‘0’ and logic ‘1’
  - Working region in presence of noise signals for logic ‘0’ and respectively ‘1’
  - Transitory region

## Normal working region (no noise signals)

- For low input voltage level (L), between values $V_{IL2}$ - $V_{IL1}$
- For high input voltage level (H) between values $V_{IH2}$ - $V_{IH1}$

## Working region when noise signals apply

- For low input voltage level (L), between values $V_{ILmax} – V_{ILmin}$
- For high input voltage level (H) between values $V_{IHmax}$ - $V_{IHmin}$

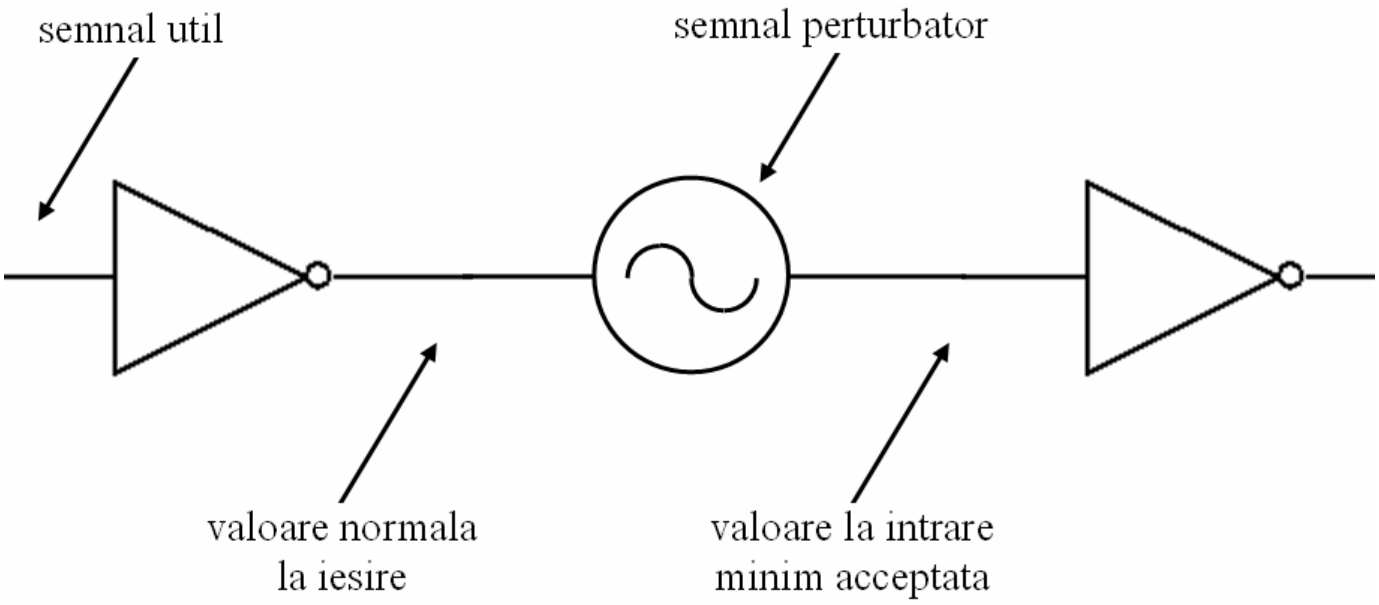
# Transitory region

- For input voltage levels between $V_{IHmin}$ – $V_{ILmax}$
- Those input voltages driving circuit from one stable state to the other

# Noise margins

- Noise (immunity) margins: stability at static perturbations
- the noise margin is the peak amount of spurious or "noise" voltage that may be superimposed on a weak gate output voltage signal before the receiving gate might interpret it wrongly
- Guaranteed noise margin for a logic state is given by difference between guaranteed output voltage level of the driving circuit and the worst case for the input voltage level accepted for that state by the driven circuit

# Guaranteed noise margins (manufacturer's specifications)

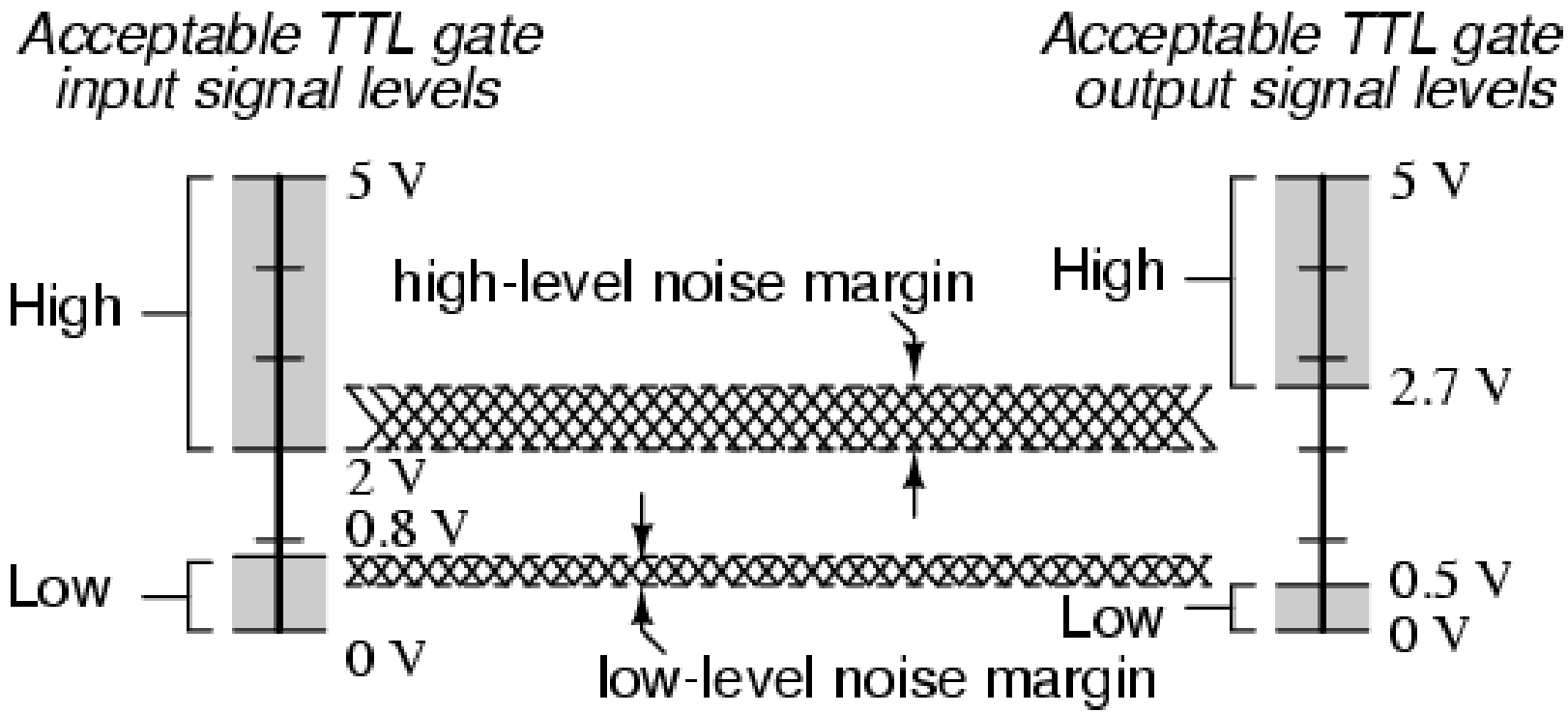



- For logic '0' state:

$$M_L = V_{ILmax} - V_{OLmax}$$

- For logic '1' state:

$$M_H = V_{OHmin} - V_{IHmin}$$




Example for TTL family

# Fan-out and Fan-in

- The input of a circuit is a load for its driver circuit
- For a logic circuit generates guaranteed output voltage levels is a must to be driven at inputs with corresponding current levels
- For circuit interconnection, important to design the output current of the driving circuit, and to consider the sum of input currents of the driven circuits

# Fan-in factor for logic circuits

- Fan-in (FI) and Fan-out (FO) factors are defined based on some current values, those correspondind to allowed input voltages and respectively to guaranteed output voltages, in the worst case: $I_{ILmax}$, $I_{IHmin}$, $I_{OLmax}$ şi $I_{OHmin}$
- For any integrated circuits family, a basic (fundamental) gate is defined, and the fan-in/ fan-out values for the rest of circuits are defined as multiples of the values for that basic gate
- For an input, the FI value means the number N (N>1) of standard inputs (i.e. of basic gate) equivalent to that input: FI=N

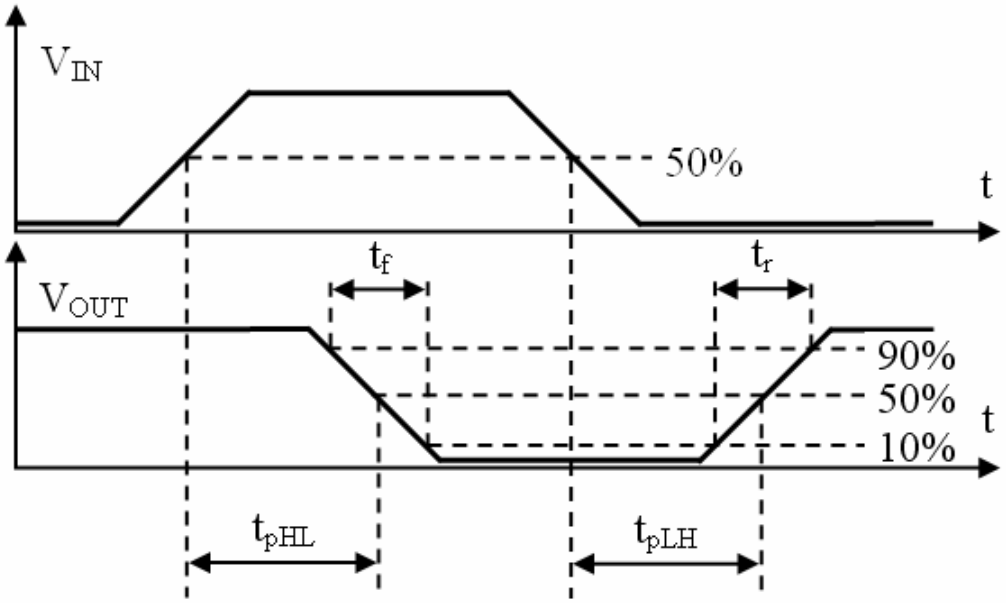
# Fan-out factor for logic circuits

$$FO_L = \left\lfloor \frac{|I_{OL}|}{|I_{IL}|} \right\rfloor, FO_H = \left\lfloor \frac{|I_{OH}|}{|I_{IH}|} \right\rfloor, FO = \min(FO_L, FO_H)$$

- When interconnecting logic circuits (from a family), the following relations must be satisfied (associate with the worst case):

$$I_{OL} \geq \sum_{n}^{i=1} I_{IL}, \; I_{OH} \geq \sum_{n}^{i=1} I_{IH}$$

# Propagation Time




- Raising-up and fall-down times ($t_r$ , $t_f$) are defined using ratios of signal amplitude (0.1 and 0.9)

- Propagation times (delay) ($t_{pHL}$ si $t_{pLH}$) are defined for halves the input/output signal amplitudes
- Average propagation time: $t_{pd}=(t_{pHL}+t_{pLH})/2$
- Important parameter for any circuit, giving sign of performance

# Power Dissipation

- Parameter depending on:
  - Power supply voltage ($V_{CC}$);
  - Absorbed currents from $V_{CC}$ when output is logic ‘1’ ($I_{CCH}$), or ‘0’ logic ($I_{CCL}$);
  - Output current on shortcircuit ($I_{OS}$);
  - Average power consumption ($P_m$);

# Average power dissipation on cc

$$P_{CC} = \frac{P_H + P_L}{2} = \frac{I_{CCH} + I_{CCL}}{2} \cdot V_{CC}$$

## Power dissipation on ac

- Important power component, due to charging/ discharging of stray output capacitances Cp
- Power consumption during the switching regime:

$$P_C = f C_P V_{CC}^2$$

f – switching frequency

# Total power dissipation

$$P_m = P_{CC} + P_c = \frac{I_{CCH} + I_{CCL}}{2} V_{CC} + f C_P V_{CC}^2$$

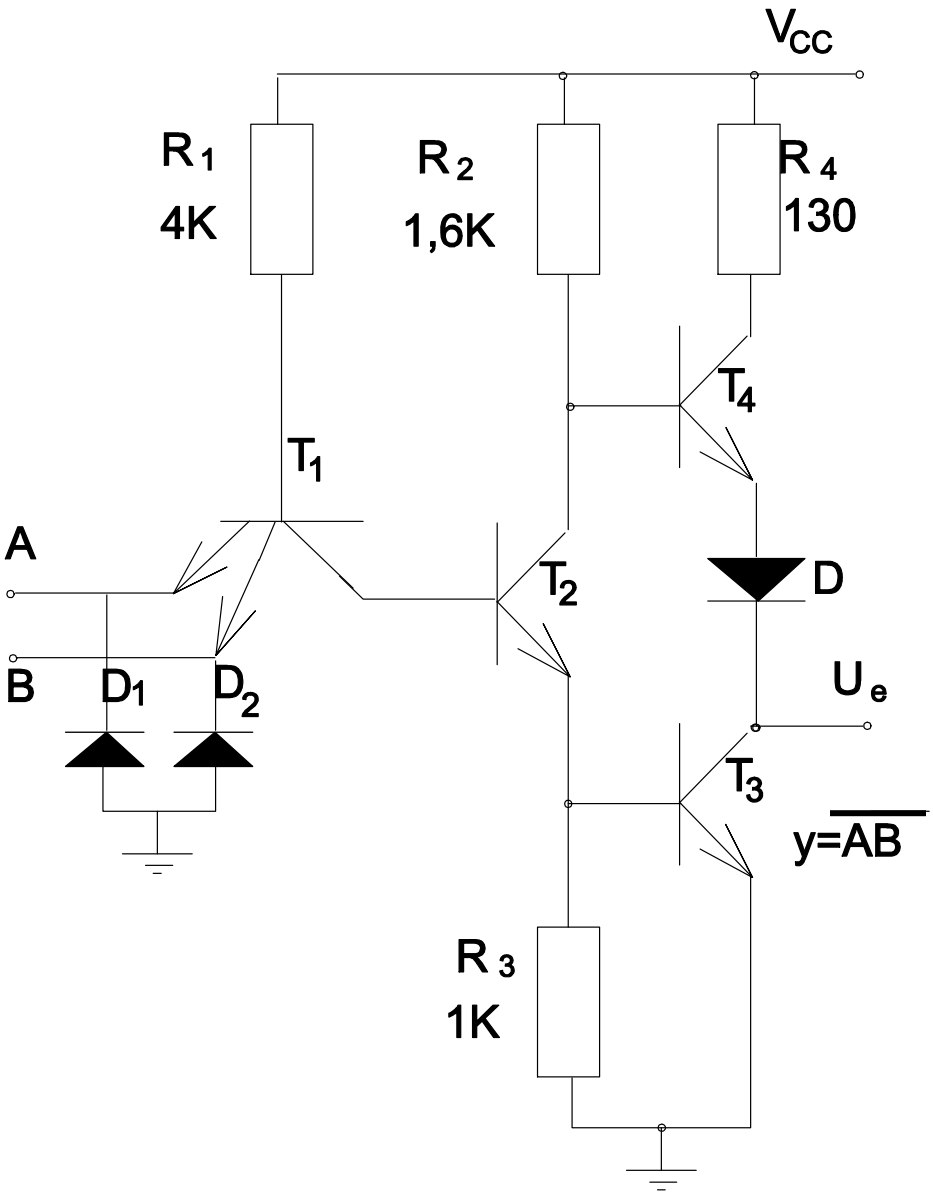
# TTL Logic Integrated Circuits

- General considerations
- TTL standard series
  - –TTL basic (fundamental) gate
  - –Circuit description
  - –Gate operation
  - –Parameters of TTL basic gate

# General Considerations

- TTL (Transistor-Transistor-Logic)
- Family with a lot of circuit series, developed based on a trade-off between propagation speed and power dissipation
- Standard, high-speed (H), Low power (L), Schottky (S)

# TTL Basic Gate




**Input stage**

- Multi-emitter transistor $T_1$
- Clipping diodes $D_1$, $D_2$

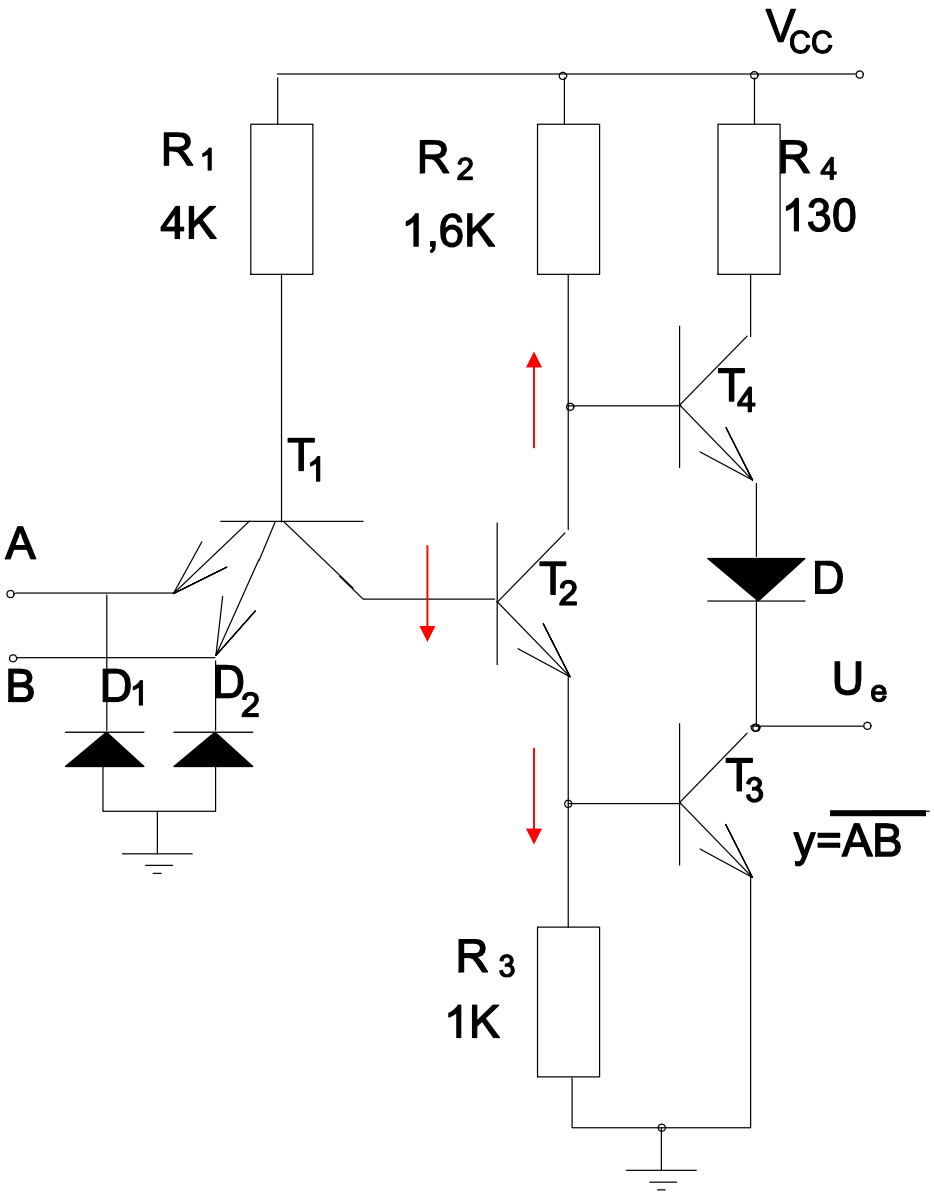
**Driver transistor**

- Transistor $T_2$

**Output stage**

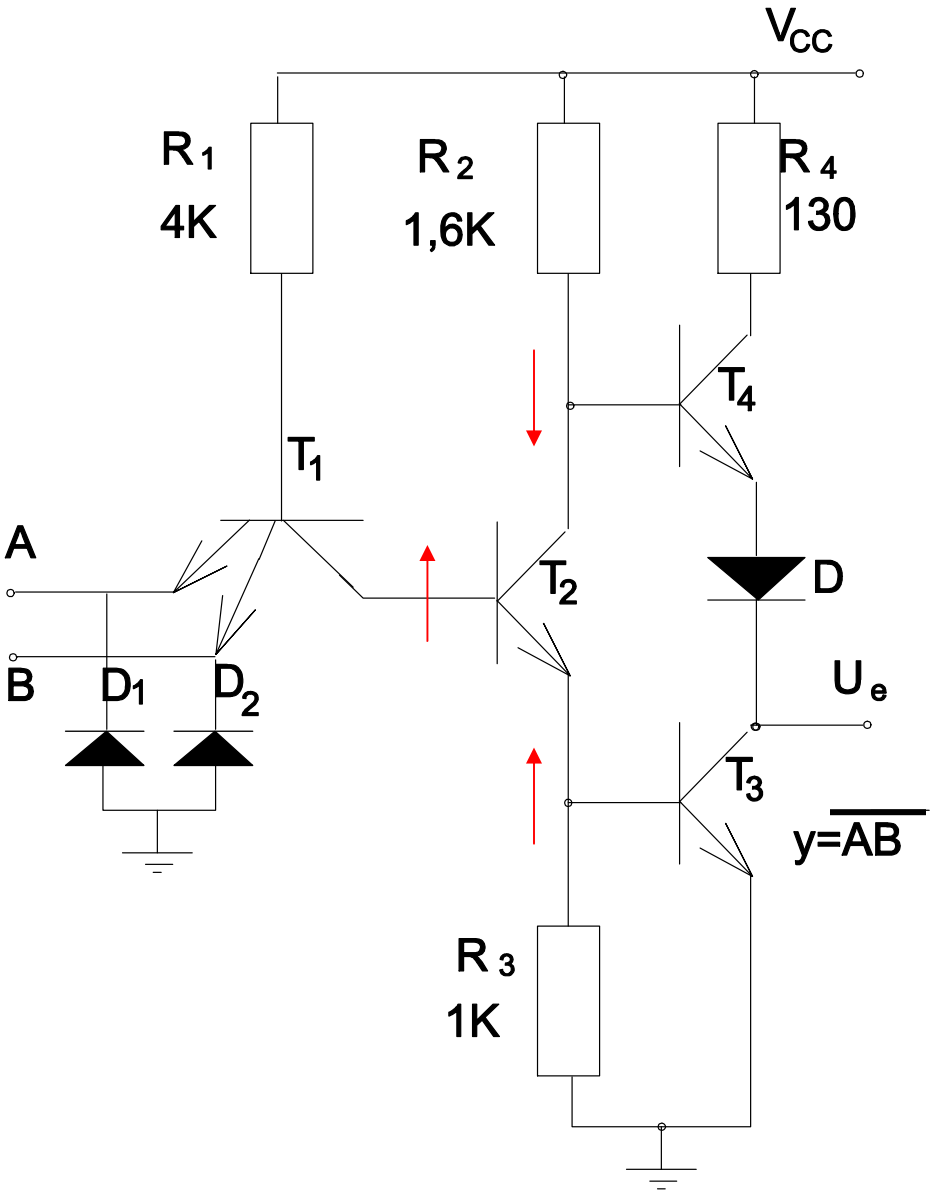
- transistors $T_4$ şi $T_3$
- diode D

# Gate operation for one input ‘0’




- $T_1$ saturated, voltage from $T_1$ collector lowers, transistor $T_2$ off
- Low voltage level from $T_2$ emitter drives $T_3$off
- High potential of $T_2$ collector opens transistor $T_4$
- $U_{R2}$ low, $U_{BE(T4)}+U_D \approx 1,5V$, $U_e > 3,4V$ corresponding to logic level "1"

# Gate operation when both inputs at logic ‘1’




- $T_1$ base-emitter junctions reverse biased (reverse active region)
- $T_1$ base-collector junction and base-emitter junctions of $T_2$ & $T_3$ make a chain of open diodes (forward biased by $R_1$ from power supply), $T_2$ & $T_3$ saturated
- $T_4$ off due to base potential, lower than emitter’s, due to presence of diode D
- $Ue=U_{CES(T3)}$ corresponding to logic "0"

$$U_e = \overline{A * B}$$

- Transistors $T_4$ & $T_3$ switch in counter-time, making $R_4$ being low (130Ω), building a low output impedance and a small time constant for charge/discharge of output stray capacitances

# Logic Levels

- $V_{ILmax}$ = 0.8 V
- $V_{IHmin}$ = 2 V
- $V_{OLmax}$ = 0.4 V
- $V_{OHmin}$ = 2.4 V
- $V_T$ = 1.3V, threshold voltage, same value for input and output voltages

# Noise Margins

- Guaranteed values

  $M_L = V_{ILmax} - V_{OLmax} = 0.8V - 0.4V = 0.4V$

  $M_H = V_{OHmin} - V_{IHmin} = 2.4V - 2V = 0.4V$
- Real values

  $M_L = V_T - V_{OL} = 1.3V - 0.2V = 1.1V$

  $M_H = V_{OH} - V_T = 3.5V - 1.3V = 2.2V$
- It implies that prefered output idle state being '1' logic, and switching command being ‘zero active’, i.e. a signal going from high to low

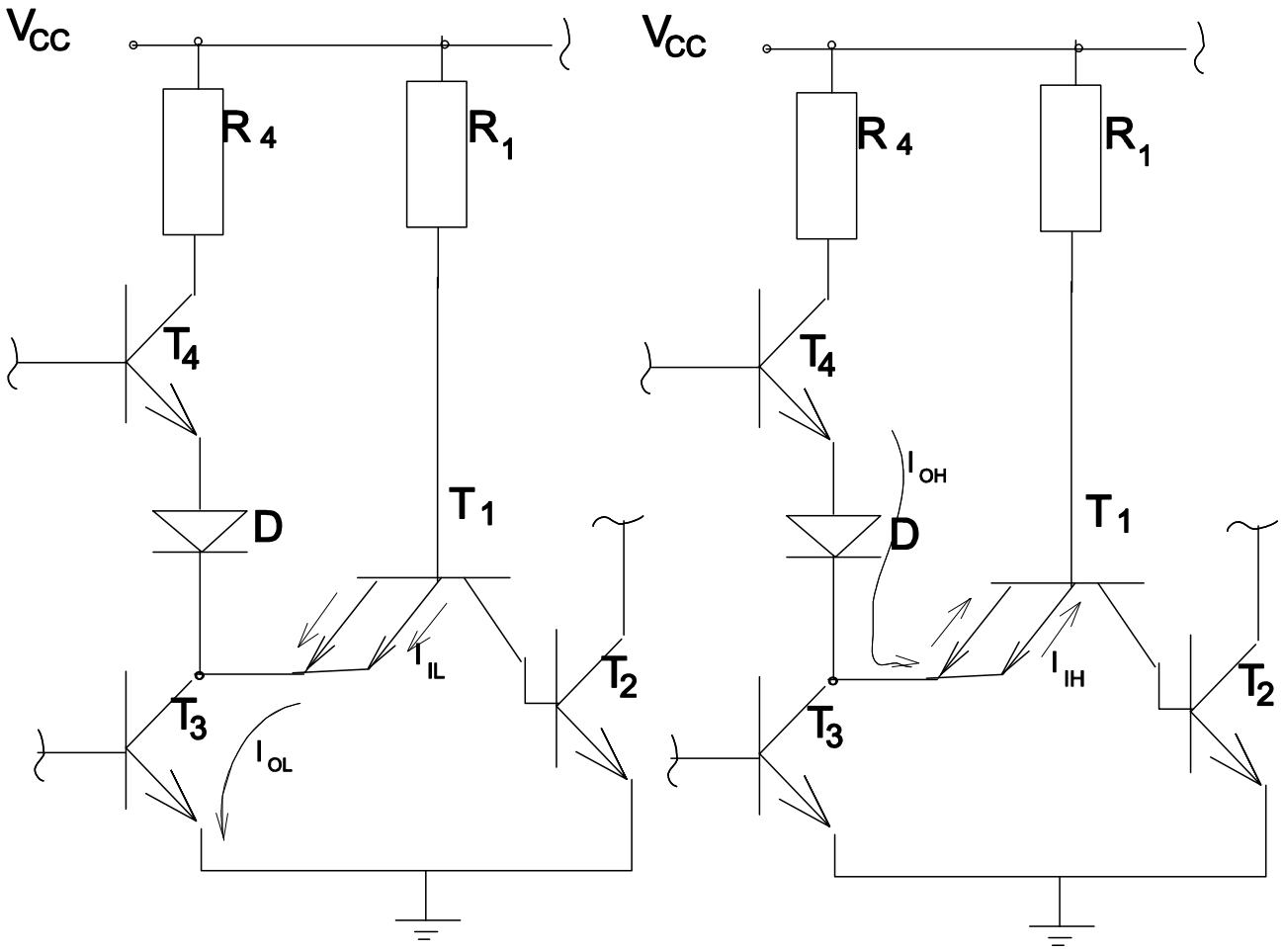
## Input & output currents

- By convention: positive value if gate sinks current and negative value if gate generates currents
- $I_{IH}$ = 40 µA
- $I_{IL}$ = -1,6 mA
- $I_{OH}$ = -800 µA
- $I_{OL}$ = 16 mA

# Fan-in/ fan-out

$FI_L = 1$, $I_{IL} = -1{,}6mA$

$FI_H = 1$, $I_{IH} = 40\mu A$

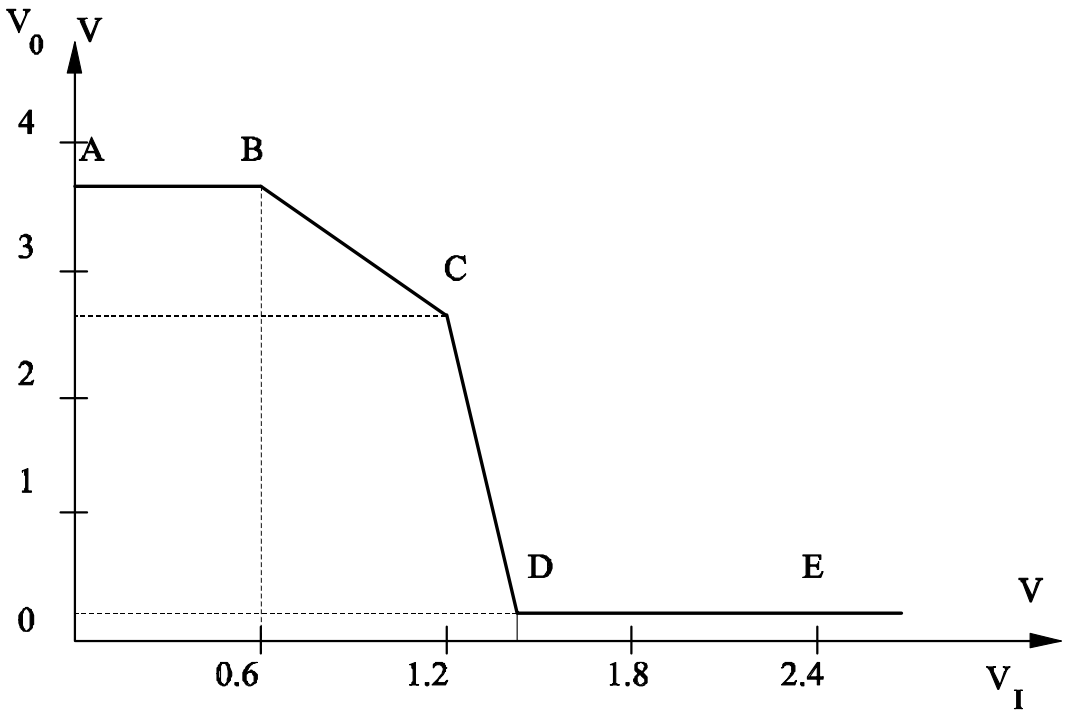



$$FO_L = \left\lfloor \frac{|I_{OL}|}{|I_{IL}|} \right\rfloor = \left\lfloor \frac{16mA}{1.6mA} \right\rfloor = 10, FO_H = \left\lfloor \frac{800\mu A}{40\mu A} \right\rfloor = 20, FO = \min(FO_L, FO_H) = 10$$

# Static transfer characteristic

$0V<U_i<0,65V$, $T_1$ on, $T_2$ off, $U_e = V_{CC} - R_2 \cdot I_{R2} - U_{BE(T4)} - V_D$, $U_{BE(T4)}=V_D=0,75V$, $I_{R2} \approx I_{B(T4)} = I_{OH}/(\beta_N+1)$, $U_e=3,4V$, on AB segment.

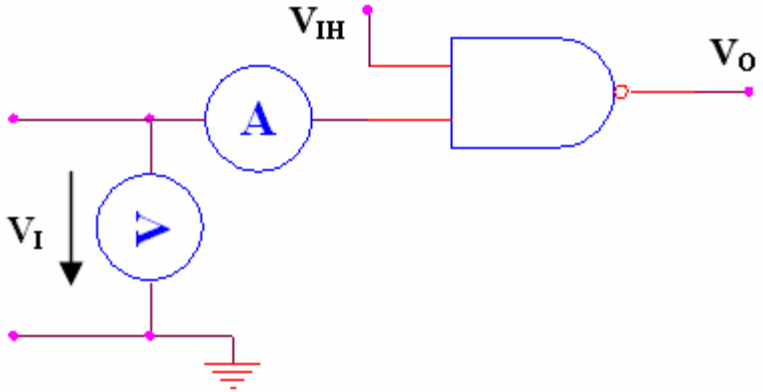
$0,65V<U_i<1,3V$, $T_2$ starts conducting, going into forward active region. Current gain for transistor $T_2$ over segment BC is: $\alpha \approx -R_2/R_3$. $T_4$ repeater, $T_3$ off, state for segment BC.

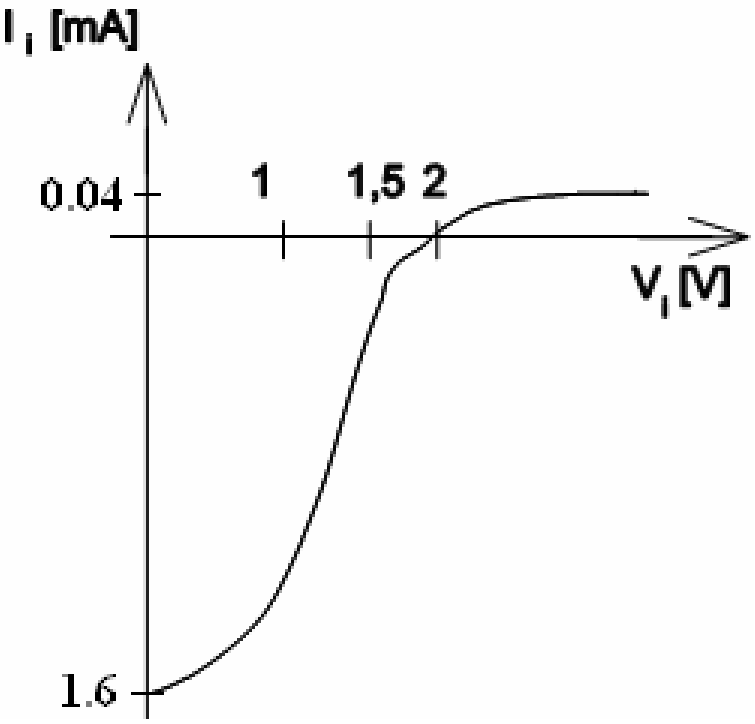



$1,3V<U_i<1,5V$, $T_3$ starts conducting, $U_e$ lowers quikly (segment CD). $T_2$, $T_4$ and $T_3$ conducting into forward active region. Current sink from the power supply increases.

$1,5V<U_i<2,25V$, $T_4$ off, $T_3$ saturated, $U_e=U_{CEs(T3)} \approx 0,2V$, region DE.

# Input Characteristics



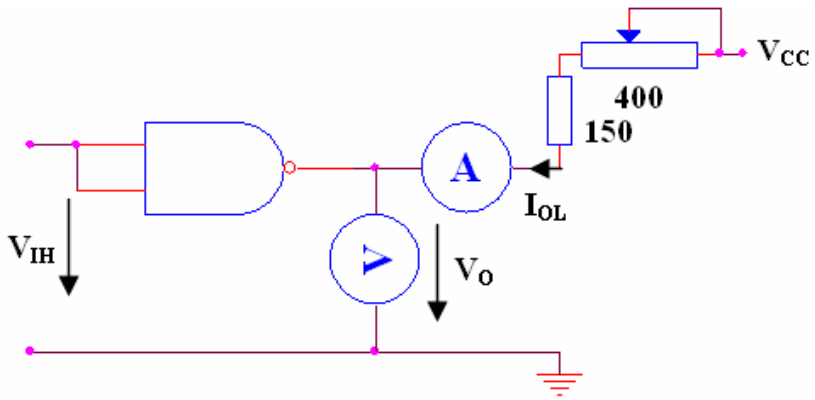



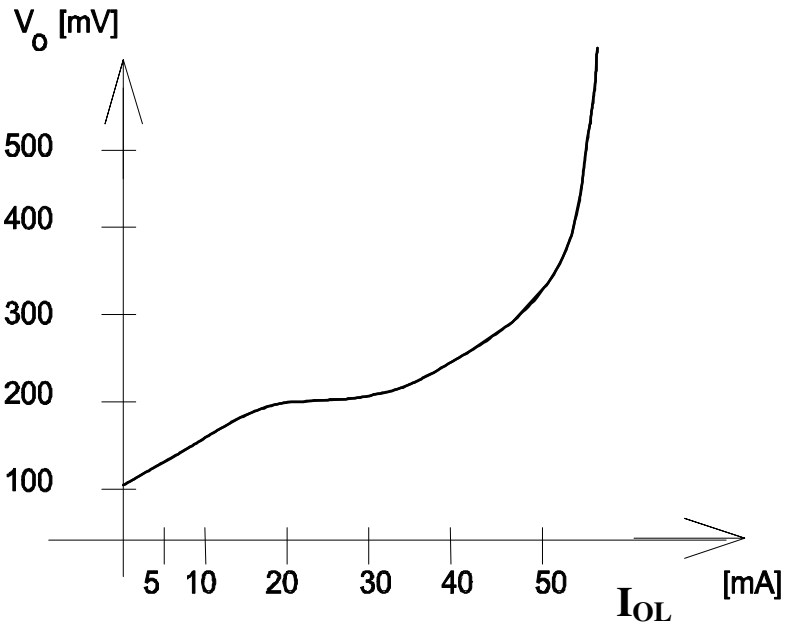

- $V_i < 0,8V$

$$I_I = \frac{V_{CC} - V_{BE(T1)} - V_I}{R_1}$$

- $V_i$ grows over 0,8V, $I_i$ lowers in absolute value
- $V_i > 1,3V$, $I_i$ tends abruptly toward 0
- $V_i = 1,7V$, $I_i=0$
- $V_i > 2 \div 2,25V$, $I_i \approx 28\mu A$

# Output Characteristics




- $V_{OL} = f(I_{OL})$
- $I_{OL}$ depends on $T_3$ base current, wich depends on $T_2$ emitter current, as:

$$I_{C(T2)} = \frac{V_{CC} - V_{BE(T3)} - V_{CEs(T2)}}{R_2}$$

$$I_{B(T2)} = \frac{V_{CC} - V_{BC(T1)} - V_{BE(T2)} - V_{BE(T3)}}{R_1}$$

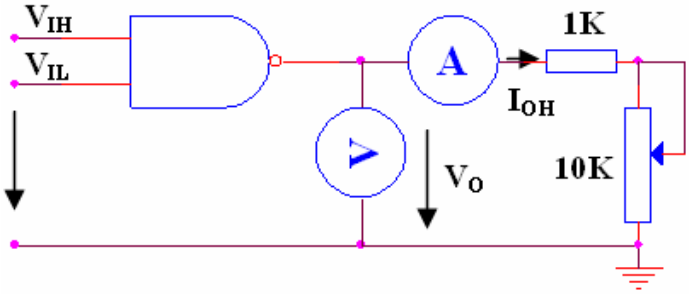
$$I_{E(T2)} = I_{B(T2)} + I_{C(T2)} = 3{,}2mA$$

$$I_{B(T3)} = I_{E(T2)} - I_3 = I_{E(T2)} - \frac{V_{BE(T3)}}{R_3}$$

$T_3$ saturated, $\beta_N=20$, output current:

$$I_{OL} = \beta_N \cdot I_{B(T3)} = 49mA$$

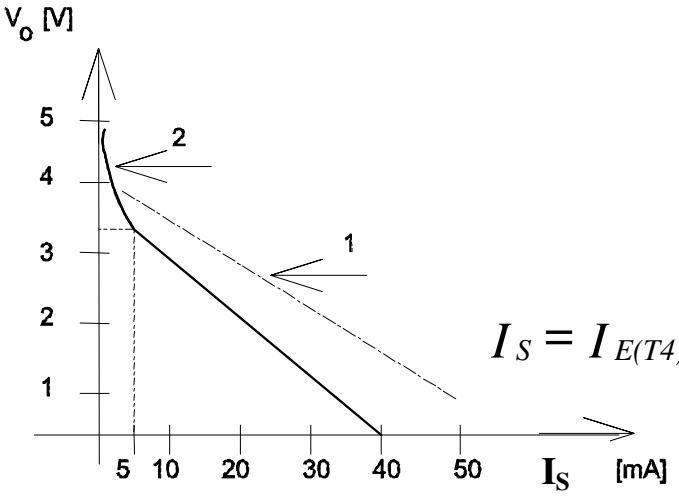
# Output Characteristics




- $V_{OH} = f(I_{OH})$
- Figure below presents in positive domain $V_{OH}=f(I_S)$ characteristics, where load current $I_S$ is considered $I_S= -I_{OH}$
- $T_4$ on, tending toward saturation
- $T_4$ when in forward active region, segment 1, $V_{OH}$ and $I_S$ are in relation:

$$V_O = V_{CC} - R_2\frac{I_S}{\beta_N + 1} - V_{BE(T4)} - V_D$$

$$V_{OH} = 3{,}7 - 32 \cdot I_S$$




- $T_4$ saturated, curve 2, relation becomes:

$$I_S = I_{E(T4)} = I_{B(T4)} + I_{C(T4)} = \frac{V_{CC} - V_O - V_D - V_{BE(T4)}}{R_2} + \frac{V_{CC} - V_O - V_D - V_{CE(T4)}}{R_4}$$

$$V_O \approx 4{,}5 - I_S \cdot R_4$$

- Curves 1 and 2 cross eachother at $I_S \approx 5$mA

# Power dissipation

$$P_{CC} = \frac{I_{CCH} + I_{CCL}}{2} V_{CC}$$

$I_{CCH}=I_{R1}=(V_{CC}-V_{B(T1)})/R_1 \approx 1mA$

$I_{CCL}=I_{E(T2)}=I_{C(T2)}+I_{B(T2)}=(V_{CC} - V_{C(T2)})/R_2+(V_{CC}-V_{B(T1)})/R_1 \approx 3,3mA$

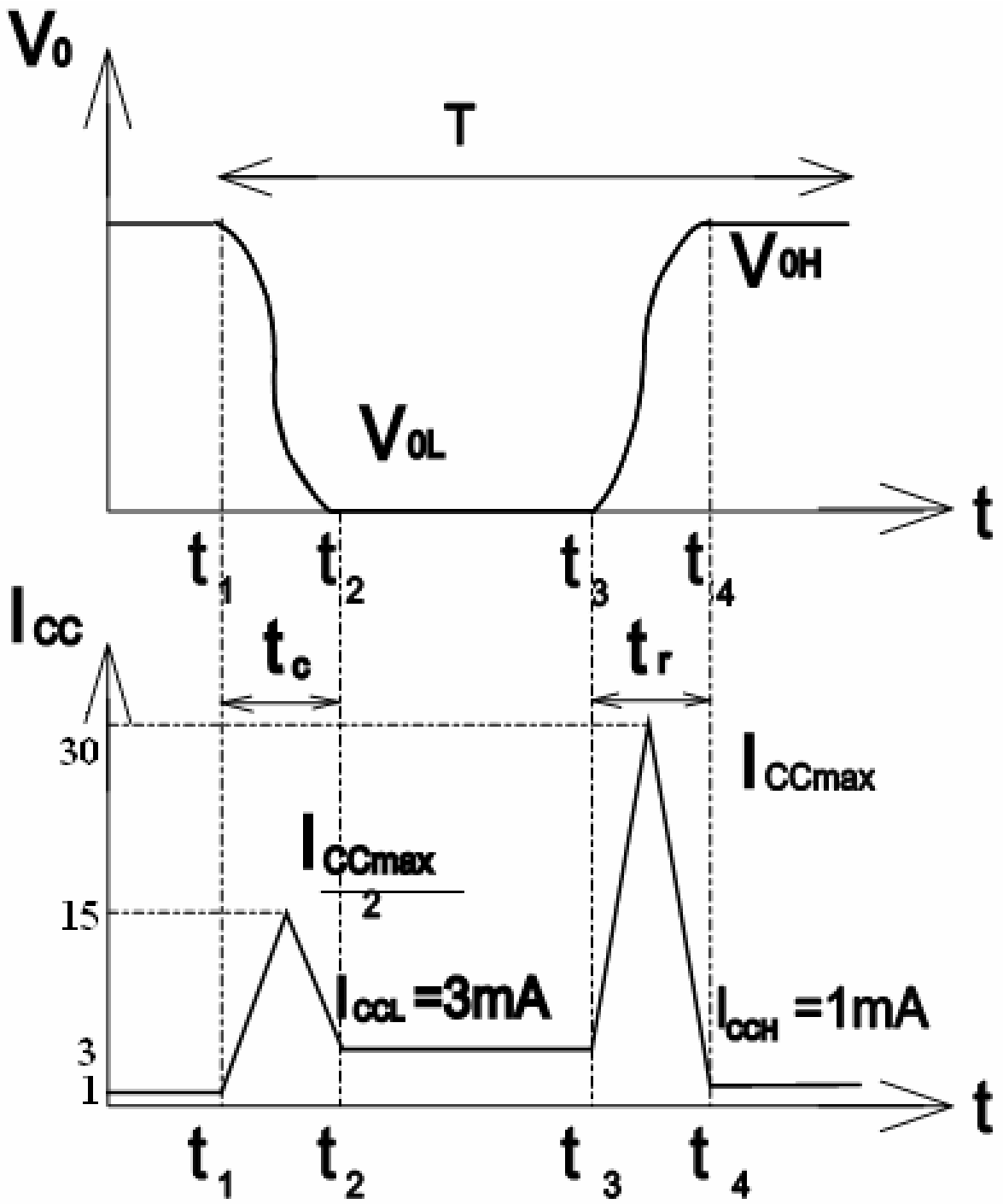
$P_{CC} \approx 10mW$

$P_C=C_p V_{CC}^2 f$

$C_p=15pF$; f=1MHz, $P_C \approx 0,4mW$; f=20MHz, $P_C \approx 7,5mW$

- Besides the two components $P_{CC}$ and $P_C$, there is another, due to simultaneous conduction of transistors $T_3$ and $T_4$. This extra power consumption $P_{DS}$ has the formula:

$$P_{DS} = V_{CC}\left( \frac{I_{CCmax}}{2.2} \cdot \frac{t_c}{T} + \frac{I_{CCmax}}{2} \cdot \frac{t_r}{T} \right)$$


V0
T
V0H
V0L
t
t1
t2
t3
t4
ICC
tc
tr
30
ICCmax
ICCmax/2
15
ICCL=3mA
ICCH=1mA
3
1
t
t1
t2
t3
t4

# Propagation Delay

- Given by charging/discharging times of stray capacitance from gate's output and by switching times of transistors
- $t_{pHL} = t_{c1} + t_{des}$
- $t_{pLH} = t_{c2} + t_{inc}$
- $t_{pd} = (t_{pHL} + t_{pLH})/2$
- Switching times: $t_{c1}$ = 5ns and $t_{c2}$ = 8ns
- Charging/discharging times of stray capacitances:

$$t_{des} = C_p \frac{V_{OH} - V_{OL}}{I_{OL}} \qquad t_{inc} = C_p \frac{V_{OH} - V_{OL}}{I_{OH}}$$

- Formula for $t_{inc}$, short-circuit current value is considered $I_{OS}$
- For $I_{OS}$ = 18mA results $t_{inc}$ = 2.5ns
- Calculated values: $t_{pHL}$ = 8ns şi $t_{pLH}$ = 10.5ns
- Data book values: $t_{pHL}$ = 8ns and $t_{pLH}$= 12ns, resulting $t_{pd}$ = 10ns

# Proposed Problems

- Find out the maximum value of a resistor may be connected between two standard TTL gates, without modifying the circuit behavior. How this resistor is affecting the noise margins?
- Design a circuit based on a NAND TTL standard gate, able to drive a LED. For the LED, following values are considered: $V_{LED}$=1,6V and $I_{LED}$=10mA.
- Design a circuit based on a NOR TTL standard gate, able to drive a LED. For the LED, following values are considered: $V_{LED}$=0,65V and $I_{LED}$=20mA.
- Design a positive edge detector circuit, using NAND gates.
- If a pulse train signal is propagating through a NAND gate, how this influences the filling factor of one pulse? But if propagating through two NAND gates? Input signal has a 20MHz frequency and a filling factor of ½.