

## Laboratory 1

Expected delivery of lab\_01.zip including:

- program\_1.s
- lab\_01.pdf (fill and export this file to pdf)

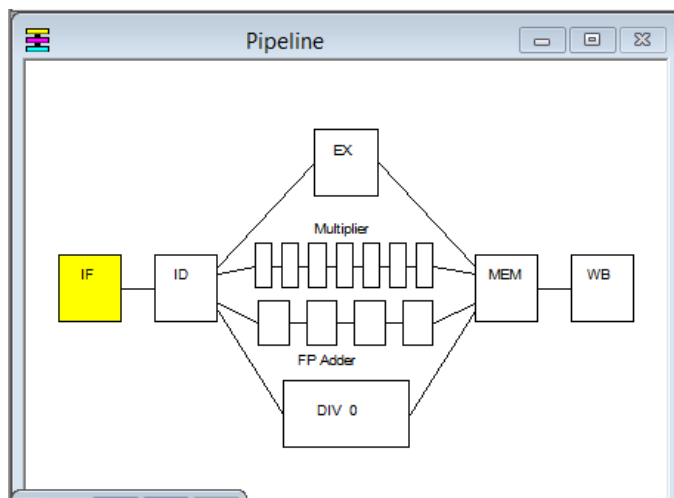
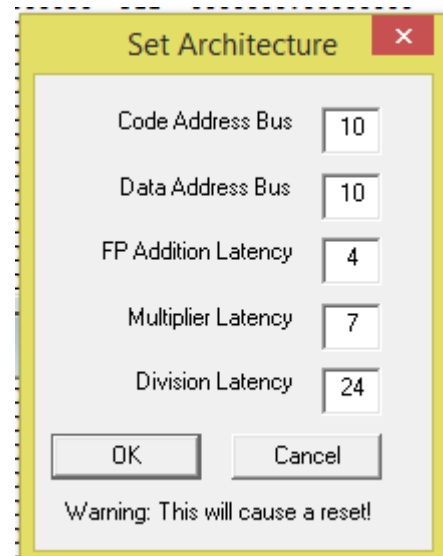
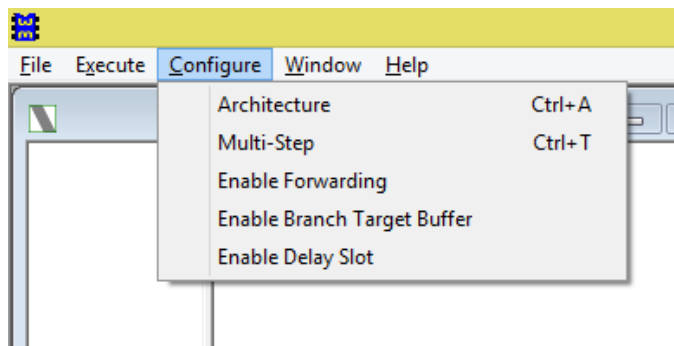
Please, configure the winMIPS64 processor architecture with the *Base Configuration* provided in the following:

- Integer ALU: 1 clock cycle
- Data memory: 1 clock cycle
- Branch delay slot: 1 clock cycle
- Code address bus: 12
- Data address bus: 12
- Pipelined FP arithmetic unit (latency): 6 stages
- Pipelined FP multiplier unit (latency): 8 stages
- FP divider unit (latency): not pipelined unit, 28 clock cycles
- Forwarding optimization is disabled
- Branch prediction is disabled
- Branch delay slot optimization is disabled.

Use the Configure menu:

- remove the flags (where activating Enable options)
- Browse the Architecture menu →

Modify the defaults Architectural parameters (where needed)



← Verify in the Pipeline window that the configuration is effective

- 1) Exercise your assembly skills and learn by example about pipeline optimizations.  
To write an assembly program called **program\_1.s (to be delivered)** for the *MIPS64* architecture and to execute it.

The program must:

1. Given 2 arrays a and b, compute  $c[i] = 4 * (a[i] + b[i])$ . Each array contains 30 **16-bit integer numbers**.
2. Search for **both** the maximum and minimum in the array c. The program saves the obtained value in two variables allocated in memory, called max and min respectively.

Identify and use the main components of the simulator:

- a. Running the *WinMIPS* simulator
  - Launch the graphic interface  
...\winMIPS64\winmips64.exe
- b. Assembly and check your program:
  - Load the program from the **File→Open** menu (*CTRL-O*). In the case the of errors, you may use the following command in the command line to compile the program and check the errors:  
...\winMIPS64\asm program\_1.s
- c. Run your program step by step (*F7*), identifying the whole processor behavior in the six simulator windows:  
**Pipeline, Code, Data, Register, Cycles and Statistics**
- d. Enable one at a time the optimization features that were initially disabled and collect statistics to fill the following table **(fill all required data in the table before exporting this file to pdf format to be delivered)**.

Table 1: **Program performance for different processor configurations**

Program	Number of clock cycles			
	No optimization	Forwarding	Branch Target Buffer	Delay Slot
program_1	677	467	619	677

2) Perform execution time measurements.

Search in the winMIPS64 folder the following benchmark programs:

- a. isort.s
- b. mult.s
- c. series.s
- d. program\_1.s (your program)

Starting from the basic configuration with no optimizations, compute by simulation the number of cycles required to execute these programs; in this initial scenario, it is assumed that the programs weight is the same (25%) for everyone. Assume a processor frequency of 15MHz.

Then, change processor configuration and vary the programs weights as following. Compute again the performance for every case and fill the table below **(fill all required data in the table before exporting this file to pdf format to be delivered).**:

- 1) Configuration 1
  - a. Enable Forwarding
  - b. Disable branch target buffer
  - c. Disable Delay Slot
 Assume that the weight of all programs is the same (25%).
- 2) Configuration 2
  - a. Enable Forwarding
  - b. Enable branch target buffer
  - c. Disable Delay Slot
 Assume that the weight of all programs is the same (25%).
- 3) Configuration 3
 

Configuration 1, but assume that the weight of the program *your program* is 50%.
- 4) Configuration 4
 

Configuration 1, but assume that the weight of the program *series.s* is 50%.

**Table 2: Processor performance for different weighted programs**

Program	No opt	Conf. 1	Conf. 2	Conf. 3	Conf. 4
isort.s	$46041 * (1/f)$ = 3.1 ms	$33277 * (1/f)$ = 2.2 ms	$31039 * (1/f)$ = 2.1 ms	$33277 * (1/f)$ = 2.2 ms	$33277 * (1/f)$ = 2.2 ms
mult.s	$1880 * (1/f)$ = 125 $\mu$ s	$980 * (1/f)$ = 65 $\mu$ s	$922 * (1/f)$ = 62 $\mu$ s	$980 * (1/f)$ = 65 $\mu$ s	$980 * (1/f)$ = 65 $\mu$ s
series.s	$550 * (1/f)$ = 37 $\mu$ s	$233 * (1/f)$ = 16 $\mu$ s	$234 * (1/f)$ = 16 $\mu$ s	$233 * (1/f)$ = 16 $\mu$ s	$233 * (1/f)$ = 16 $\mu$ s
program_1.s	$677 * (1/f)$ = 45 $\mu$ s	$467 * (1/f)$ = 31 $\mu$ s	$409 * (1/f)$ = 27 $\mu$ s	$467 * (1/f)$ = 31 $\mu$ s	$467 * (1/f)$ = 31 $\mu$ s
<b>TOTAL TIME</b>	$(0.25 * 3.1ms)$ + $(0.25 * 125\mu s)$ + $(0.25 * 37\mu s)$ + $(0.25 * 45\mu s)$ = 827 $\mu$ s	$(0.25 * 2.2ms)$ + $(0.25 * 65\mu s)$ + $(0.25 * 16\mu s)$ + $(0.25 * 31\mu s)$ = 578 $\mu$ s	$(0.25 * 2.1ms)$ + $(0.25 * 62\mu s)$ + $(0.25 * 16\mu s)$ + $(0.25 * 27\mu s)$ = 551 $\mu$ s	$(0.167 * 2.2ms)$ + $(0.167 * 65\mu s)$ + $(0.167 * 16\mu s)$ + $(0.50 * 31\mu s)$ = 396 $\mu$ s	$(0.167 * 2.2ms)$ + $(0.167 * 65\mu s)$ + $(0.50 * 16\mu s)$ + $(0.167 * 31\mu s)$ = 391 $\mu$ s

For time computations, use a clock frequency of 15MHz.

## **Appendix: winMIPS64 Instruction Set**

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### ***WinMIPS64***

#### **The following assembler directives are supported**

.data - start of data segment  
.text - start of code segment  
.code - start of code segment (same as .text)  
.org <n> - start address  
.space <n> - leave n empty bytes  
.ascii <s> - enters zero terminated ascii string  
.ascii <s> - enter ascii string  
.align <n> - align to n-byte boundary  
.word <n1>,<n2>.. - enters word(s) of data (64-bits)  
.byte <n1>,<n2>.. - enter bytes  
.word32 <n1>,<n2>.. - enters 32 bit number(s)  
.word16 <n1>,<n2>.. - enters 16 bit number(s)  
.double <n1>,<n2>.. - enters floating-point number(s)

where <n> denotes a number like 24, <s> denotes a string like "fred", and  
<n1>,<n2>.. denotes numbers separated by commas.

#### **The following instructions are supported**

lb - load byte  
lbu - load byte unsigned  
sb - store byte  
lh - load 16-bit half-word  
lhu - load 16-bit half word unsigned  
sh - store 16-bit half-word  
lw - load 32-bit word  
lwu - load 32-bit word unsigned  
sw - store 32-bit word  
ld - load 64-bit double-word  
sd - store 64-bit double-word  
ld - load 64-bit floating-point  
sd - store 64-bit floating-point  
halt - stops the program  
  
daddi - add immediate  
daddui - add immediate unsigned  
andi - logical and immediate  
ori - logical or immediate  
xori - exclusive or immediate  
lui - load upper half of register immediate  
slti - set if less than or equal immediate  
sltiu - set if less than or equal immediate unsigned

beq - branch if pair of registers are equal  
bne - branch if pair of registers are not equal  
beqz - branch if register is equal to zero  
bnez - branch if register is not equal to zero  
  
j - jump to address  
jr - jump to address in register  
jal - jump and link to address (call subroutine)  
jalr - jump and link to address in register (call subroutine)  
  
dsll - shift left logical  
dsrl - shift right logical  
dsra - shift right arithmetic  
dsllv - shift left logical by variable amount  
dsrlv - shift right logical by variable amount  
dsrav - shift right arithmetic by variable amount  
movz - move if register equals zero  
movn - move if register not equal to zero  
nop - no operation  
and - logical and  
or - logical or  
xor - logical xor  
slt - set if less than  
sltu - set if less than unsigned  
dadd - add integers  
daddu - add integers unsigned  
dsub - subtract integers  
dsubu - subtract integers unsigned  
  
add.d - add floating-point  
sub.d - subtract floating-point  
mul.d - multiply floating-point  
div.d - divide floating-point  
mov.d - move floating-point  
cvt.d.l - convert 64-bit integer to a double FP format  
cvt.l.d - convert double FP to a 64-bit integer format  
c.lt.d - set FP flag if less than  
c.le.d - set FP flag if less than or equal to  
c.eq.d - set FP flag if equal to  
bc1f - branch to address if FP flag is FALSE  
bc1t - branch to address if FP flag is TRUE  
mtc1 - move data from integer register to FP register  
mfc1 - move data from FP register to integer register