T-46-13-29

Signetics

27C64A
64K CMOS UV Erasable PROM (8K × 8)

Product Specification

Military Application Specific Products

DESCRIPTION

The Signetics 27C64A CMOS EPROM is 64K-Bit 5V only memory organized as 8192 words of 8 bits, employing advanced CMOS circuitry for systems requiring high-power, high performance speeds and immunity to noise

The 27C64A has a non-multiplexed addressing interface and is pin compatible with the standard 2764.

The 27C64A achieves both high performance (200ns access time) and low power consumption (10mA active current maximum, CMOS inputs) making it ideal for high performance portable equipment.

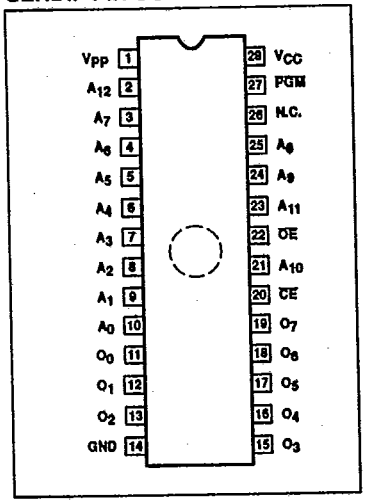
The highest degree of protection against latch-up is achieved through EPI (Epitaxial) processing. Prevention of latch-up is provided for stresses up to 100mA on address and data pins for -1V to V_{CC} + 1V.

The 27C64A is programmed with standard EPROM programmers and the intelligent programming algorithm may be utilized.

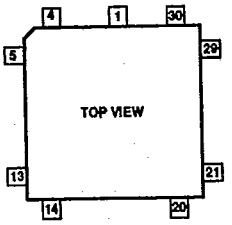
FEATURES

- **CMOS microcontroller and microprocessor compatible**
  - **Universal 28- and 32-Pin memory site, 2-line control**
- **Low power consumption**
  - **10mA maximum active current**
  - **100μA maximum standby current**
- **Noise immunity features**
  - **±10% supply voltage**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **Programs in under one minute**
  - **12.5V_{PP}**

CERDIP PIN CONFIGURATION



LLCC PIN CONFIGURATION



PIN / FUNCTION

1	NC	12	NC	23	$\overline{OE}$
2	V_{PP}	13	O_0	24	A_{10}
3	A_{12}	14	O_1	25	$\overline{CE}$
4	A_7	15	O_2	26	NC
5	A_6	16	V_{SS}	27	A_{11}
6	A_5	17	NC	28	A_9
7	A_4	18	O_3	29	A_8
8	A_3	19	O_4	30	NC
9	A_2	20	O_5	31	$\overline{PGM}$
10	A_1	21	O_6	32	V_{CC}
11	A_0	22	O_7		

PIN NAMES

A_0 - A_{12}	Addresses
O_0 - O_7	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program Strobe
NC	No connect
GND	Ground
V_{PP}	Program Voltage
V_{CC}	Power Supply

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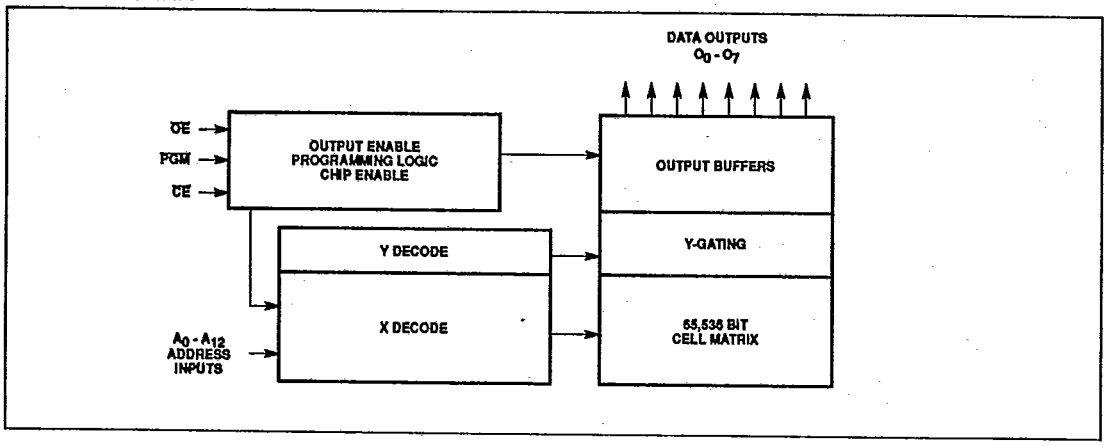
BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGES	ORDER CODE			
	150ns	200ns	250ns	350ns
28-Pin Ceramic DIP w/Quartz Window	27C64A/BXA-15	27C64A/BXA-20	27C64A/BXA-25	27C64A/BXA-35
28-Pin Ceramic DIP w/o Quartz Window[1]	27C64A/BXA-15 OT	27C64A/BXA-20 OT	27C64A/BXA-25 OT	27C64A/BXA-35 OT
32-Pin Rectangular LLCC w/Quartz Window	27C64A/BUA-15	27C64A/BUA-20	27C64A/BUA-25	27C64A/BUA-35

ABSOLUTE MAXIMUM RATINGS[2]

SYMBOL	PARAMETER	RATING	UNIT
T_{STG}	Storage temperature range	-65 to +125	°C
V_I, V_O	Voltage on any pin with respect to ground	-2.0 to V_{CC} +7V	V
V_I	Voltage on $\overline{CE}$ pin with respect to ground	-2.0 to +13.5	V
V_{PP}	Supply voltage with respect to ground during programming	-2.0 to 14.0	V
T_C	Operating temperature during read	-55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}[3]	High-level input voltage		2.0		V_{CC} + 0.5[9]	V
V_{IH}[3]	High-level input voltage CMOS	V_{PP} = V_{CC}	V_{CC} - 0.2		V_{CC} + 0.2[9]	V
V_{IL}[3]	Low-level input voltage	V_{PP} = V_{CC}	-0.5[9]		0.8	V
V_{IL}[3]	Low-level input voltage CMOS	V_{PP} = V_{CC}	-0.2[9]		0.2	V
I_{OH}	High-level output current				-400	µA
I_{OL}	Low-level output current				2.1	mA
V_{PP}	V_{PP} read voltage[8]		V_{CC} - 0.7		V_{CC}	V
T_A	Operating temperature range		-55		+125	°C

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DC ELECTRICAL CHARACTERISTICS $-55\,°C \le T_C \le +125°C$, $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	TEST CONDITIONS	27C64A-15, -20, -25			27C64A-35			UNIT
			Min	Typ[4]	Max	Min	Typ[4]	Max	
I_{LIH}	Input leakage current	$V_I = V_{CC}$ = Max		0.01	+1.0		0.01	+1.0	µA
I_{LIL}		V_I = 0.0V			-1.0			-1.0	
I_{OIH}	Output leakage current	$V_I = V_{CC}$ = Max		0.01	+1.0		0.01	+1.0	µA
I_{OIL}		V_I = 0.0V			-1.0			-1.0	
I_{CC}[5,7] TTL	Operating supply current TTL inputs	$\overline{CE} = \overline{OE}$ - V_{IL}, $V_{PP} = V_{CC}$, O_{0-7} = 0mA			30.0			25.0	mA
I_{CC}[5,7] CMOS	Operating supply current	$\overline{CE} = \overline{OE}$ - V_{IL}, $V_{PP} = V_{CC}$ = Max, O_{0-7} = 0mA			10.0			10.0	mA
I_{SB}[5] TTL	Standby supply current TTL inputs	$\overline{CE} = V_{IH}$, V_{CC} = Max			1.0			1.0	mA
I_{SB}[5,6] CMOS	Standby supply current CMOS inputs	$\overline{CE} = V_{CC}$ = Max			100.0			140.0	µA
I_{PP}[7]	V_{PP} read current	$V_{PP} = V_{CC}$ = Max			100.0			100.0	µA
V_{IL}	Input Low voltage (TTL)	$V_{PP} = V_{CC}$ = Max	-0.5[10]		+0.8	-0.5[10]		+0.8	V
V_{IL}	Input Low voltage (CMOS)	$V_{PP} = V_{CC}$ = Max	-0.2[10]		+0.2	-0.2[10]		+0.2	V
V_{IH}	Input High voltage	$V_{PP} = V_{CC}$ = Min	2.0		V_{CC} + 0.5[10]	2.0		V_{CC} + 0.5[10]	V
V_{IH}	Input High voltage (CMOS)	$V_{PP} = V_{CC}$ = Min	V_{CC} - 0.2		V_{CC} + 0.2[10]	V_{CC} - 0.2		V_{CC} + 0.2[10]	V
V_{OL}	Output Low voltage	I_{OL} = Max, V_{CC} = Min			0.45			0.45	V
V_{OH}	Output High voltage	I_{OH} = Max, V_{CC} = Min	2.4			2.4			V
I_{OS}[8]	Output short-circuit current	V_{CC} = Max			-100.0			-100.0	mA

CAPACITANCE $T_A = 25°C$, f = 1.0MHz[10]

SYMBOL	PARAMETER	TEST CONDITIONS	MAX	UNIT
C_I	Address/control capacitance	V_I = 0V	6	pF
C_O	Output capacitance	V_O = 0V	12	pF

READ MODES

MODE	PINS				
	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	OUTPUTS (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_O
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X[12]	X[12]	V_{CC}	Hi-Z

READ MODE

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{CE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a Standby mode which reduces the maximum V_{CC} current to 100µA. The device is placed in the Standby mode when $\overline{CE}$ pin is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

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READ OPERATION - AC CHARACTERISTICS $-55\,°C \le T_C \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

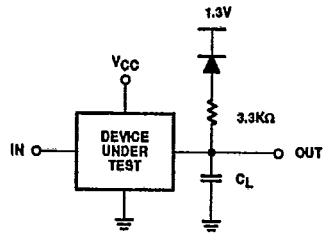
VERSIONS		27C64A-15		27C64A-20		27C64A-25		27C64A-35		UNIT
SYMBOL	CHARACTERISTIC[11]	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to output delay		150		200		250		350	ns
t_{CE}	$\overline{CE}$ to output delay		150		200		250		350	ns
t_{OE}	$\overline{OE}$ to output delay		65		75		100		120	ns
t_{OP}[10]	$\overline{OE}$ or $\overline{CE}$ High to output Hi-Z		40		55		55		75	ns
t_{OH}[10]	Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change - whichever is first	0		0		0		0		ns

ERASURE CHARACTERISTICS

The recommended erasure procedure for the 27C64A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The 27C64A should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C64A can be exposed to without damage is 7258µW/cm^2 (1 week @ 12,000Wsec/cm^2). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

The erasure characteristics of the 27C64A are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C64A in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C64A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

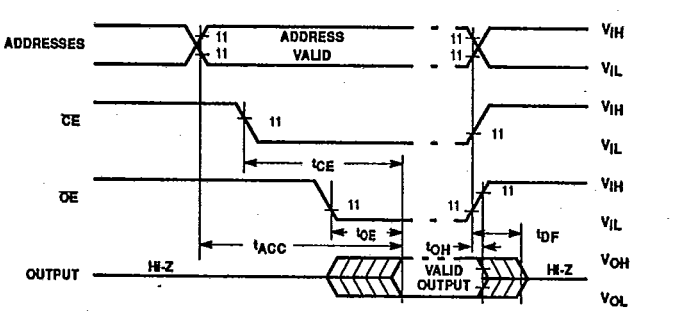
AC TESTING LOAD CIRCUIT



NOTE:
C_C = 100pF AND INCLUDES JIG CAPACITANCE

Figure 1. Test Configuration

AC WAVEFORMS



Input Pulse Characteristics: t_r, $t_f \le 5ns$, P_{RR} = 1MHz; for measurement points see Note 11.

PROGRAMMING MODES

MODES	PINS							
	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	A_9 (24)	A_0 (10)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
Intelligent programming	V_{IL}	V_{IH}	V_{IL}	X[12]	X[12]	V_{PP}	6.0V[15]	D_1
Program verify	V_{IH}	V_{IL}	V_{IH}	X[12]	X[12]	V_{PP}	6.0V[15]	D_0
Program inhibit	V_{IH}	V_{IH}	X	X[12]	X[12]	V_{PP}	6.0V[15]	Hi-Z
Intelligent identifier-manufacturer[14]	V_{IL}	V_{IL}	V_{IL}	V_H[13]	V_{IL}	V_{CC}	V_{CC}	15H
Intelligent identifier[14]	V_{IL}	V_{IL}	V_{IL}	V_H[13]	V_{IH}	V_{CC}	V_{CC}	OBH

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CMOS NOISE CHARACTERISTICS

Special epitaxial processing techniques have enabled Signetics to build CMOS with features adding to system reliability. These include Input/Output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100mA and voltages from -1V to V_{CC} + 1V.

Additionally, the V_{PP} (Programming) pin is designed to resist latch-up to the 14V maximum device limit.

PROGRAMMING

Caution: Exceeding 14.0V on V_{PP} pin may permanently damage the 27C64A.

Initially, and after each erasure, all bits of the 27C64A are in the "1" state. Data is introduced by selectively programming "0" into the desired bit locations. Although only "0" will be programmed, both "1" and "0" can be present in the data word. The only way to change an "0" to a "1" is by ultraviolet light erasure.

The 27C64A is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

INTELLIGENT PROGRAMMING ALGORITHM

The 27C64A intelligent programming algorithms rapidly program Signetics CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flow-chart of the 27C64A intelligent program algorithm is shown in Figure 2.

The intelligent programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3Xms. X is a duration counter and is equal to the number of the initial 1ms pulses applied to a particular 27C64A location, before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

PROGRAM INHIBIT

Programming of multiple 27C64A EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits other 27C64A EPROMs from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27C64A's may be common. A TTL low-level pulse applied to the $\overline{PGM}$ and $\overline{CE}$ input with V_{PP} at 12.5V will program the selected 27C64A.

VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}. Data should be verified a minimum of T_{OEV} after the falling edge of $\overline{OE}$.

INTELLIGENT IDENTIFIER MODE

The intelligent identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C64A.

To activate this mode the programming equipment must force 11.5V to 12.5V on address line A_9 of the 27C64A. Two bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during intelligent identifier mode.

INTELLIGENT PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.5V ± 0.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
I_I	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input low level (all inputs		-0.1	0.8	V
V_{IH}	Input High level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	$O_0 - O_7$ = 0mA		30	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		30	mA

AC PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[16]	LIMITS			UNIT
			Min	Typ	Max	
t_{CES}	$\overline{OE}$ setup time		2			µs
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}[19]	$\overline{OE}$ High to output float delay		0		130	µs
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{PW}	$\overline{PGM}$ Initial program pulse width	(See note 17)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ overprogram pulse width	(See note 18)	2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

NOTES:
1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Minimum DC input voltage is -0.5V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Typical limits are at V_{CC} = 5V, T_A = + 25°C.
5. TTL inputs: spec V_{IL}, V_{IH} levels;
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
6. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
7. Maximum active power usage is the sum $I_{PP} + I_{CC}$.
8. Output shorted for no more than one second. No more than one output shorted at a time.
9. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.
10. Guaranteed, but not tested.
11. AC characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
12. X can be V_{IL} or V_{IH}.
13. V_H = 12.0V ± 0.5V.
14. A_1 - A_8, A_{10} - A_{12} = V_{IL}.
15. V_{CO} = 6.0V ± 0.25V.
16. AC Conditions of Test:
    Input Rise and Fall Times (100% to 90%): 20ns
    Input Pulse Levels: 0.45V to 2.4V
    Input Timing Reference Level: 0.8V to 2.0V
    Output Timing Reference Level: 0.8V to 2.0V
17. Initial Program Pulse width tolerance is 1msec ± 5%.
18. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
19. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven (see Timing Diagram).

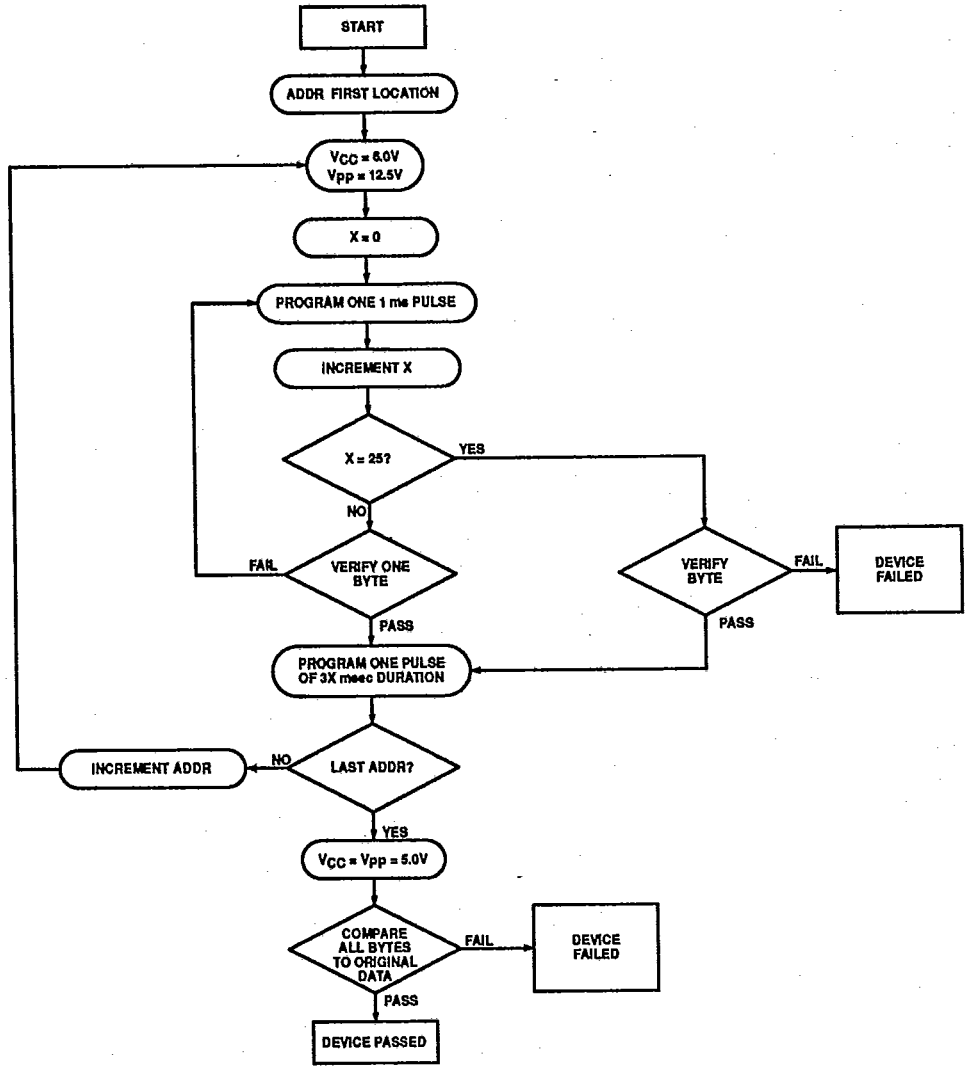

Figure 2. Intelligent Programming Flowchart

64K CMOS UV Erasable PROM (8K×8) 27C64A

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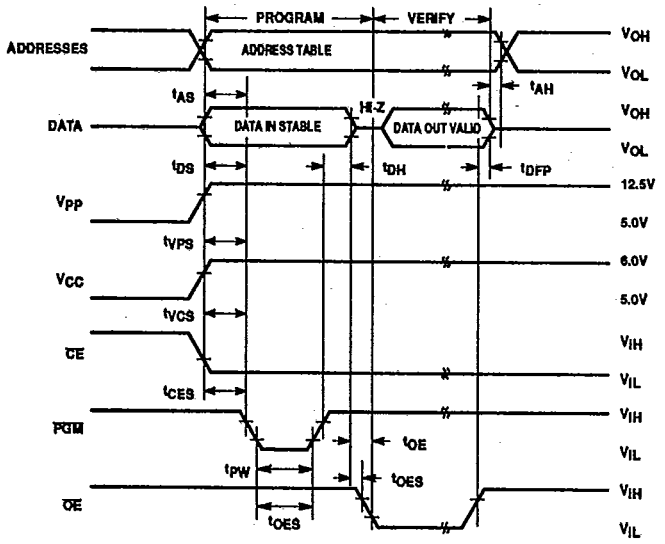

NOTES:
1. The Input Timing Regerence Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming 27C64A, a 0.1uF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

Figure 3. Intelligent Programming Waveform