Module 2 Assignment

7nm FinFET Device and Inverter Characterization

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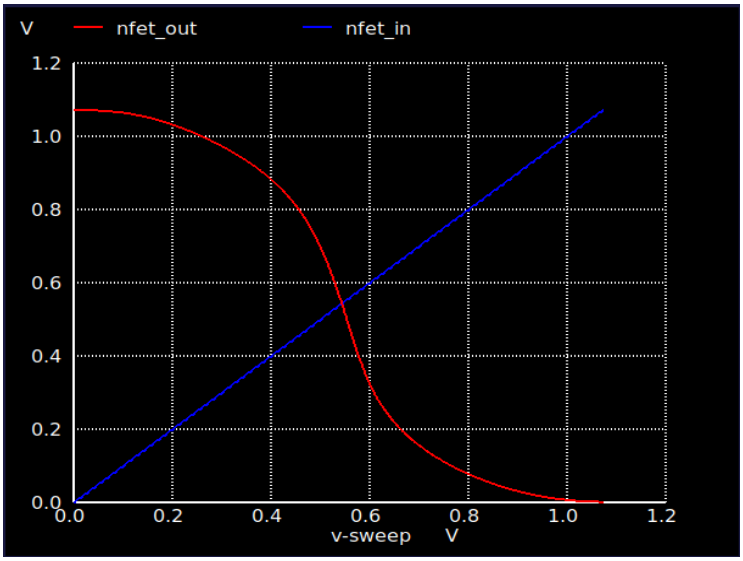
For my username ***gjjaswanth*** the ASCII sum in mV is 1.073.

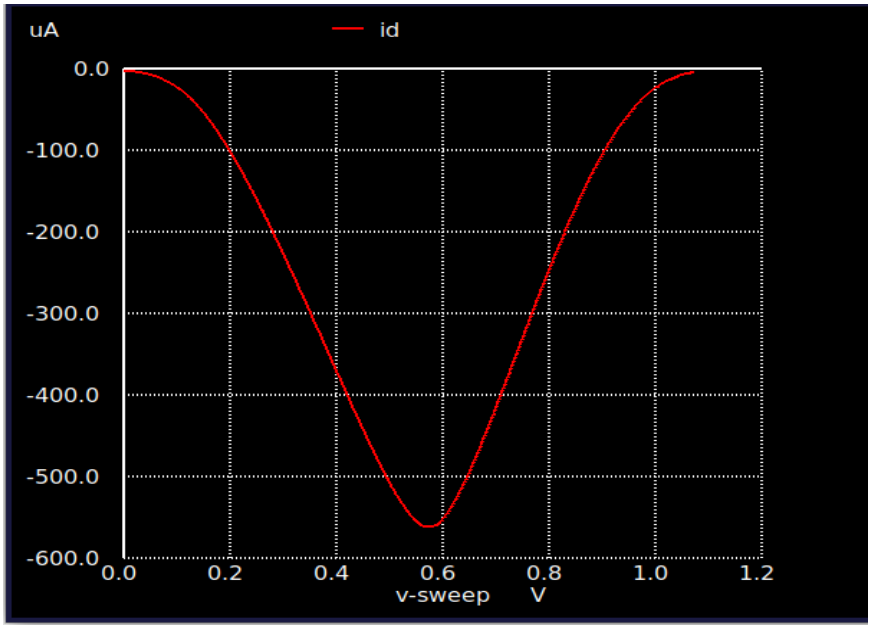
So i have taken voltage as 1.073V for V2.

1.VTC Curve

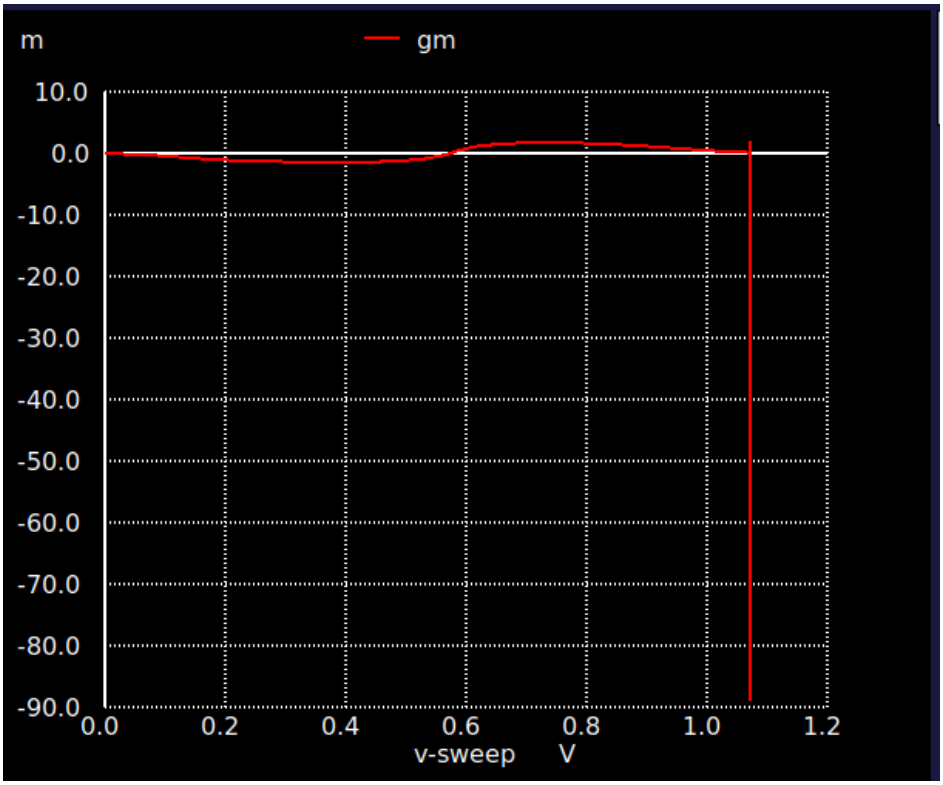


- This curve shows the relation between the input and output voltage of the inverter.
- Vth - is the point where both the curves(lines) intersect.
- Vth = 0.543V

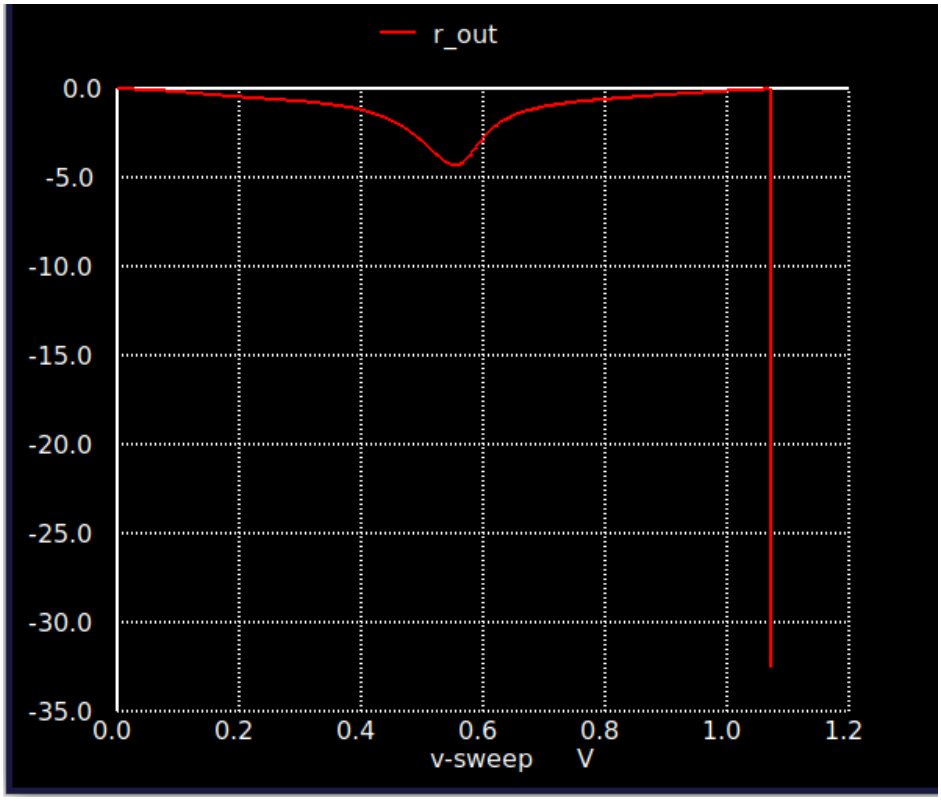
2.Drain Current(Id) = 564uA



3.Transconductance(gm)



4.Output Resistance(r_out)



5. Max Gain, Noise Margin & Transconductance

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No. of Data Rows : 1074
v_th                 =  5.430339e-01
max_gain             =  4.301872e+00 at=  5.560000e-01
vil                  =  5.536459e-01
voh                  =  4.979529e-01
vih                  =  5.579859e-01
vol                  =  4.792880e-01
v_th = 5.430339e-01
max_gain = 4.301872e+00
vil = 5.536459e-01
voh = 4.979529e-01
vih = 5.579859e-01
vol = 4.792880e-01
nmh = -6.00330e-02
nml = 7.435790e-02
gm_max               =  2.081076e-03 at=  1.071000e+00
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
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6.Power consumption and propagation delay

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Initial Transient Solution
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Node                                   Voltage
----                                   -------
nfet_out                               1.07218
nfet_in                                      0
vdd                                      1.073
v2#branch                           -2.1627e-06
v1#branch                           2.06213e-11

 Reference value :  2.15000e-11
No. of Data Rows : 120
tpr                  =  2.500000e-11
tpf                  =  2.562997e-11
id_pwr               =  -4.93099e-15 from=  2.00000e-11 to=  6.00000e-11
tpr = 2.500000e-11
tpf = 2.562997e-11
tp = 2.531498e-11
id_pwr = -4.93099e-15
pwr = -5.29096e-15
power = 1.322739e-04
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver
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7. Frequency

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Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
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Node                                    Voltage
----                                    -------
nfet_out                                1.07218
nfet_in                                       0
vdd                                       1.073
v2#branch                           -2.1627e-06
v1#branch                           2.06213e-11


No. of Data Rows : 71
tr                  =  2.100000e-11
tf                  =  2.321015e-11
t_delay = 4.421015e-11
f = 2.261924e+10
```

Characterization Table:

S. No	W/L (PMOS)	W/L (NMOS)	Vth (V)	Id (uA)	P (W)	tpd (ps)	Av	f (Hz)
1	0.5	2	0.439	472	9.131158e-05	2.472593e-11	4.597815e+00	2.303233e+10
2	3	2	0.6023	632	1.564404e-04	2.563707e-11	4.511432e+00	2.233846e+10
3	2	0.5	0.641	670	8.671761e-05	2.589069e-11	4.776468e+00	2.202725e+10
4	2	2	0.543	546	1.322739e-04	2.531498e-11	4.301872e+00	2.261924e+10
5	2	4	0.439	784	1.826231e-04	2.472593e-11	4.597815e+00	2.303233e+10

Observations:

When the **width of NMOS or PMOS is increased**, the transistor becomes **stronger** (lower resistance), which directly affects current, delay, power, and switching point.

Increasing NMOS Width

- Increases pull-down strength → **higher drain current**
- Output discharges faster → **reduced fall delay**
- Inverter switches earlier → **Vth shifts lower**

Increasing PMOS Width

- Increases pull-up strength → **higher current during charging**
- Output charges faster → **reduced rise delay**
- Inverter switches later → **Vth shifts higher**
- Power consumption **increases**

Balanced PMOS and NMOS Width

- Pull-up and pull-down strengths are comparable
- **Switching threshold near VDD/2**
- Nearly equal rise and fall delays
- **Optimal trade-off** between speed and power

Key Takeaway

Increasing transistor width improves **speed** but at the cost of **higher power**, and the **PMOS/NMOS width ratio controls the inverter switching point** and delay symmetry.