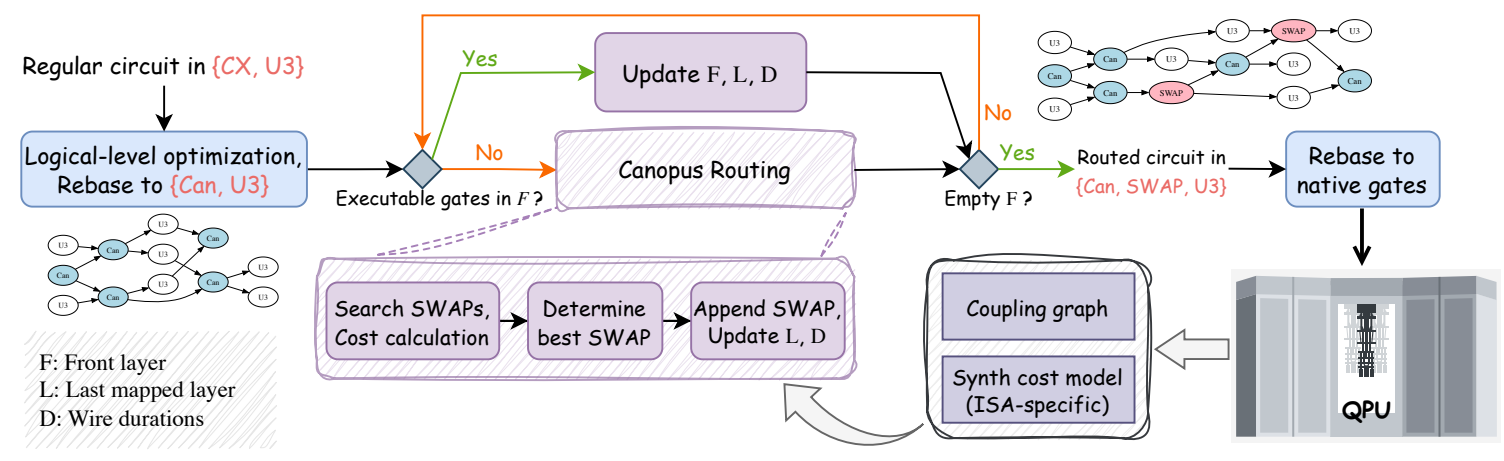
Regular circuit in {CX, U3}
Logical-level optimization, Rebase to {Can, U3}
Executable gates in F ?
Yes
No
Update F, L, D
Canopus Routing
Empty F ?
No
Yes
Routed circuit in {Can, SWAP, U3}
Rebase to native gates
Search SWAPs, Cost calculation
Determine best SWAP
Append SWAP, Update L, D
Coupling graph
Synth cost model (ISA-specific)
QPU
F: Front layer
L: Last mapped layer
D: Wire durations