

Qubit Mapping and Routing tailored to Advanced Quantum ISAs: Not as Costly as You Think

Abstract

We propose CANOPUS (**C**anonical-**O**ptimized **P**lacement **U**tility **S**uite), a qubit mapping/routing framework tailored to advanced quantum ISAs adaptive to versatile hardware architectures.

1 Introduction

Advanced ISAs—Can [1], \sqrt{i} SWAP [2]

CANOPUS (**C**anonical-**O**ptimized **P**lacement **U**tility **S**uite) is a qubit mapping and routing framework that is tailored to advanced quantum ISAs, such as Can [1] and \sqrt{i} SWAP [2], which are adaptive to versatile hardware architectures. CANOPUS is designed to optimize the placement of qubits and the routing of quantum gates, taking into account the specific requirements of these advanced ISAs.

2 Background

2.1 Qubit mapping/routing

2.2 Quantum gates realization in diverse ISAs

3 Motivation

Two-fold motivations:

1. The scalable qubit routing effects (2x-4x) is still a critical challenge in practical quantum computing systems
2. How to utilize the emerging advanced ISAs (hardware breakthroughs); across all phases of compilation, routing is the bottleneck and is the most easily handled for co-optimization

[ZY: Use a “optimal routing benchmark” to illustrate the OVERHEAD of existing methods]

[ZY: There should be many takeaways]

- Previous routing overhead is not precise for hardware execution
- Previous routing is costly and also not precise for hardware execution
- SWAP can be implemented in low overhead (gate duration) with the recent breakthrough gate schemes for advanced ISAs
- How to efficiently capture the rich commutation relations when performing co-optimization during qubit routing and gate scheduling

4 CANOPUS framework

4.1 Overview

4.2 2Q synthesis cost modeling

4.3 Routing in canonical form

- Unified and highly-effective qubit routing approach in canonical form, with properties of quantum ISAs tailored to the routing process

4.4 Enhanced optimization via commutation

- Capture optimization opportunities exposed by gate commutation; while commutation relations can be uniformly described in canonical form

Theorem 1 (Canonical gate commutation). *Let $\text{Can}(a, b, c)_{q_0, q_1}$ and $\text{Can}(a', b', c')_{q_1, q_2}$ be two canonical gates acting on qubits (q_0, q_1) and (q_1, q_2) respectively, with an overlapping qubit q_1 . They are commutative “if and only if”*

$$b = b' = c = c' = 0, \quad (1)$$

that is, when both consist solely of XX rotations.

[ZY: Proposition?? Theorem?]

5 Implementation

5.1 Core functionalities

5.2 Extensions

5.3 Scalability

6 Case Studies

6.1 QFT kernel

6.2 Co-exploration of routing and ISA selection

6.3 Stabilizer circuit

6.4 Mapping on FTQC architecture

7 Evaluation

8 Related Works

9 Conclusion

References

- [1] Jianxin Chen, Dawei Ding, Weiyuan Gong, Cupjin Huang, and Qi Ye. 2024. One Gate Scheme to Rule Them All: Introducing a Complex Yet Reduced Instruction Set for Quantum Computing. In *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2*. ACM, La Jolla, CA, USA, 779–796.
- [2] Cupjin Huang, Tenghui Wang, Feng Wu, Dawei Ding, Qi Ye, Linghang Kong, Fang Zhang, Xiaotong Ni, Zhijun Song, Yaoyun Shi, Hui-Hai Zhao, Chunqing Deng, and Jianxin Chen. 2023. Quantum Instruction Set Design for Performance. *Physical Review Letters* 130 (Feb 2023), 070601. Issue 7. doi:10.1103/PhysRevLett.130.070601

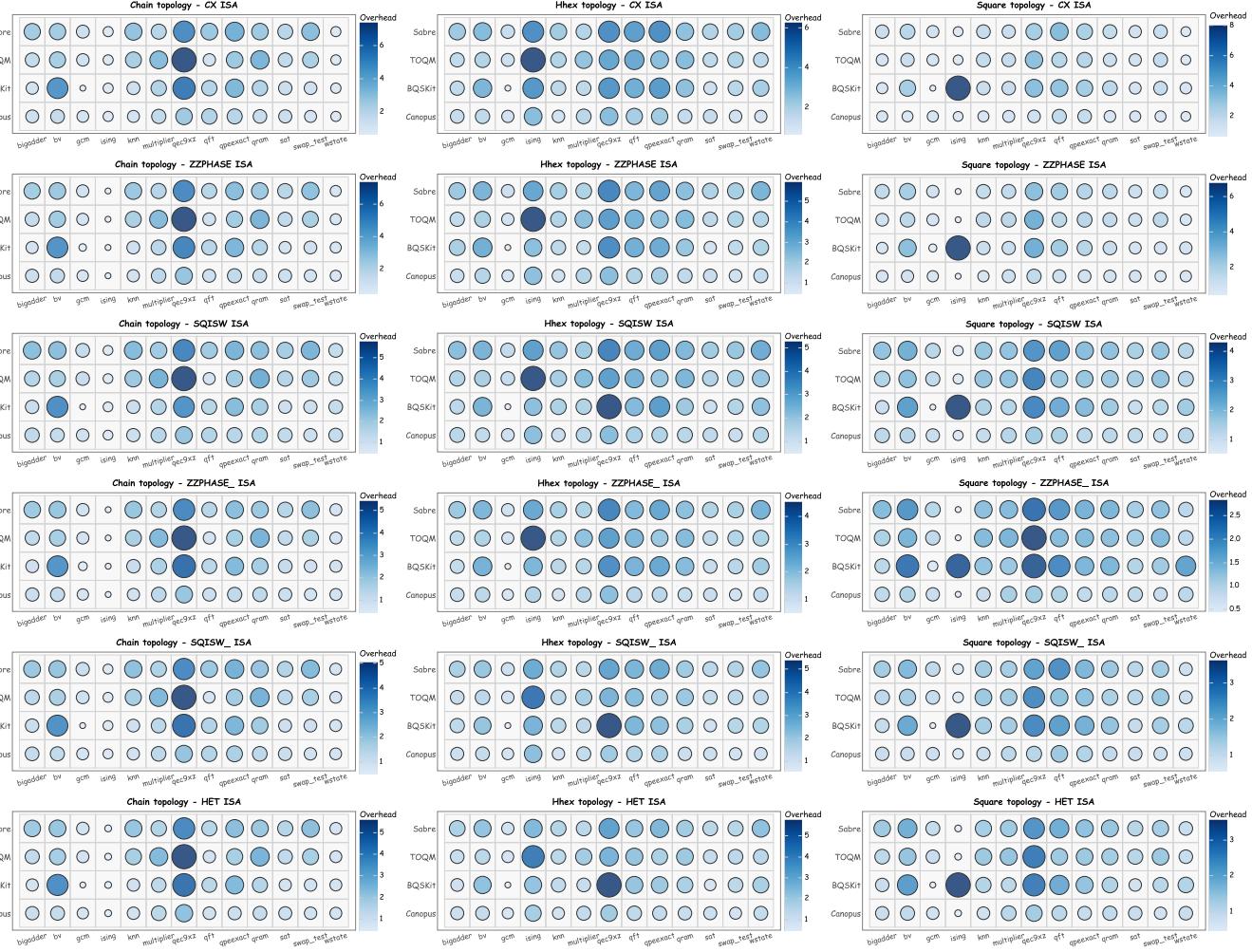


Figure 1. Detailed benchmarking results for different compilers (SABRE, TOQM, BQSKit, CANOPUS) across diverse topologies (columns from left to right: 1D Chain, 2D HHex, 2D Square) and quantum ISAs (rows from top to bottom: CX, ZZPhase, SQiSW, ZZPhase₊, SQiSW₊, Het). Sizes and colors of the bubbles represent the values for routing overhead (multiples of the routed and rebased circuits compared to that of prior-routing ones).

- [3] Ang Li, Samuel Stein, Sriram Krishnamoorthy, and James Ang. 2023. Qasmbench: A low-level quantum benchmark suite for nisq evaluation and simulation. *ACM Transactions on Quantum Computing* 4, 2 (2023), 1–26.
- [4] Nils Quetschlich, Lukas Burgholzer, and Robert Wille. 2023. MQT Bench: Benchmarking software and design automation tools for quantum computing. *Quantum* 7 (2023), 1062.

Table 1. Benchmarks information. These metrics are collected from the circuits after logical-level optimization by TKET, thus including only Can and U3 gates. Circuit cost (Duration T) is calculated in CXISA.

Program	#Qubit	#Can	Depth2Q	Circuit cost
bigadder [3]	18	114	79	88.0
bv [3]	19	18	18	18.0
gcm [3]	13	377	376	510.0
ising [3]	26	25	2	4.0
knn [3]	25	72	50	62.0
multiplier [3]	15	198	122	133.0
qec9xz [3]	17	32	12	12.0
qft [4]	18	153	33	66.0
qpeexact [4]	16	127	43	86.0
qram [3]	20	110	70	78.0
sat [3]	11	210	182	204.0
swap_test [3]	25	72	50	62.0
wstate [3]	27	52	28	28.0

Table 2. Summarized results for the routing overhead with average (geometric-mean) values emphasized.

Topology	Routing overhead (CX)				Routing overhead (ZZPhase)			
	Sabre	TOQM	BQSKit	Canopus	Sabre	TOQM	BQSKit	Canopus
Chain	2.94x	2.67x	2.33x	1.84x	2.66x	2.52x	2.11x	1.64x
HHex	2.93x	2.56x	2.65x	1.85x	2.63x	2.37x	2.29x	1.70x
Square	2.18x	2.02x	2.42x	1.44x	1.89x	1.79x	1.92x	1.21x
Routing overhead (SQiSW)				Routing overhead (ZZPhase_)				
Topology	Sabre	TOQM	BQSKit	Canopus	Sabre	TOQM	BQSKit	Canopus
Chain	2.58x	2.26x	1.97x	1.66x	2.10x	1.94x	1.81x	1.33x
HHex	2.61x	2.33x	2.29x	1.69x	2.09x	1.90x	1.97x	1.34x
Square	2.08x	1.91x	1.99x	1.42x	1.57x	1.47x	1.66x	1.01x
Routing overhead (SQiSW_)				Routing overhead (Het)				
Topology	Sabre	TOQM	BQSKit	Canopus	Sabre	TOQM	BQSKit	Canopus
Chain	2.18x	1.93x	1.76x	1.44x	2.15x	2.00x	1.69x	1.32x
HHex	2.20x	1.94x	2.12x	1.48x	2.15x	1.94x	1.97x	1.39x
Square	1.70x	1.56x	1.79x	1.18x	1.60x	1.50x	1.57x	1.04x

A Canonical gate and 2Q circuit synthesis

B Optimal gate duration with Can ISA

C Commutation relation between canonical gates

Herein we present detailed proof for Theorem 1, relying on the following two lemmas.