DDR4 Timing Parameters Specification

1. The device used as an example is Micro DDR4_4Gb_x8 MT40A512M8 running at 2133MHz 16-16-16-11. It is internally configured as 16 banks, 4 bank groups with 4 banks for each bank for x8. NUM_ROWS = 2^15 = 32768, NUM_COLS = 2^10 = 1024, Page size = 1KB. Read and write operation to the DDR4 SDRAM are burst oriented, either with a burst length of eight (BL8) or a chopped burst of four (BC4) in a programmed sequence.

2. **Important Timing Parameters**

   From Spec for this device, the basic timing parameters can be obtained as follows:

   CL = 16

   AL = 0

   BL = 8

tRP = 16	Precharge period
tRC = 52	ACTIVATE to ACTIVATE period
tRAS = 36	ACTIVATE to PRECHARGE period
tRCD = 16	ACTIVATE to internal READ or WRITE delay
tCWL = 11	CAS to WRITE LATENCY
tCCD_L = 6	CAS to CAS delay to same bank group
tCCD_S = 4	CAS to CAS delay to different bank group
tRRD_L = 8	ACTIVATE to ACTIVATE delay to same bank group
tRRD_S = 5	ACTIVATE to ACTIVATE delay to different bank group
tFAW = 23	Four active window

tWTR_S = 3 Delay from end of internal write transaction to internal read command to a different Bank Group.

tWTR_L = 8 Delay from end of internal write transaction to internal read command to same Bank Group.

tRTP = 6 READ_TO_PRE_DELAY

tWR = 16 minimum write recovery time

tRFC1 = 260 1x Refresh Time

tCKE = 7

tXP=5

Some new features about DDR4:

1. DDR4 supports Command Address Latency, CAL, which is the delay in clock cycles between CS_n and CMD/ADDR.

2. Changed Preamble. DDR4 will support a programmable write preamble, 1tCK and 2tCK modes selected by MRS. Not considered in Dramsim2 yet.

3. Calculation on Delay

RL = AL + CL Delay from read command and start of read transaction

WL = CWL + AL Delay from write command and start of write transaction

READ_TO_READ_DELAY_ bg = max(CCDS, BL/2) + BL/2 //same bank group

READ_TO_READ_DELAY_ dbg = max(CCDL, BL/2) +BL/2//different bank group

READ_TO_WRITE_DELAY= RL + BL/2 + tRTRS - WL //Will change as write preamble change, apply for same/different bank group.

READ_TO_PRE_DELAY = AL + BL/2 + max(tRTP, tCCDS) - tCCDS

READ_AUTOPRE_DELAY = AL+ BL/2 + tRTP+ tRP

READ_TO_READ_DELAY_R = BL/2 + tRTRS //interrank

READ_TO_WRITE_DELAY_R = RL + BL/2 + tRTRS - WL //interrank

WRITE_TO_PRE_DELAY = WL + BL/2 + tWR

WRITE_AUTOPRE_DELAY=WL+BL/2+tWR+Trp

WRITE_TO_WRITE_DELAY_bg = max(CCDS, BL/2) //same bank group

WRITE_TO_WRITE_DELAY_dbg = max(CCDL, BL/2) //different bank group

WRITE_TO_READ_DELAY_bg = WL + BL/2 + tWTRL

WRITE_TO_READ_DELAY_dbg = WL + BL/2 + tWTRS

WRITE_TO_READ_DELAY_R = WL + BL/2 + tRTRS - RL //interrank

WRITE_TO_WRITE_DELAY_R = BL/2 + tRTRS //interrank

PRE_TO_ACT = tRP

ACT_TO_PRE = tRAS

ACT_TO_READ = tRCD + BL/2

ACT_TO_WRITE = tRCD + BL/2

ACT_TO_ACT_bg = tRRDS

ACT_TO_ACT_dbg = max(tRRDL, tRC)

ACT_TO_ACT_4 = tFAW

READ_TO_POWERDOWN = CL + BL/2 + 1

WRITE_TO_POWERDOWN = CL + BL/2 + WR