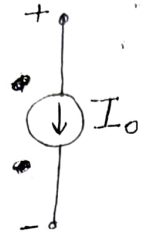
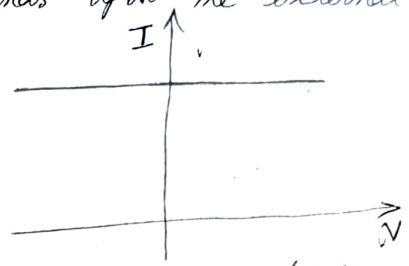
# 3. Current Mirrors and Current Sources/Sinks

Current mirrors, current sources/sinks along with active and passive resistors, capacitors, voltage and current references are the basic building blocks of analog design.

An ideal current source is a 2 terminal element whose current is constant for any voltage across the source. The voltage across a current source depends upon the external circuitry.

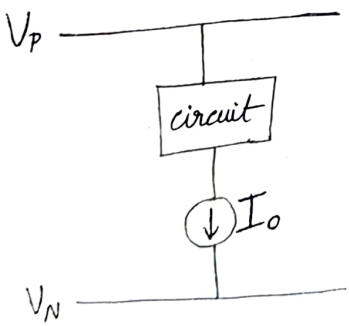



(a) Symbol

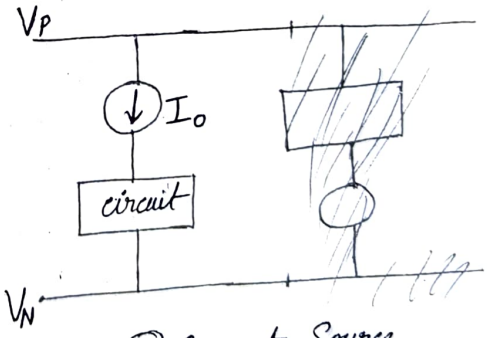



(b) I–V characteristics

Most current source applications require one of their terminals to be common with the most positive or the most negative d.c. voltages in the circuit. This leads to the 2 possible configurations shown below. $V_P$ and $V_N$ are the most +ve & most −ve d.c. voltages resp.



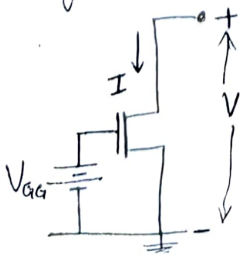

(a) Current Sink

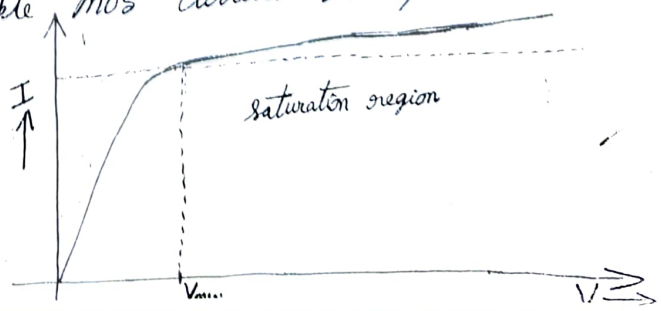



(b) Current Source

A third category is the "floating current source", where neither terminal is connected to $V_P$ or $V_N$.

Fig. below shows a simple MOS current source/sink and its char.



Applications :- Current mirrors and current sources are widely u. in analog ICs.

1. Current sources are used as biasing elements for amplifier stages. Because they are insensitive to power supply & temperature variations.

2. They are used as load devices for amplifiers. Because a current source has high incremental resistance, that results in high voltage gain at low power supply voltages.

3. Current sources are more economical than resistors in terms of the die area required to fabricate. So they act as large resistors without consuming excessive voltage headroom.

4. In some Digital-to-Analog (D/A) converters employ an array of current sources to produce an analog output proportional to the digital input.

5. Current sources, in conjunction with "current mirrors", can be used for analog signal processing.

Basic

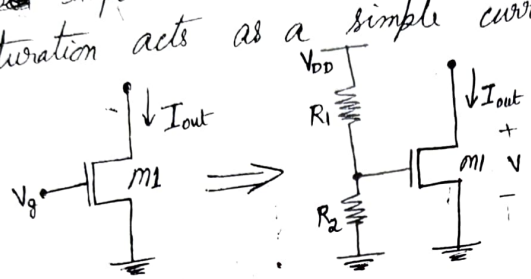
Note :-

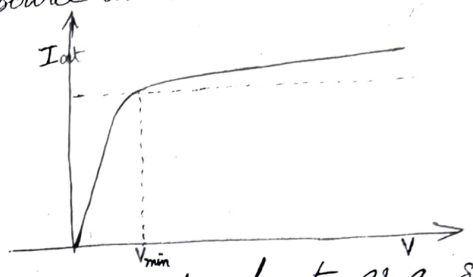
current mi

## Basic current mirrors:-

Note:- There is no clear cut difference between current source and current mirror. A current mirror is also called as current controlled current source (CCCS).

As we know that an ideal current source has ~~(zero input)~~ infinite o/p impedance and capable of supplying a constant current independent of voltage across its terminals. But this ideal current source is ~~impossible~~ impossible to realize. But we know that a simple MOSFET in saturation acts as a simple current source as shown below.



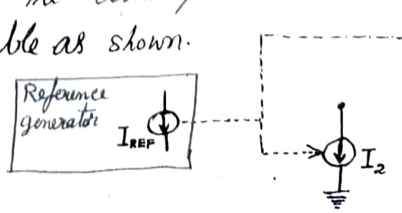

The MOSFET is biased as shown above so as to operate as a stable current source. With the resistive biasing as shown above and assuming M1 is in saturation, we can write,

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[\left(\frac{R_2}{R_1+R_2}\right)V_{DD} - V_{th}\right]^2 \quad \text{—— (1)}$$

(overdrive voltage)

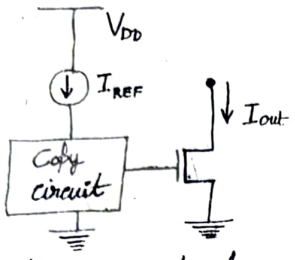
As revealed by the above eqn., Iout depends on supply voltage, process parameters and temperature. The overdrive voltage is a function of $V_{DD}$ and $V_{th}$; the threshold voltage may vary by 100 mV from wafer to wafer. Further more, both $\mu_n$ and $V_{th}$ exhibit temperature dependance. Thus Iout is no more constant and is poorly defined. Even if the gate voltage is not a function of the supply voltage, process and temperature dependencies exist. In other words, even if the gate-source voltage of a MOSFET is precisely defined, its drain current is not. For this reason, we must seek other methods of biasing MOS circuits.

The design of current sources in analog ckts is based on "copying" currents from a reference, with the assumption that one precisely-defined current source is already available as shown.



A relatively complex circuit – sometimes requiring external adjustments is used to generate a stable reference current, $I_{REF}$, which is then copied to many current sources in the system.

## How to generate copies :-



Conceptual means of copying.

Here $I_{out}$ should be equal to $I_{REF}$. For a MOSFET, if $I_D = f(V_{GS})$, then $V_{GS} = f^{-1}(I_{REF})$ as shown in the fig (a) below. Thus, if this voltage is applied to the gate and source terminals of a second MOSFET, the resulting current is,

$I_{out} = f(f^{-1}(I_{REF})) = I_{REF}$ as shown in fig (b) below.

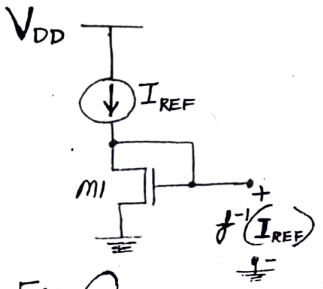


Fig. (a)

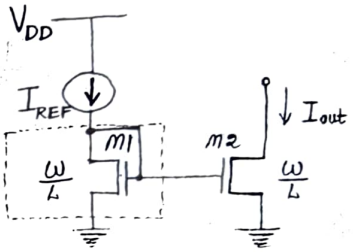


Fig. (b)

From another point of view, 2 identical MOS devices that have equal gate-source voltages and operate in saturation carry equal currents (if $\lambda = 0$).

The structure consisting of M1 and M2 in fig (b) above is called a "current mirror". In the general case, the devices need not be identical. Neglecting channel-length modulation (i.e. $\lambda = 0$), we can write,

$$I_{REF} = \tfrac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{gs} - V_{th})^2$$

$$I_{out} = \tfrac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{gs} - V_{th})^2$$

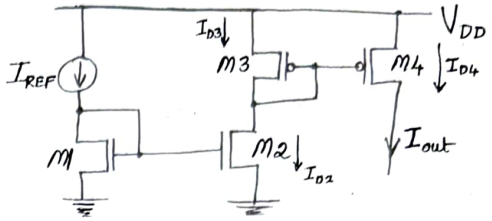
$$\text{or, } \frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

$$\text{or, } I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \quad \text{——— (2)}$$

The key property of this topology is that it allows precise copying of the current with no dependence on process and temperature. The ratio of $I_{out}$ &

$I_{REF}$ is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.

Eg:- ① Find the drain current of M4 in the fig. below, if all of the transistors are in saturation.




We have,

$$I_{D2} = I_{REF}\frac{(W/L)_2}{(W/L)_1}.$$

Also, $|I_{D3}| = |I_{D2}|$ and $I_{D4} = I_{D3}\frac{(W/L)_4}{(W/L)_3}$

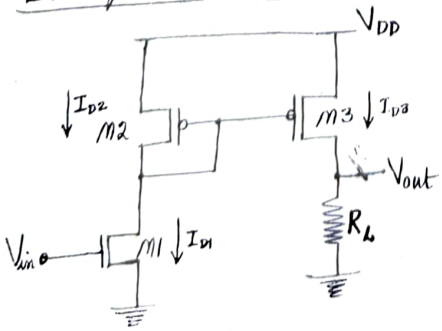
Thus, $|I_{D4}| = \alpha\beta I_{REF}$ where $\alpha = \frac{(W/L)_2}{(W/L)_1}$ and $\beta = \frac{(W/L)_4}{(W/L)_3}$

Current mirrors usually employ the same length for all of the transistors so as to minimize the errors due to the lateral diffusion of the source and drain areas ($L_D$). This is because if, for example, $L_D$ is doubled, then $L_{eff} = L - 2\cdot L_D$ is not. Furthermore, the threshold voltage of short-channel devices exhibits some dependence on the channel length. Thus, current ratioing is achieved by only scaling the width of transistors.

i.e., $I_{out} = \frac{W_2}{W_1} I_{REF}$ ——③

We have also mentioned that current mirrors can process signals as well. For example, if $I_{REF}$ increases by $\Delta I$, then $I_{out}$ increases by $\Delta I\left(\frac{W_2}{W_1}\right)$. That is, the ckt. amplifies the small-signal current if $\frac{W_2}{W_1} > 1$ (but at the cost of proportional multiplication of the bias current)

Example 2:- Calculate the small signal voltage gain of the ckt. shown below.




The small-signal drain current of M1 = $g_{m1} V_{in}$

Since $I_{D2} = I_{D1}$ and $I_{D3} = I_{D2}\frac{(W/L)_3}{(W/L)_2}$

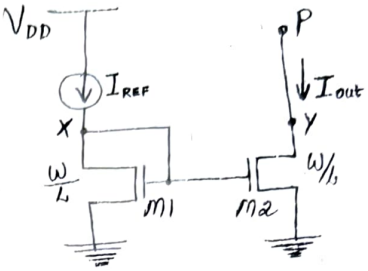
The small-signal drain current of M3, $I_{D3} = g_{m1} V_{in}\frac{(W/L)_3}{(W/L)_2}$

$V_{out} = I_{D3} \cdot R_L$

$\therefore$ voltage gain, $\frac{V_{out}}{V_{in}} = g_{m1} R_L \frac{(W/L)_3}{(W/L)_2}$.

## Cascode current mirrors :-

So far we have neglected channel length modulation. In practice, this effect results in significant error in copying currents, especially if minimum-length transistors are used so as to minimize the width & hence the o/p capacitance of the current source. For the simple mirror shown below, we can write,




$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{gs}-V_t)^2(1+\lambda V_{ds1})$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{gs}-V_t)^2(1+\lambda V_{ds2})$$

Hence,

$$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}\cdot\frac{(1+\lambda V_{ds2})}{(1+\lambda V_{ds1})}$$

while $V_{ds1} = V_{gs1} = V_{gs2}$, $V_{ds2}$ may not equal $V_{gs2}$ because of the circuitry fed by M2.

In order to suppress the effect of channel-length modulation, a cascode current source can be used.

As shown in fig. (a) below, if $V_G$ is chosen such that $V_{DY} = V_X$, then $I_{out}$ closely tracks $I_{REF}$. This is because, ~~as described in connection~~ the cascode device "shields" the bottom transistor from variations in $V_P$.

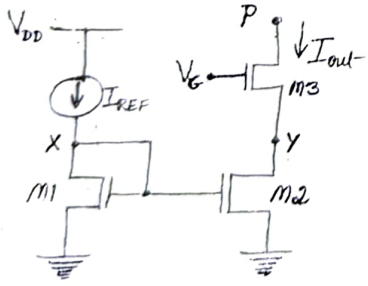



Fig (a)

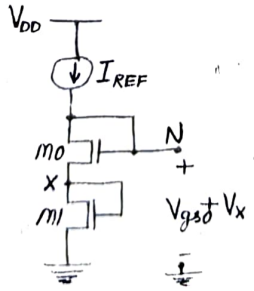



Fig. (b)

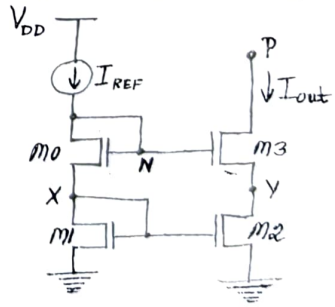


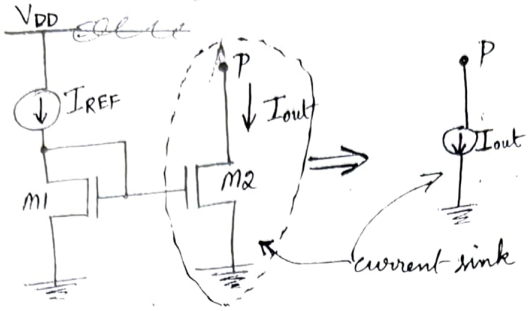

Fig (c)

Thus, we say that $V_Y$ remains close to $V_X$ & hence $I_{REF} \approx I_{out}$ with high accuracy. Such accuracy is obtained at the cost of the voltage headroom consumed by M3.

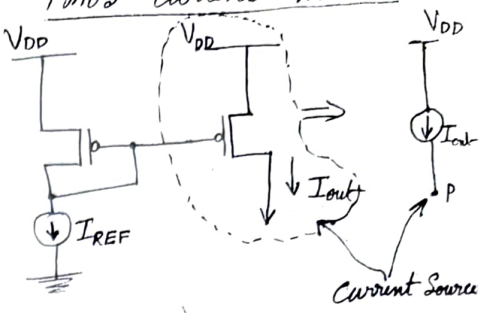
How do we generate $V_G$ in fig (a)? Since the objective is to ensure $V_Y = V_X$, we must guarantee $V_G - V_{gs3} = V_X$ or $V_G = V_{gs3} + V_X$. This result suggests that if a gate-source voltage is added to $V_X$, the required value of $V_G$ can be obtained. Depicted in fig (b), the idea is to place another

## Current mirrors :- [Cover this before starting cascode current mirror]

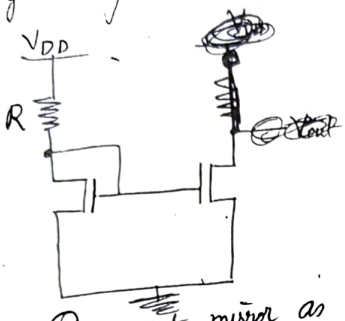
### NMOS current mirror :-



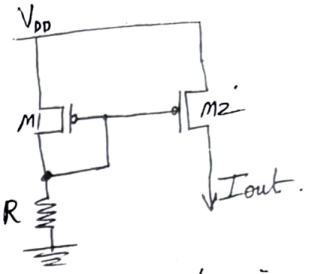

### PMOS current mirror




The simple way of deriving the reference current source $I_{REF}$ is by using a simple resistor.



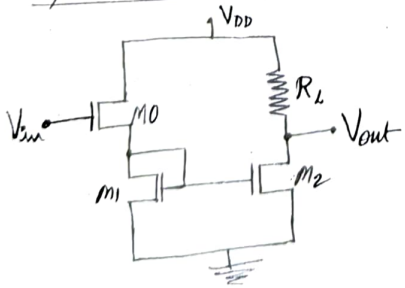

(a) current mirror as sink.

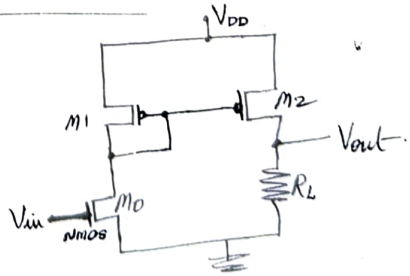



(b) current mirror as source.

If we observe the above figures, in the NMOS case, one terminal of the current mirror is always tied to the most -ve point (ground) in the ckt. and in the PMOS case one terminal of the mirror is always connected to the most +ve point, ($V_{DD}$). So current sinks are made using NMOSs, while current sources are made using PMOSs.

### Signal processing using current mirrors :-



Other topics to be covered in this chapter:-

1. Prove that o/p resistance of simple cascode current mirror is
   $R_o = r_{o4}\left(1 + g_{m4} r_{o2}\right) + r_{o2}$.
2. Layout of the simple current mirror:
3. Matching in MOSFET mirrors
4. Other current sources & Sinks
   a) Wilson current mirror
   b) Regulated cascode current mirror.

Refer to Baker & Boyce page 445 to 455.

Example:
current
source and
Note:

**Example:** Design a current sink using $V_{DD} = -V_{SS} = 2.5\,V$ to sink a current of $10\,\mu A$. Estimate the minimum voltage across the current source and the o/p resistance.

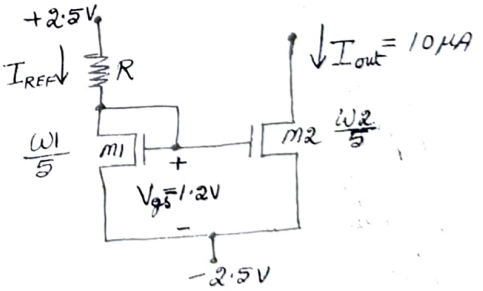
**Note:-** For digital design we used the minimum length, $2.0\,\mu m$ for CN20 process, for our MOSFET switches because we did not care about the o/p resistance of the MOSFET in the saturation region.

For analog design, however, it is extremely important to keep the o/p resistance as high as possible. It is also desirable to reduce the effects of channel length & mobility modulation. These effects are reduced by increasing the channel length of the devices. A general design rule is to set the length of the MOSFETs used in analog applications to two to five times the minimum drawn gate length.

For CN20 process, $\lambda \simeq 0.06/V$ (for N & P MOSFETs). We know that, $r_o = 1/g_o = \frac{1}{\lambda I_{ds}}$. Therefore, when designing with CN20 process, we assume that the length, $L$, of the MOSFETs used in analog applications is atleast $5\,\mu m$.

**Solution:-**

Consider the basic design for a current sink shown below, assuming $L = 5\,\mu m$, $V_{GS} = 1.2\,V$, $V_{th} = 0.83\,V$ and $\lambda = 0.06/V$.




The value of R, assuming $I_{REF} = I_{out} = 10\mu A$, is determined by solving the equations (2)

$$I_{REF} = \frac{K}{2}\frac{W_1}{L_1}(V_{gs1} - V_{th})^2 \quad \text{---(1)}$$

$$I_{REF} = \frac{V_{DD} - V_{gs} - V_{SS}}{R} \quad \text{---(2)}$$

By equating (1) & (2) & solving

$$10\,\mu A = \frac{2.5 - 1.2 - (-2.5)}{R} \quad \text{or} \quad R = 380\,K\Omega$$

$K = \mu C_{ox}$
$K_n = 50\,\mu A/V^2$
$K_p = 17\,\mu A/V^2$.

By equating (1) & (2) & solving for $W_1$;

$$I_{REF} = \frac{K}{2}\frac{W}{L}(V_{gs} - V_{th})^2 \text{ ; i.e, } 10\mu A = \frac{50\mu A/V^2}{2}\cdot\frac{W}{5\mu m}(1.2 - 0.83)^2.$$

or, $W = W_1 = W_2 = \underline{14.61\,\mu m} \simeq 15\,\mu m$.

The requirement for M2 to stay in the saturation region is, "connected $V_{gs0} + V_x$. Bu
$V_{ds2} \geq V_{gs2} - V_{th} = \Delta V = 1.2 - 0.83 = 0.37V$ = excess gate voltage" M3 yields $V_{gs0}$ = in fig.

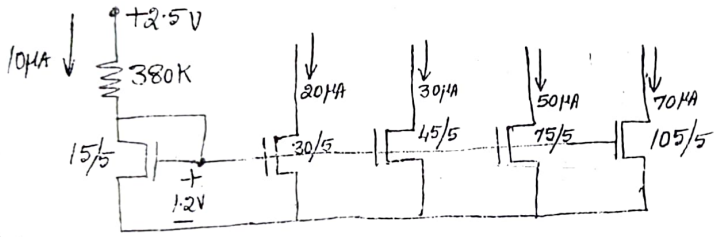
$\therefore$ To keep the transistor M2 in saturation, the drain of M2 should be approximately $V_{D2} \geq -2.5 + 0.37 = \underline{-2.13V}$.

The small signal o/p resistance of the current source is then

$$r_o = \frac{V}{\lambda I_{out}} = \frac{1}{0.06 \times 10\mu A} = \underline{1.67\,M\Omega}$$

Example:-

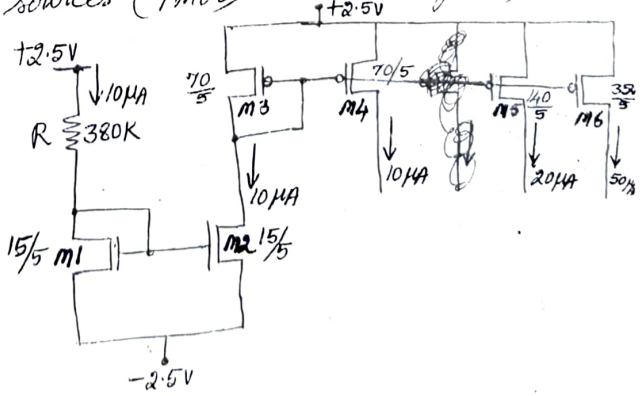
Design four current sinks with values 20, 30, 50 and 70 μA. What is the minimum voltage across each sink? Again assume $V_{DD} = -V_{SS} = 2.5V$.




$\Delta V = 0.37V$ (excess gate voltage) $\quad V_{GS} = \Delta V + V_{th}$

$V_D = -2.5 + 0.37 = \underline{-2.13V}$

Example:- Using the 10 μA NMOS reference current sink of the previous example, design three current sources (PMOS) with values of 10, 20 and 50 μA.




To determine the width of M3, we solve,

$$10\mu A = \frac{17\mu A/V^2}{2} \frac{W_3}{5\mu m} (1.2 - 0.91)^2$$

$\Rightarrow W_3 \simeq 70\,\mu m$.

$\therefore$ The sizes of M4, M5, M6 for supplying 10, 20, 50 μA are 70, 140, and 350 μm resp.

connected device, $M_0$, in series with $M_1$, thereby generating a voltage $= V_{gs0} + V_x$. Proper choice of the dimensions of $M_0$ w.r.t. those of $M_3$ yields $V_{gs0} = V_{gs3}$. Connecting node N to the gate of $M_3$ as shown in fig. ⑥, we have $V_{gs0} + V_x = V_{gs3} + V_y$. Thus, if $(W/L)_3/(W/L)_0 = (W/L)_2/(W/L)_1$, then $V_{gs3} = V_{gs0}$ and $V_x = V_y$. Note that this result holds even if $M_0$ and $M_3$ suffer from "body effect."

If the mismatch effects are neglected, the output current of the cascode current mirror is given by,

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}.$$