FUN 2 Final Project Report

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***Abstract*—The goal of our project was to design a simple circuit which could differentiate high and low frequencies through lighting up an LEDs at predetermined and set thresholds. Real world applications of this include the rise in holiday light shows have led to innovation in RGB lighting syncing with music. While this synchronicity allowed for more complex performances, it typically has a reliance on microchips and amidst a microchip shortage has led to increased prices.**

This project investigates a more affordable alternative to modern lighting rigs that is just as entertaining. We designed this project using analytical, numerical, and experimental techniques. We created the PCB layout using Ultiboard. We then soldered the chosen component parts and confirmed the functionality of the design.

After testing the prototype and reflecting on the design process we have a couple key takeaways. First, modular system design is crucial to simplifying the system and makes analysis and debugging easier. Second, it is important to know when a value can be approximate, like the corner frequencies, and when it must be exact, like the MOSFET parameters. Finally, it is important to have corroborating evidence across all forms of testing (analysis/numerical/experimental) and understand the system to know how to respond if physical components produce different results.

This prototype proves the entertainment value of a minimal LED system. Future designs can utilize the sub-system chaining and add filters to get a more complex response.

I. Background Information and Rationale

We wanted to create our take on blinking holiday lights using our fundamental knowledge of circuit analysis, frequency analysis, and system design. Our project allows LEDs to respond to music, specifically, "Losing it" by Fisher. Songs are made up of a sequence of notes and the higher the pitch of the note, the higher the frequency of the digital signal. We chose this song because of its wide range of frequencies as shown in Fig. 1.

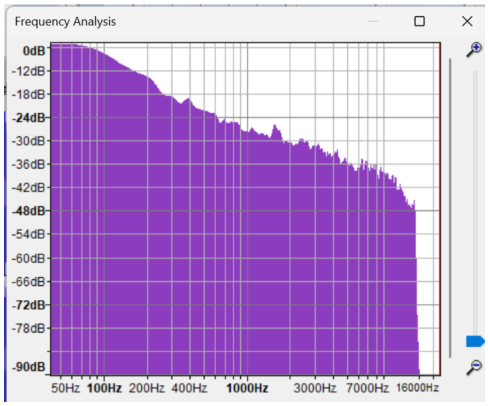

Fig. 1. Frequency Analysis of "Losing it" by Fisher (Chosen bounds are in Bold)

The LEDs respond to the music by lighting up when the frequency of the signal is within certain upper and lower bounds. These bounds were determined through testing and available component parts. What this means is that when you hear a sound with a very low pitch, the red LED should light up, and when you hear a sound with a very high pitch the green LED should light up. We used two LEDs for this project so the system has 4 possible states. The system is made up of 4 modular sub-systems. Each sub-system has a component, either a op-amp or MOSFET, that allows us to analyze the sub-systems independently. By designing the circuit with modular subsystems, analysis and debugging was a lot easier.

The system has two input channels and each channel affects the state of the LEDs. To prevent conflicting states, where one input channel dictates one state of the LED while the other dictates another, the signals were combined and amplified in the first sub-system, the summing amplifier. Next, the signal was filtered through either the high or low pass filter to isolate the extreme frequency content using the corner frequencies in Fig. 1. This signal was then approximately rectified with a peak detector, which controlled the transition rate between states (on and off). The signal then fed into the gate of a common drain amplifier that controlled the current through the LED, allowing it to blink.

II. Design and Analysis

To design this system that separates a song into high and low frequencies and flashes an LED for each, the system was broken down into subsections or blocks. These blocks include: the summing amplifier, the high and low pass sallen key filters, each peak detector, and each mosfet LED driver. The gain of the summing amplifier and the sallen key filters was taken from the requirement of the assignment. The circuit was designed to run off of +4.5 volts and -4.5 volts. A 9 volt battery was used to power the circuit. To split this 9 volt supply into a dual power supply, the TLE2426IP rail splitter IC was used. This creates a virtual ground to be used with the op amps. A BSP170P P-channel mosfet was also used for power management. It was placed in series with the positive voltage from the battery to act as a diode and protect against plugging in the battery backwards.

A. Summing Amplifier

The first section of the circuit is the summing amplifier. It takes the right and left audio channels from the input jacks, passes them through a high pass filter of 20 Hz, adds them together, and amplifies the resulting sum by 3. It also, implements a "T" feedback network with the op amp to increase the input impedance of the circuit. We chose the resistor values of the "T" network to be larger than 10 kΩ to keep the input impedance high. This reduces the loading on the device that is inputting voltage into the summing amplifier. The final schematic can be seen in Fig. 2.

The circuit can be broken into two sections, the passive RC high pass filter associated with each input and the summing amplifier itself. C_3 and R_{18} are associated with the left channel while C_{14} and R_{19} are associated with the right channel. The target cutoff frequency was 20 Hz. Because this is a simple RC filter, the equation for the cutoff frequency is as follows:

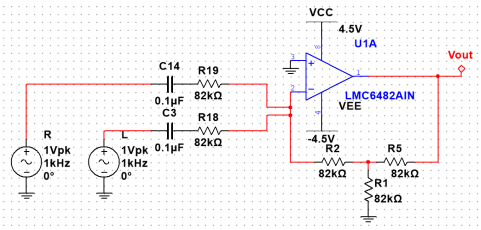

Fig. 2. Schematic for Summing Amplifier

$$f_{cutoff} = \frac{1}{2\pi RC}$$

A 0.1 μF capacitor and a 82 kΩ resistor were chosen, when used with the equation, the cutoff frequency becomes 19.41 Hz which is close enough to the target value of 20 Hz. The filter is the same for each channel so R_{19} and R_{18} are set to 82 kΩ and C_3 and C_{14} are set to 0.1 μF.

The second part of the circuit is the summing amplifier itself. To analyze this in the pass band of the RC filter, the capacitor is treated as a short circuit and one of the inputs is zeroed. This simplified circuit can be seen in Fig. 3.

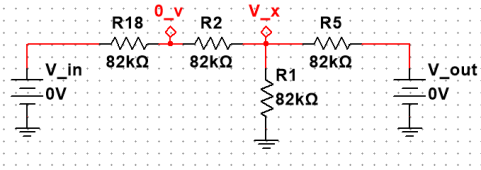

Fig. 3. Simplified Summing Amplifier Schematic for Analysis

The V_0 label is the point where the resistors connect to the inverting input of the op amp. It is labeled as 0 volts because the non-inverting input is connected to ground and the inverting and non-inverting inputs have to be the same. The other rule that is used in this analysis is the fact that no current flows into either op amp input. V_x is just a label used for analysis. I_1-I_4 correspond to the current flowing through resistors R_{18}, R_2, R_1, and R_5 respectively. Using KCL, the following equations are produced:

$$I_2 + I_3 = I_4, I_2 = I_1$$

Using V = IR, the following equations are produced:

$$I_1 = \frac{V_{in}}{R_{18}}, I_2 = \frac{-V_x}{R_2}$$

$$I_3 = \frac{-V_x}{R_1}, I_4 = \frac{V_x - V_{out}}{R_5}$$

Using algebra to manipulate these equations to produce gain results in the following equation:

$$\frac{V_{out}}{V_{in}} = \frac{-(R_2R_1 + R_5R_1 + R_2R_5)}{R_1R_18}$$

Substituting $V_L + V_R$ for V_in and moving V_in, this equations becomes:

$$V_{out} = \frac{-(R_2R_1 + R_5R_1 + R_2R_5)}{R_1R_18}(V_R + V_L)$$

Finally, inserting the chosen resistor values, the equation for the output voltage becomes:

$$V_{out} = -3(V_R + V_L)$$

This is exactly what the design requirements of the circuit specified. The negative gain comes from the fact that the circuit is a negative summing amplifier.

B. High Pass Filter (HPF)

The high pass filter takes the amplified signal from the summing amp, filters out frequencies below our chosen corner frequency and passes the signal to the peak detector. We considered design requirements, cost, and accuracy when building the high pass filter. Based on a frequency analysis of our chosen song in audacity, we wanted the corner frequency of the high pass filter to be 1000 Hz. To minimize costs and increase the attentuation of the filter, we decided to build a Sallen-key high pass filter. This filter allows us to achieve a second-order filter with a higher quality factor (Q > 0.5) without the use of inductors. The part values in Fig. 4 were chosen by a program in Fig. 38 that considered available component values from our kit greater than 10kΩ and prioritized an under-damped system without a peak (0.5 < Q < 0.707) that had the chosen corner frequency.

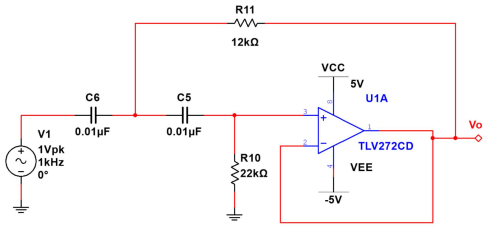

Fig. 4. HPF Schematic

We used a standard unity gain high pass sallen-key filter [1]. So the filter had the following characteristics.

The general form of a second order filter.

$$H(s) = \frac{ks^2}{s^2 + s\frac{w_0}{Q} + w_0^2}$$

K = 1 because there are no feedback resistors allowing the frequency in the passband to have no gain.

$$\lim_{w \to \infty} H(s) = K = 1$$

The output of a DC signal is 0.

$$\lim_{w \to 0} H(s) = \frac{0}{w_0^2} = 0$$

The quality factor equation was used in the code as bounds (0.5 < Q < 0.707), but there was no preference for Q.

$$Q = \frac{\sqrt{R_{10}R_{11}C_{10}C_2}}{R_{11}C_2 + R_{11}C_1 + R_{10}C_2(1-K)} = 0.677$$

The result of the corner frequency equation was compared with the expected corner frequency for accuracy.

$$\omega_0 = \frac{1}{\sqrt{R_{10}R_{11}C_1C_2}} = 979.53Hz$$

These equations allowed us to determine the best values from our part kit shown in Fig. 4.

C. Low Pass Filter (LPF)

We designed the low pass filter with the same priorities of cost, accuracy and functionality as the high pass filter. From looking at the frequency analysis of our song, we selected a corner frequency of 100Hz. A Sallen-Key low pass filter was determined to be the best solution for our design. This filter allows us to maintain a quality factor between 0.5 and 0.707 while filtering out everything above the 100Hz cutoff frequency. A schematic of the low pass filter is shown below in Fig. 5 with part values chosen by a program in Fig. 38.

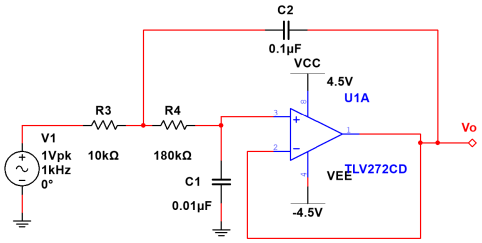

Fig. 5. LPF Schematic

We calculated the quality factor for the low pass filter using its transfer function. The calculations for the quality factor, Q, are shown below.

$$H(s) = \frac{k}{s^2 + s\frac{w_0}{Q} + w_0^2}$$

k equals 1 under the current conditions where there is no resistance in the feedback loop.

$$Q = \frac{\sqrt{R_3R_4C_1C_2}}{R_3(C_1 + C_2) + R_4C_2}$$

$$\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

When plugging in our chosen resistor and capacitor values through the code included in the appendix, we found a Q value of 0.706 and a cutoff frequency of 118.627Hz. This results in a gain of -3.023 dB at the cutoff frequency. While the cutoff frequency is lower than we initially intended, it still would be acceptable for this song which has enough frequencies below 118Hz. The trade-off of this component combination is a higher quality factor which means better filtering of the input signal.

D. Peak Detector

The purpose of the peak detector is to create a near constant voltage at the peak value fed into it. It does this through combining aspects of a super diode and a low pass filter. It achieves a time constant, before taking the next peak input voltage, through adding a capacitor in parallel with the resistor heading to the negative rail. The values of the resistor and capacitor will determine how long the capacitor takes to discharge thus setting the time constant. A capacitor value of 10 μF was used a resistor value of 18 kΩ. These values were determined through experimentation with the LED and our preference for its response time given a range for what the time constant should be. In regards to our conceptual design, this allows the circuit to sample voltages coming in from the high and low pass filters and hold them so the LED drivers can react using a steady gate voltage.

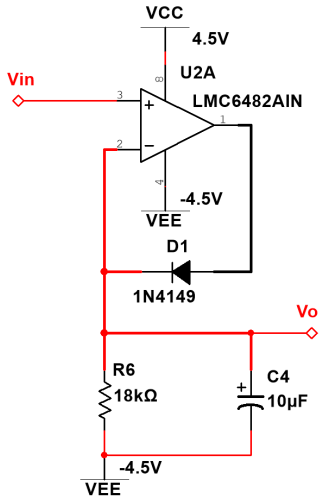

Fig. 6. Peak Detector Schematic

E. LED Driver

The LED Driver takes the output from the high/low pass filters. It is configured as a common drain amplifier as shown in Fig. 7 to isolate the output and input impedance's, it also provides control over the current gain.

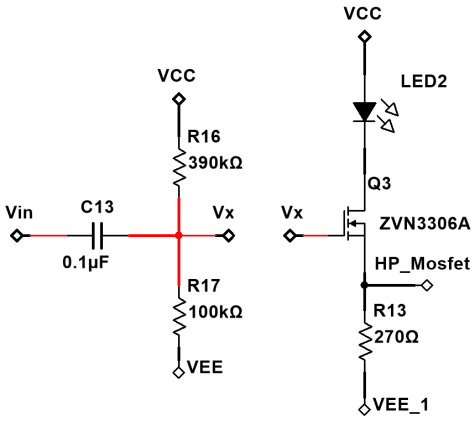

Fig. 7. LED Driver Schematic

From experimental tests of our MOSFETs as shown in Fig. 32, we were able to determine the transconductance parameter, K_N, and the threshold voltage, V_T.

$$V_T = 2.179, K_N = 0.168 \quad Green\,LED$$

$$V_T = 2.126, K_N = 0.153 \quad Red\,LED$$

We wanted the gate voltage to be less than the threshold voltage so we chose resistors accordingly. Without a signal, the gate voltage is determined by a voltage divider. Where Vcc is 9v.

Green LED

$$v_G = \frac{R_{17}}{R_{16} + R_{17}} * v_{cc} < V_T$$

$$\therefore R_{16} = 390k\Omega, R_{17} = 100k\Omega, v_G = 1.837v < V_T$$

RED LED

$$v_G = \frac{R_{15}}{R_{14} + R_{15}} * v_{cc} < V_T$$

$$\therefore R_{14} = 390k\Omega, R_{15} = 82k\Omega, v_G = 1.564v < V_T$$

Since the circuit will switch from saturation to cutoff, We can assume the circuit is in the saturation region when it has an output > 0. The max current for the Green LED is 15mA [2], so we chose our max current to be 10 mA to be safe. The max [3] current for the Red LED is 7mA so we chose 4 mA to be safe. We also know the max input signal is 3v. Using this information, we can solve for the source resistors.

$$I_{DS} = \frac{K_N}{2}(V_{GS} - V_T)^2$$

Green LED

$$I_{DS} = \frac{K_N}{2}(((V_{G,constant} + V_{input}) - I_{DS}R_{13}) - V_T)^2$$

$$R_{13} = 241.29\Omega \approx 270\Omega$$

Red LED

$$I_{DS} = \frac{K_N}{2}(((V_{G,constant} + V_{input}) - I_{DS}R_7) - V_T)^2$$

$$R_7 = 436.47\Omega \approx 680\Omega$$

A higher resistor was chosen for R_7 after testing.

III. Simulations

A. Summing Amplifier

To test and verify the design for the summing amplifier, several simulations were run in Multisim. The first two simulations tested the frequency response of each of the input channels separately. These can be seen in Fig. 8 and Fig. 9. The channel not being used was zeroed. It can be seen from the bode plots that with a near DC input, the output of the system approaches zero.

It can be seen that the approximate cutoff frequency for the right channel is 19.31 Hz and 19.64 Hz. These values are close enough to the analytical values of 19.41 Hz. The point of the corner frequency was found by subtracting 3 dB from the pass band gain:

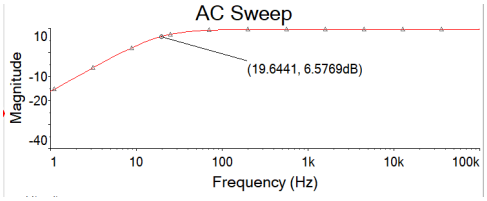

Fig. 8. Bode Plot from 1 Hz to 100 KHz for Left Channel

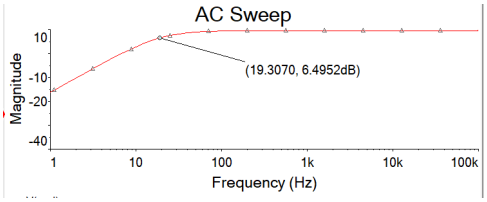

Fig. 9. Bode Plot from 1 Hz to 100 KHz for Right Channel

$$20log(3)dB - 3dB = 6.54dB$$

Tests were run to verify the -3 gain of each channel. The channel not being used was zeroed. These tests can be seen in Fig. 10 and Fig. 11.

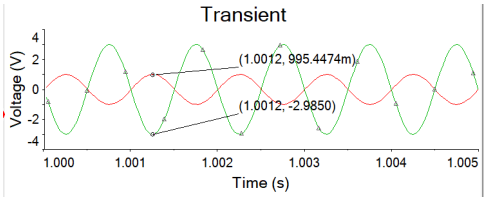

Fig. 10. Transient of Right Channel Input (Red) and Summer Output (Green)

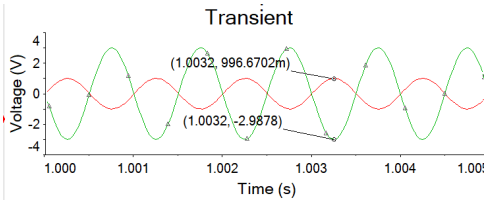

Fig. 11. Transient of Left Channel Input (Red) and Summer Output (Green)

A sine wave input of 1 kHz and amplitude 1 v was input into each of the channels and the output of the summer was observed. It can be seen in both images that the summer inverts both inputs and amplifies them by 3. The cursor is set when the input is equal to 1 volt and it can be seen that the output is -3 volts at this point.

The last test conducted demonstrated the summing amplifier's ability to sum the left and right inputs. Both sine waves had a frequency of 1 KHz. The sine wave on the right channel had an amplitude of 0.5 volts and the sine wave on the left channel had an amplitude of 1 volt. The output of

summer was a sine wave 180 degrees out of phase with an amplitude of 4.5. This is expected as the sum of the inputs is 1.5 and that multiplied by 3 is -4.5. The result of this test can be seen in Fig. 12.

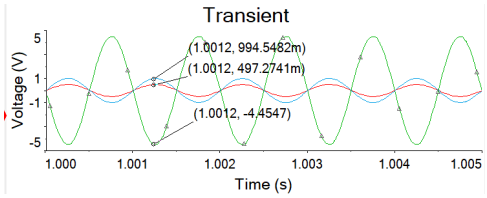

Fig. 12. Transient of Left Channel Input (Blue), Right Channel Input (Red) and Summer Output (Green)

The voltage levels of both inputs and the outputs at a peak in the inputs are labeled in the figures. All of these tests together numerically verify the design requirements of the summing amplifier.

B. High Pass Filter

The design of the high pass sallen-key filter was verified with two multisim simulations a AC sweep, and DC operating point analysis. First, the AC sweep in Fig. 13 verified the corner frequency. Using the equations from the analysis. We know Q = 0.677 and fc = 979.53 Hz so at 20log(Q) = -3.388 dB below the passband, fc is expected. The simulation found a fc of 984 Hz, which is a 0.46% error. Second, the AC sweep verified the passband gain. We know from the equations in the analysis that $K = 1$ and the simulation shows the passband is at 0dB. $H(s) = 10^{\frac{0dB}{20}} = 1$ which confirms our analysis.

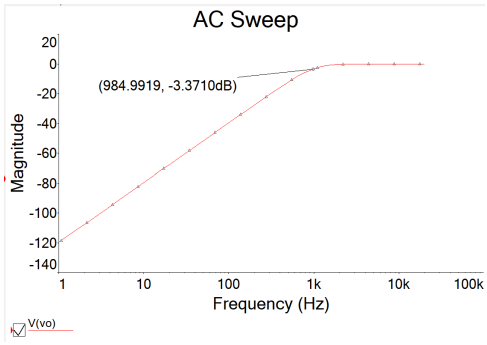

Fig. 13. AC Sweep of HPF from 1 Hz to 20 kHz

From the analysis we also expected the output signal of a DC input to be 0V because of the input capacitor and Fig. 14 confirms this.

	Variable	Operating point value
1	V(vo)	-280.27673 u
2	V(vin)	12.00000

Fig. 14. Operating point analysis with 12V DC Input Signal

C. Low Pass Filter

When simulating with Multisim, we plugged in our resistor and capacitor values and got a corner frequency of about 117.897Hz as shown in Fig. 15 below. This is very close to the calculated cutoff frequency of 118Hz. Similarly, the calculated gains at the cutoff frequency was very similar to what was simulated, the two having a difference of only 0.042 dB.

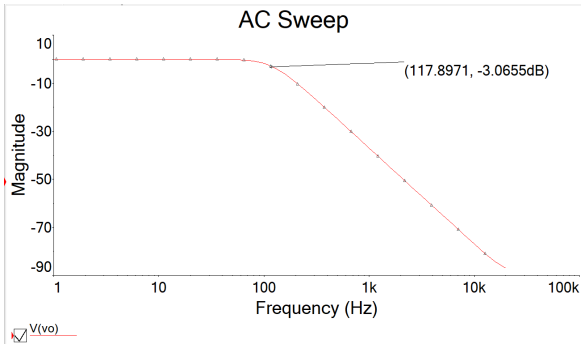

Fig. 15. LPF Bode Plot 1 Hz to 20 kHz AC Sweep

D. Peak Detector

Fig. 16 shows that even with an input signal near the lowest frequency extreme, the peak detector provides a good approximate rectification of the input signal. An increased frequency may have a better approximation for the peak detector's response using our song when simulating. The difference between the peak detector's max and min output was 0.69V. While this may seem high, it had negligible effect on the LED response when testing.

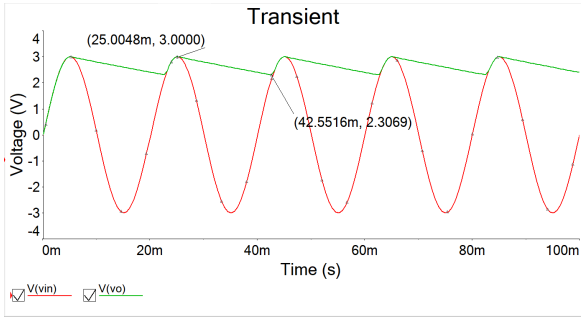

Fig. 16. Transient with 3v 50 Hz input

E. LED Driver

The following measurements used Fig. 7 with varying inputs. The MOSFET was not simulated, only tested in Fig. 32 because the parametes are so component dependent.

With no input, the gate voltage (Vx) is lower than V_T, putting the MOSFET in the cutoff region, which makes sense because the current across the LED is about 0A.

The max voltage at the gate (Vx) will be the DC offset from Fig. 17 + a max input signal of 3V. Fig. 18 shows that the LED stays within the safe max current range of 10mA.

	Variable	Operating point value
1	-I(LED2:K) | I(I_LED)	7.21940 u
2	V(vx)	1.83673

Fig. 17. Steady State Measurements

	Variable	Operating point value
1	-I(LED2:K) | I(I_LED)	9.63526 m
2	V(vx)	4.83600

Fig. 18. Max Input Signal Measurements

F. System Simulations

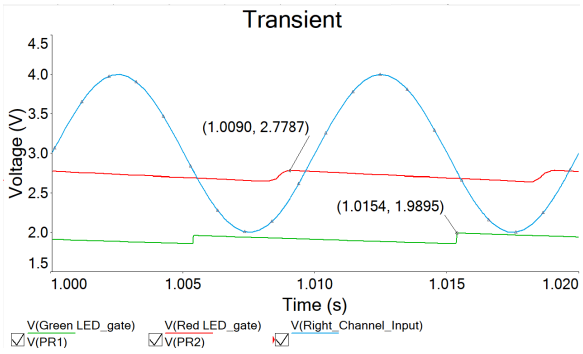

Fig. 19. Right Channel 1V 100Hz Input Signal with 3v offset with VCC from 0 to 9V

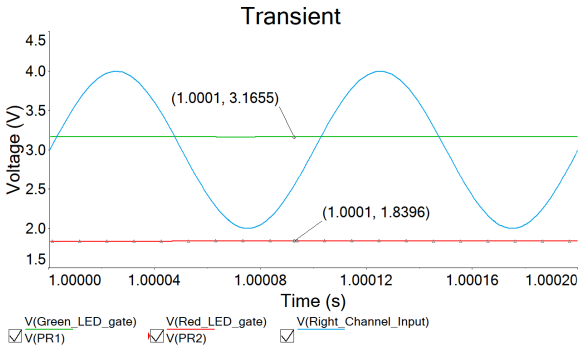

Fig. 20. Right Channel 1V 10kHz Input Signal with 3v offset with VCC from 0 to 9V

Fig. 19 Shows that the LED with the high pass filter (Green LED) has a gate voltage that is kept below its threshold of 2.179 V and the RED LED has its gate voltage above its MOSFETs threshold of 2.126V, allowing it to light. The offset can be seen to be filtered out. The opposite is shown in Fig. 20.

IV. Experimental Results

In this section, the different Sections of the PCB board were tested to confirm their function. For all of the tests, the positive supply of the AD2 was set to 4.5 volts and the negative supply was set to -4.5 volts unless otherwise specified. The ground of the AD2 was connected to the ground of the PCB, the positive supply was connected to VCC and the negative supply was connected to VEE.

A. Summing Amplifier Experimental Results

The experimental tests for the summing amplifier were exactly the same as the tests in Section III-A. The first two tests tested the frequency response of the left and right inputs separately. Wave Gen 1 of the AD2 was connected to the left or right input with the other one connected to ground and the output was connected to the 1+ scope of the AD2. The results can be seen in Fig. 21 and Fig. 22.

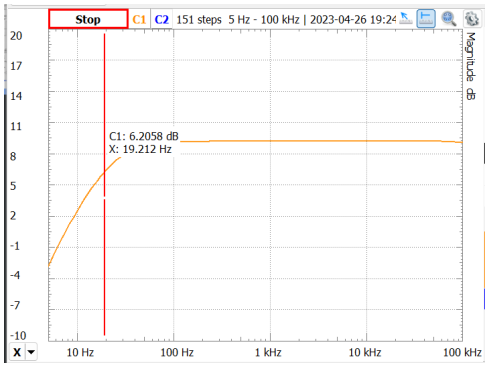

Fig. 21. Bode Plot of the Right Channel Input to the Summing Amplifier (Left Channel Zeroed

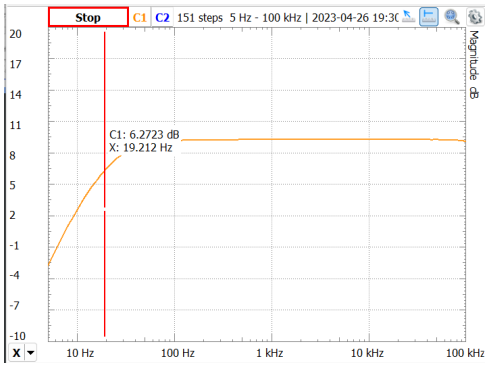

Fig. 22. Bode Plot of the Left Channel Input to the Summing Amplifier (Right Channel Zeroed

Fig. 21 shows the right channel input bode plot. Since the gain of the amplifier is 3 in the pass band, the decibel gain should be around 9.54 dB. It was measured to be 9.205 dB. Using the measured pass band gain, the -3 dB point should be around 6.205 dB. Using this value, the break frequency was measured to be 19.212 Hz which is acceptably close to the expected value of 19.41 Hz. Fig. 22 shows the left channel input bode plot. Since the gain of the amplifier is

3 in the pass band, the decibel gain should be around 9.54 dB. It was measured to be 9.255 dB. Using the measured pass band gain, the -3 dB point should be around 6.255 dB. Using this value, the break frequency was measured to be 19.212 Hz which is acceptably close to the expected value of 19.41 Hz.

The next two tests tested for the gain of each channel of the summing amplifier independently in the pass band. Wave Gen 1 and 1+ scope of the AD2 were connected to the right or left input with the other input being grounded. The results of the tests can be seen in Fig. 23 and Fig. 24.

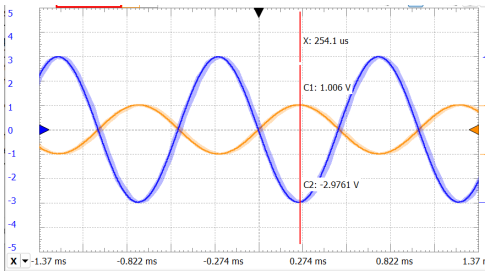

Fig. 23. Time Plot Showing the Right Input (Orange) and the Output (Blue) of the Summing Amplifier with a Sine Wave of 1 kHz an Amplitude of 1 Volt.

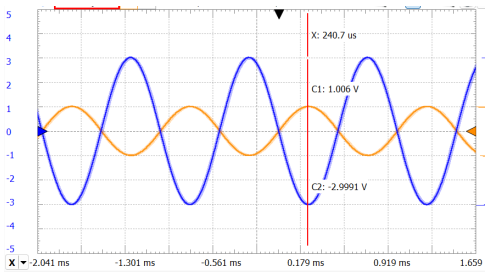

Fig. 24. Time Plot Showing the Left Input (Orange) and the Output (Blue) of the Summing Amplifier with a Sine Wave of 1 kHz an Amplitude of 1 Volt.

In both tests, the input was a sine wave of 1 kHz and amplitude of 1 volt. In both of the of the tests, a peak of the input is labeled with the voltage of the input and the output. In both tests, when the input was 1 volt, the output was -3 volts. This verifies that the gain of the amplifier was -3.

The next test involved inputting an identical sine wave to the left and right channels to observe the summing property of the summing amplifier. Wave Gen 1 was connected to the right input, Wave Gen 2 was connected to the left input and the 1+ scope pin, and the output of was connected to the 2+ scope pin. This test can be seen in Fig. 25.

In the figure, the voltage at a peak in the input is labeled as well as the voltage of the output. If both inputs are 500 mV volt, the output voltage should be -3 volts because $-3(500mV + 500mV) = -3volts$. This test verifies the summing property of the amplifier.

The last test involved inputting the audio signal into the summing amplifier and probing the output. The audio cable was plugged into the computer and the PCB and the out of

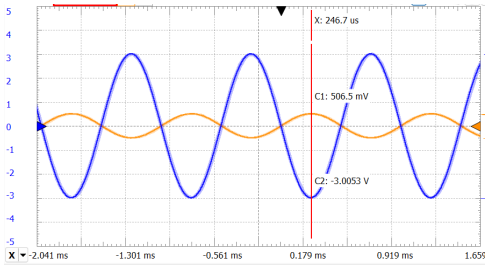

Fig. 25. Time Plot Showing the Left Input (Orange) and the Output (Blue) of the Summing Amplifier with a Sine Wave of 1 kHz and Amplitude of 500 mV Volt on Both Inputs

the summing amplifier was connected to the 1+ scope pin of the AD2. The results can be seen in Fig. 26.

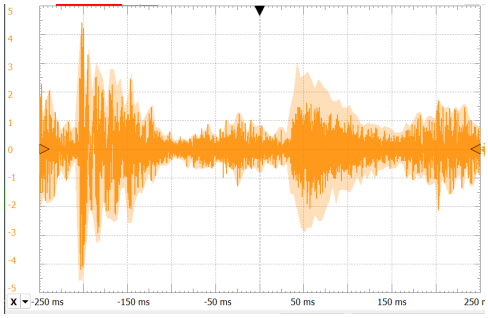

Fig. 26. Time Plot Showing the Output of the Summing Amplifier with the Song as an the Input to the Left and Right Channel

B. High Pass Filter Experimental Results

We can confirm the corner frequency, DC operating point, and passband gain from Fig. 27. First, The plot shows that there will be enough attenuation to produce an output of 0V at 0Hz. Second, at $20log(Q) = 3.388dB$, the corner frequency is 1.08 kHz. This is a 10.2% error from the expected vale of 979.53 Hz, but accurate enough because the corner frequency was chosen and doesn't have to be exact. Lastly, The passband gain can be seen to be 0dB which corresponds to a gain k = 1 as we expected.

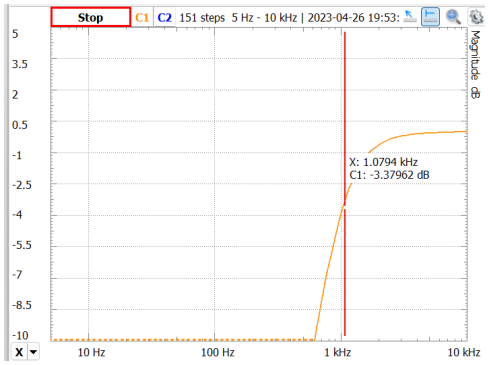

Fig. 27. Bode Plot AC Sweep 5 Hz - 10kHz

C. Low Pass Filter Experimental Results

We can confirm the corner frequency, DC operating point, and passband gain from Fig. 28. First, The plot shows that there will be enough attenuation to produce an output of 0V as the frequency approaches ∞. Second, at $20log(Q) = -3.023dB$, the corner frequency is 119.57 Hz. This is a 10.2% error from the expected value of 118.627Hz, but accurate enough because the corner frequency was chosen and doesn't have to be exact. Lastly, The passband gain can be seen to be 0dB which corresponds to a gain k = 1 as we expected.

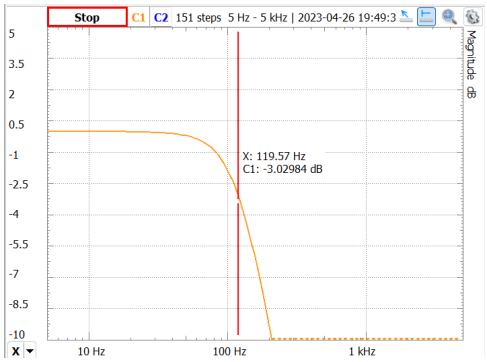

Fig. 28. Bode Plot AC Sweep 5 Hz - 5kHz

D. Peak Detector Experimental Results

Due to the placement of the test points on the pcb, the input biasing resistor and capacitor network was tested with the peak detectors for the high and low side. To test the biasing resistors and the peak detector, the left and right inputs were grounded, the output of the summing amp was connected to the inputs of the filters, the output of the filters to the peak detectors were open, the input to both mosfet stages were connected to V_{EE}, and the input of the peak detector not is use was grounded. The input of the peak detector being tested was connected to wavegen 1 on the AD2 as well as the 1+ scope pin. The output of the peak detector was connected to the 2+ scope pin.

For each peak detector circuit, a 75 Hz sine wave with an amplitude of 1 volt was used an in input and the output of the peak detector was observed. The peak detector associated with the high frequency side was tested first. The sine wave described above and the output of the peak detector can be seen in Fig. 29. The signal enters the resistor biasing network consisting of C_{13}, R_{17}, and R_{16} sets the average value of the sine wave to -2.66 volts. The peak detector then holds the maximum value of this shifted signal. It can be seen in Fig. 29 that the peak voltage of the output is -1.899 volts. The amplitude of the output is then $-1.899v - (-2.66v) = 0.77v$. This value is acceptable because the capacitor in the peak detector cannot charge fast enough to reach all the way to 1 volt.

The peak detector associated with the low frequency side was tested second. The sine wave described above and the output of the peak detector can be seen in Fig. 30. The signal enters the resistor biasing network consisting of C_{12}, R_{15}, and R_{14} sets the average value of the sine wave to -2.94 volts. The peak detector then holds the maximum value of this shifted signal. It can be seen in Fig. 29 that the peak voltage of the output is -1.899 volts. The amplitude of the output is then $-2.196v - (-2.94v) = 0.74v$. This value is acceptable because the capacitor in the peak detector cannot charge fast enough to reach all the way to 1 volt.

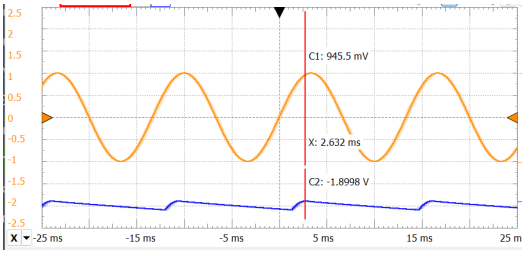

Fig. 29. High Side Peak Detector Input (Orange) and output (Blue) with a 75 Hz Sine Wave with Amplitude of 1 Volt as the Input

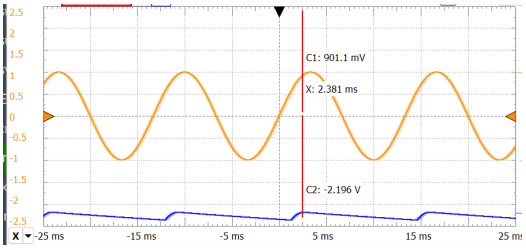

Fig. 30. Low Side Peak Detector Input (Orange) and output (Blue) with a 75 Hz Sine Wave with Amplitude of 1 Volt as the Input

E. LED Driver Experimental Results

The MOSFETs was characterized with the circuit in Fig. 31. Two points in the saturation region were chosen from Fig. 32 and a system of equations was solved to determine the MOSFET parameters Kn and Vt.

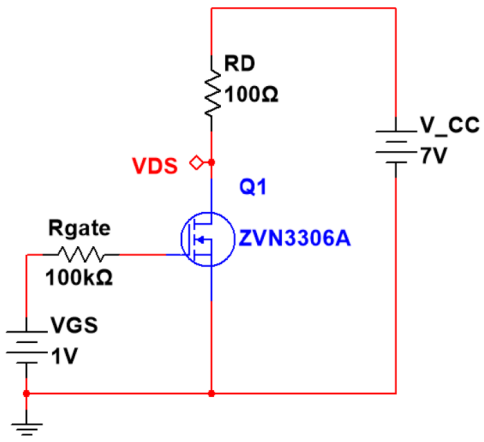

Fig. 31. MOSFET Characterization Schematic

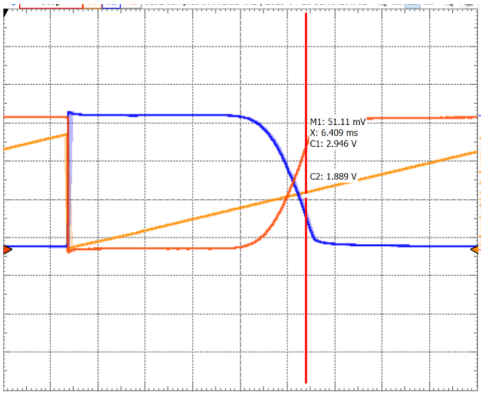

Fig. 32. VGS Sweep of MOSFET with 3V amplitude 1V offset ramp-up signal from Fig. 31

Due to the location of the test points, the mosfet circuit test here only consists of testing the mosfet, LED, and source resistor. In the following tests. The right and left inputs were grounded and the gates of the mosfets were connected to different voltages. The voltage across the source resistor was measured relative to V_{EE}. The following equation will be used when testing the mosfets with the maximum input level because it is assumed they are in the saturation region.

$$I_{DS} = \frac{K_n}{2}(V_{GS} - V_T)^2$$

The mosfet controlling the green LED (high frequnecy indicator) was tested first. Because the resistors R_{16} and R_{17} set the gate voltage of the mosfet at 1.837 volts (relative to V_{EE}) when there is no input, the gate of the mosfet was set to this voltage to test the case when no input is applied. The voltage across the source resistor was measured with this input. The values can be seen in Fig. 33. The voltage across the resistor is practically 0 which indicates that there is no current flowing through it and the LED is off.

	Channel 1	Channel 2
DC	1.849 V	12 mV
True RMS	1.849 Ṽ	12 mṼ
AC RMS	1 mṼ	2 mṼ

Fig. 33. Gate Voltage (Channel 1) and Voltage Across Source Resistor (Channel 2) of the Mosfet Controlling the High Frequency LED

To test the maximum possible input, the maximum amplitude of the signal coming from the peak detector was added to the voltage of the gate with no input, for the high frequency mosfet, the gate voltage becomes 4.8367 volts relative to V_{EE}. The voltage of the source was measured, this can be seen in Fig. 34. The voltage on the source resistor is 2.363 volts. Using the fact that the source resistor on the high frequency LED mosfet driver is 270 Ω and $V = IR$, it can be determined that the current flowing through the LED is 8.75 mA. This value indicates that the LED is on and it is also less than the target maximum current of 10 mA. The K_n and V_T values for this mosfet are 0.168 A/V^2 and 2.179 volts respectively. Calculating I_{DS} with the saturation equation yields an I_{DS} of 8.17 mA, which is close to the measured value.

$$I_{DS} = \frac{0.168}{2}((4.854v - 2.363v) - 2.179v) = 8.17mA$$

	Channel 1	Channel 2
DC	4.854 V	2.363 V
True RMS	4.854 Ṽ	2.363 Ṽ
AC RMS	2 mṼ	2 mṼ

Fig. 34. Gate Voltage (Channel 1) and Voltage Across Source Resistor (Channel 2) of the Mosfet Controlling the High Frequency LED

The mosfet controlling the red LED (low frequnecy indicator) was tested second. Because the resistors R_{14} and R_{15} set the gate voltage of the mosfet at 1.563 volts (relative to V_{EE}) when there is no input, the gate of the mosfet was set to this voltage to test the case when no input is applied. The voltage across the source resistor was measured with this input. The values can be seen in Fig. 35. The voltage across the resistor is practically 0 which indicates that there is no current flowing through it and the LED is off.

	Channel 1	Channel 2
DC	1.56 V	12 mV
True RMS	1.56 Ṽ	12 mṼ
AC RMS	2 mṼ	2 mṼ

Fig. 35. Gate Voltage (Channel 1) and Voltage Across Source Resistor (Channel 2) of the Mosfet Controlling the Low Frequency LED

To test the maximum possible input, the maximum amplitude of the signal coming from the peak detector was added to the voltage of the gate with no input, for the low frequency mosfet, the gate voltage becomes 4.563 volts relative to V_{EE}. The voltage of the source was measured, this can be seen in Fig. 36. The voltage on the source resistor is 2.255 volts. Using the fact that the source resistor on the high frequency LED mosfet driver is 680 Ω and $V = IR$, it can be determined that the current flowing through the LED is 3.32 mA. This value indicates that the LED is on and it is also less than the target maximum current of 4 mA. The K_n and V_T values for this mosfet are 0.153 A/V^2 and 2.126 volts respectively. Calculating I_{DS} with the saturation equation yields an I_{DS} of 14.9 mA. This value is far from what was measured. One of the possible reasons is the fact that the threshold voltage measurement was known to be off.

$$I_{DS} = \frac{0.153}{2}((4.576v - 2.255v) - 2.126v) = 14.9mA$$

	Channel 1	Channel 2
DC	4.576 V	2.255 V
True RMS	4.576 Ṽ	2.255 Ṽ
AC RMS	1 mṼ	1 mṼ

Fig. 36. Gate Voltage (Channel 1) and Voltage Across Source Resistor (Channel 2) of the Mosfet Controlling the Low Frequency LED

F. System Level Experimental Results

To test the pcb on a system wide level, the chosen song was used an input and the voltage at the output of either peak detector was measured. This test was performed with the battery as the power source and the rail-splitter IC inserted. The result can be seen in Fig. 37.

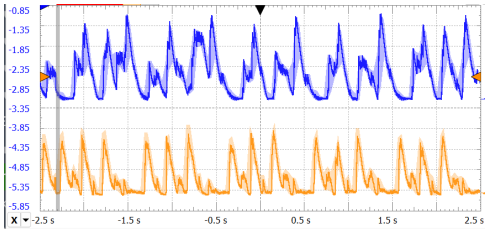

Fig. 37. Voltages of the Gates of the Driver Mosfets With the Song playing (High frequency Peaks in Orange and Low Frequency Peaks in Blue)

It can be seen that the amplitude of both signals is under 3 volts and that the signals are independent. There are portions where the high frequency output is on and the low frequency is off and vise versa.

V. Challenges and Workarounds

The PCB and circuit design process rendered a few issues that were addressed and resolved. They are listed and described below:

1) The summing amplifier, low pass and high pass filters were not outputting correctly. The voltage output should have been centered at ground but it was centered at the negative rail of the supply (V_{EE}). This was solved by inspecting the board and finding a resistor that had not been soldered in well. The solder on the end of the resistor lead made it appear to have a good connection when in reality it did not. Soldering the resistor back in solved the problem.
2) The red LED was dimly lit even if there was no input signal. The threshold voltage for the mosfet driving the LED was measured to be 2.125 volts. The voltage divider in the mosfet driver stage was designed to give it 2 volts when there was no input. Because the LED was lit with no input, this meant the measurement of the threshold voltage was wrong. The bottom resistor in the voltage divider was decreased from 100 kΩ to 82 kΩ. This lowered the gate voltage and the LED was no longer dimly lit with no input signal.
3) To characterize the Mosfet, we created a transient analysis of Fig. 31 and took a measurement approximately at the transition between the cutoff and saturation regions. We thought this was a good approach to finding the Mosfet parameters because at this point, $V_{DS} = V_{GS} - V_T$. However, because it is difficult to tell exactly where this transition point was, our values didn't make sense (ie. too extreme). Instead, we took two measurements in the saturation region of I_{DS}, V_{DS} then solved for K_N, V_T with a system of equations. These parameters were much more accurate.

VI. Conclusions and Thoughts for Future Classes

This project was an in-depth synthesis of the topics we covered throughout the semester. We utilized our understanding of fundamental circuit laws, frequency analysis, component properties, and common circuit designs to create a successful prototype of a spectrum analyzer. This process took us through all the phases of the creation process. We designed the circuit and proved the design worked analytically and numerically. This reinforced our understanding of well-studied architectures like the high-pass sallen-key filter and common drain amplifier. We then designed the system in Ultiboard. This allowed us to gain real-world PCB design experience and we gained a better understanding of the importance of component layout, especially the power lines. Next, we built the sub-systems on a breadboard and soldered them into the PCB debugging the PCB along the way. Throughout this project we gained important trouble shooting skills and experience with industry tools.

In the future, we would love to see a greater variety of PCB designs, with an increased freedom of expression for how the LEDs respond to the song. Utilizing the same relative design, students could instead choose among a variety of filters including HPF, LPF, band-pass filters, and band-reject filters all filters that we have covered this semester. This would lead to more interesting LED responses.

Our advice to future students is to try to understand the purpose behind each sub-system. We thought the most difficult parts were the ones that had no one right answer. Thus, understanding each subsystem's function makes designing, especially choosing arbitrary component values, a lot easier. We also thought it is important to understand how the system was designed as a whole. As we attempt to build future and possibly more complicated systems, you should think about what made this project easier to tackle and or more difficult.

We leave future students with a couple questions to consider. Why did we choose a modular design? What subsystems should have been integrated into the project first and why? What values matter to the design and how important is their accuracy?

VII. Collaboration Statement

Gabriel:

- I (Background)
- II.B (HPF Analysis)
- II.E (LED Driver)
- III.B (HPF Simulation)
- III.E (LED Driver Simulation)
- III.F (System Simulations)
- IV.B (HPF Experimental) - Written portion
- IV.E (LED Driver Experimental) - Mosfet Characterization.
- V (Challenges and Workarounds) - 1 point
- References/Appendix Citations

Wolfgang:

- II.A (Summing Amplifier Analysis)

- III.A (Summing Amplifier Simulation)
- IV.A (Summing Amplifier Experimental Verification)
- IV.B (HPF Experimental Verification) - Experiment, figures
- IV.B (LPF Experimental Verification) - Experiment, figures
- IV.D (Peak Detector Experimental Verification)
- IV.E (Mosfet Driver Experimental Verification)
- IV.F (System Level Experimental Verification)
- VI (Conclusion)
- V (Challenges and Workarounds) - 2 points

Taylor

- Abstract
- II.C (LPF Analysis)
- II.D (Peak Detector)
- III.C (LPF Simulation)
- III.D Peak Detector Simulation)
- IV.C (LPF Experimental) - Written portion
- References/Appendix Citations

References

[1] J. Karki, *Analysis of the sallen-key architecture*, SLOA024B, Texas Instruments, 1999. [Online]. Available: https://collab.its.virginia.edu/access/content/group/337e7dd2-a7dc-4e13-ae85-9875b4a92fa3/M4%5C%20Laplace/Sallen-Key.pdf.

[2] *High efficiency led in ϕ 3 mm tinted diffused package*, 83006, Vishay, 2022. [Online]. Available: https://www.vishay.com/docs/83006/tlhg440.pdf.

[3] *T-1¾ (5 mm), t-1 (3 mm), low current led lamps*, AV02-1557EN, Broadcom, 2021. [Online]. Available: https://media.digikey.com/pdf/Data%20Sheets/Avago%20PDFs/HLMP-47zz,HLMP-17zz_2021-08-09.pdf.

Appendix

```
//Traverse through all combinations
for(int i = 0; i < R_vals.length; i++){
    for(int j = 0; j < R_vals.length; j++) {
        for(int k = 0; k < C_vals.length; k++) {
            for(int l = 0; l < C_vals.length; l++) {
                Q = calculateLPFQ(R_vals[i], R_vals[j], C_vals[k],  C_vals[l]);
                Q = calculateHPFQ(R_vals[i], R_vals[j], C_vals[k],  C_vals[l]);

                //Check if Q in range
                if(Q > 0.5 && Q < 0.707) {
                    W = calculateW(R_vals[i], R_vals[j], C_vals[k], C_vals[l]);
                    W_err = calculateWErr(W);
                    //Check if better combination than current combination
                    if(W_err < currentErr){
                        currentErr = W_err;
                        R1 = R_vals[i];
                        R2 = R_vals[j];
                        C1 = C_vals[k];
                        C2 = C_vals[l];
                        chosenQ = Q;
                        chosenW = W;
                    }
                }
            }
        }
    }
}
static double calculateLPFQ(double r1, double r2, double c1, double c2){
    return Math.sqrt(r1*r2*c1*c2) / (r1*c1 + r2*c1);
}
static double calculateHPFQ(double r1, double r2, double c1, double c2) {
    return Math.sqrt(r1*r2*c1*c2) / (r2*c2 + r2*c1);
}
static double calculateW(double r1, double r2, double c1, double c2){
    return (1.0 / Math.sqrt(r1*r2*c1*c2));
}
static double calculateWErr(double val) {
    double num = Math.abs(theoretical_val - val);
    return ((num / theoretical_val) * 100);
}
```

Fig. 38. Code to find HPF/LPF Resistor and Capacitor Component Values