Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2021

Subject Code:3130704 Date:06/10/2021

Subject Name:Digital Fundamentals

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Solve the following Boolean functions by using K-Map. Implement the simplified function by using logic gates $F = (w,x,y,z) = \Sigma (0,1,4,5,6,8,9,10,12,14) + d(2,15)$	**03**
	(b)	Do as directed a. Convert 378.93_{10} to octal b. Add 27.5_8 and 74.4_8 c. Convert $5C7_{16}$ to decimal d. Multiply 1101_2 by 110_2	**04**
	(c)	With a neat block diagram explain the function of decoder. Design BCD to seven segment decoder	**07**
Q.2	**(a)**	Solve below function using 4 * 1 multiplexer $F(w,x,y) = \sum(1,2,4,7)$	**03**
	(b)	Compare CMOS and TTL Logic Family	**04**
	(c)	Design full adder and subtractor using mode control	**07**
		OR	
	(c)	Obtain the minimal expression for $f=\sum m(1,2,3,5,6,7,8,9,12,13,15)$ using the tabular method(Q McCluskey)	**07**
Q.3	**(a)**	Explain D flip flop with proper diagram	**03**
	(b)	Explain 4 bit Ring counter. What is the limitation in Ring counter?	**04**
	(c)	Design the Synchronous Mod – 6 counter using JK flip flop	**07**
		OR	
Q.3	**(a)**	Explain T flip flop with proper diagram	**03**
	(b)	Design 2 bit Ripple counter using –ve edge triggered JK flip flop	**04**
	(c)	Design 3 bit down Synchronous counter using T flip flop	**07**
Q.4	**(a)**	Explain below terms for DAC: a. Resolution b. Settling time	**03**
	(b)	Draw the logic diagram of Parallel in serial out shift register	**04**
	(c)	Draw and Explain R-2R ladder type DAC	**07**
		OR	
Q.4	**(a)**	Explain two input TTL Nand Gate	**03**
	(b)	Draw and Explain the successive approximation type ADC	**04**
	(c)	Draw and Explain 4 bit Universal Shift Register	**07**

Q.5	**(a)**	Explain below memory types a. MROM b. EEPROM	**03**
	(b)	Draw internal logic of a 32*8 ROM	**04**
	(c)	Draw PAL design to implement F1= a'bc+ab'c+ac' and F2=a'b'c'+bc	**07**

OR

Q.5	**(a)**	What are the advantages of PLD over the fixed function ICs	**03**
	(b)	Draw a structure of an unprogrammed PLA circuit	**04**
	(c)	Implement the following two Boolean functions with a PLA a. F1(A,B,C)=∑m(0,1,4) b. F2(A,B,C)=∑m(0,5,6,7)	**07**

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