# EE270 Assignment: Design Project

## 1: Overview

This assignment is composed of a practical part, requiring VHDL design and implementation on a Basys3 FPGA board, and an investigative part. It is to be undertaken in groups, with all group members being expected to contribute to all aspects of the assignment (i.e. investigation, practical work, report writing and demonstration).

The ***group marks*** for this assignment are split as follows:

- **20%** for the technical investigation,
- **70%** for a the practical work (15% for a demonstration in the lab, and 55% for a technical report, to include commented code and test results),
- **10%** for management of the project, including planning and teamwork, as evidenced by the general conduct of the project, attendance at lab sessions, report and demonstration.

Further details of these aspects are presented in the following sections.

## 2: Technical Investigation: Semiconductor Industry

The investigative aspect of the assignment will require you to find out about a particular semiconductor company, the products that they make, and the markets that they serve. The company that you should research depends on your group number, as given in the following table:

| Group Number | Company | Company Website |
|---|---|---|
| 1 - 5 | Broadcom | http://www.broadcom.com |
| 6 - 10 | Xilinx | http://www.xilinx.com |
| 11 - 15 | TSMC | http://www.tsmc.com |
| 16 - 20 | Qualcomm | http://www.qualcomm.com |
| 21 - 25 | ARM | http://www.arm.com |
| 26 - 30 | NXP | http://www.nxp.com |
| 31 - 35 | Infineon | http://www.infineon.com |
| 36 - 40 | Intel | http://www.intel.com |
| 41 - 45 | Analog Devices | http://www.analog.com |
| 46 - 50 | Cirrus Logic | http://www.cirrus.com |
| 51 - 55 | Global Foundries | http://www.globalfoundries.com |
| 56 - 60 | Texas Instruments | http://www.ti.com |
| 61 - 66 | Dialog Semiconductor | http://www.dialog-semiconductor.com |

For this part of the assignment, you should write a technical review essay (suggested length: in the region of 1500 words). The essay should be included in the same overall document as the technical report, but

should be self-contained, e.g. with its own list of references (you should try to expand your reading beyond the company website!).

The following questions are provided as a starting point for thinking about your investigation, but please feel free (indeed you are encouraged) to lead your own research and come up with your own points to address.

- What does this company do? What is its business model (how do they make money)?
- What sort of products does the company make? (If it has a very broad portfolio, you can summarise into general areas if you wish).
- What are its main target markets and end-user application areas?
- Can you pick out one particular product that interests you, and discuss it in more detail?
- Is this a 'fabless' semiconductor company, or does it have its own manufacturing facilities?
- Where is the company located? How is it structured, and how many employees does it have?
- What sort of work could you do, if you were to join this company in an engineering role?
- How does this company fit into the semiconductor industry?

In writing this essay, you are likely to come across a variety of terms and concepts that are new to you. It is important that you take the time to investigate what these new things mean, such that you understand well enough to write about them in your own words.

In terms of structure, the essay should have a clear title and an abstract. It should also include page numbers, section titles (where appropriate), a conclusion, and a list of references. Note that any images that are not originally created for the report, e.g. derived from websites or articles, must be referenced.

Please take care to present references in the standard style for engineering reports. The following IEEE citation reference document can be consulted for guidance:

http://www.ieee.org/documents/ieeecitationref.pdf

## 3: Design Tasks

Each group will be tasked with fulfilling a particular design brief, using VHDL and targeting the **Basys 3** board. The task that you should attempt depends on your group number.

All of the design tasks involve some aspect of timing. Remember that the clock source on the board has a frequency of 100MHz, and therefore one second is equivalent to 100,000,000 clock cycles!

**Practical 9** is provided as an example that provides key preparation for tackling the design tasks. Please work through it as part of your efforts on the project.

Tackling your assigned problem will require you to consult the technical documentation provided by the board manufacturer, Digilent, and to develop your own code to solve the problem. A good place to start researching the capabilities of the board is the Basys 3 reference page:

https://reference.digilentinc.com/basys3:refmanual

You can incorporate code from reference designs (either from Digilent or provided during the class), but you MUST make sure to clearly identify code that has not been developed by the group as part of the assignment (failure to do so may be interpreted as academic dishonesty — see the later section on this topic).

If you are concerned about being able to complete the whole design, it is suggested that you select a part of the problem to concentrate on first, and then try to build up from there. Bear in mind that, as a group assignment, it will be important to manage tasks (and time!) by progressing some aspects in parallel. You should address planning and group working in the technical report, as part of the 10% for project management.

### *3.1: Task A: Activity Timer (Groups x0 and x1)*

This task requires you to count the number of seconds since the last detected activity on the slide switches on the board (SW0 to SW15). The 7-segment display should be used to display the time in seconds since the last activity, and the number of previous detected events, as indicated in the table below.

| **Left Digit** | **Middle Left Digit** | **Middle Right Digit** | **Right Digit** |
|---|---|---|---|
| Number of previous event detections | | Seconds since last event | |

The system should include reset inputs for both the timer, and the event counter.

### *3.2: Task B: Energy Efficient Lighting (Groups x2 and x3)*

You are required to design an energy efficient lighting system that automatically controls the lights in the corridor of a hotel, based on the detection of people present. There are 16 lights along the corridor, between opposite pairs of bedroom doors. There is also an infra-red detector in each section of the corridor to detect the presence of humans.

- If there is activity in a particular section of the corridor, the light for that section should be switched on. The lights in directly adjacent sections should also be switched on.
- The light in each section should be switched off after 10 seconds of inactivity.

You should use the slide switches and LEDs to demonstrate the system.

### *3.3: Task C: Egg Timer (Groups x4 and x5)*

Design a controller that will allow you to count down to zero (in seconds), to time the cooking of a boiled egg. The number of seconds should be displayed on the 7-segment display. Once the counter reaches zero, the LEDs should illuminate.

You can use the slide switches and/or buttons to control the timer. There should be at least two settings, for soft-boiled and hard-boiled.

For more egg-boiling info... ! http://www.bbc.co.uk/programmes/p017tm3q

### *3.4: Task D: Number Guessing Game (Groups x6 and x7)*

The scenario for this task is that there are two players. The first player specifies a number (in binary) using the rightmost 8 slide switches from the group of 16. These 8 slide switches are then covered and the other 8 are available for the second player.

The second player guesses the number entered by the first, by altering the positions of their slide switches and then pressing a button to enter their choice. If their guess is lower than the set number, the 7-segment display should display a message to represent “up”; or if it is higher, the 7-segment display should show “dn” (to represent ‘down’). If and when the correct number is guessed, the LEDs should illuminate.

### *3.5: Task E: Flow Monitor (Groups x8 and x9)*

This task involves simulating the flow of water through a pipe. The slide switches will be used to specify a rate and direction of flow, and the LEDs should illuminate in a pattern that reflects this. The rate of flow can vary from $0ms^{-1}$, to $5ms^{-1}$, in either direction.

If the rate is set to exceeds $5ms^{-1}$, a lock mechanism will be used to shut the system down (you can use the 7-segment display to show if this occurs).

# 4: Requirements and Marking

This assignment is worth 15% of the total mark for the module and will be completed over Weeks 8 - 11.

Lab sessions from weeks 8 - 11 will be dedicated to the project. You should also be prepared to spend extra effort outside of class time to complete the assignment. Note that the investigation / essay is independent of practical work, and can be started at any time.

The Basys 3 FPGA boards will be made available on a loan basis during the assignment period, starting from Week 9. You can borrow a board from the Resource Centre (1 per group), leaving a deposit of £20.

## *4.1: Marking Overview*

This assignment will be undertaken in groups, but with the assistance of peer marking, an individual mark will be derived for each student.

The ***group marks*** for this assignment are composed as detailed in Section 1. The overall group mark will be returned as a grade, e.g. A = 70%+, B = 60 - 69%, C = 50 - 59%, and so on.

***Peer marks*** will be obtained via MyPlace, collated, and used to weight the group mark to achieve an ***individual mark*** for each student. Note that peer marking scores are private and will not be disclosed to other students.

The process for peer marking is as follows.

- Let us assume that a group comprises 3 students, A, B, and C.
- Each student has a total of ***40 marks x number of group members*** (e.g. 120 marks for a 3-person group)
- Each student independently and anonymously allocates these 120 marks to the members of their group, including themselves. For instance, Student A may consider that he/she made a reasonable contribution, Student B contributed strongly, and Student C was largely absent and contributed little. (S)he may therefore decide to allocate A = 45, B = 55, and C = 20, giving a total of 120 marks as required.
- Peer marks are moderated and averaged to find the overall peer mark for each student.
- The peer mark is used to weight the group mark to reflect individual contributions. Students' individual marks may therefore be higher or lower than the group mark.

## *4.2: Written Submission*

The written submission should be submitted via MyPlace, by **5pm on Friday 31st March (Week 11)**, one per group.

The written submission should include both (i) the technical report on the practical work, and (ii) the essay on your assigned semiconductor company. There is no word or page limit as such, but for guidance, the expected length is 20 - 30 pages, to include the following:

- A title page
- An abstract
- A statement of academic integrity, signed by all group members
- Clear titles for each section, together with page, section and figure numbering
- An introduction that details the design problem being addressed, along with functional requirements and any assumptions or design decisions.
- A top-down discussion of the design.
- Details of implementation in VHDL code.
- Simulation and hardware testing results and discussion.

- Synthesis and implementation results, and discussion (e.g. how many resources are needed on the FPGA?).
- A description of the organisation of the project, and a reflection on the team working aspect
- Conclusion
- References

An appendix can be added to include the commented code, supplementary design details, simulation results, etc.

### *4.3: Demonstration*

Each group will be required to give a short demonstration on their practical work, and answer any questions arising. Demonstrations will take place during the lab session in Week 11 (Friday 31st March).

Groups are responsible for ensuring that ALL group members are present and participate in the demonstration. Any student who is absent from the demonstration without appropriate evidence (e.g. a medical certificate) cannot be awarded any marks for that part of the assignment.

### *4.4: Teamwork and Attendance*

A small part of the marks for the assignment (10%) can be gained from good management of the project, including working well as a group, and demonstrating this through good attendance and conduct in lab sessions, a coherent demonstration, evidence of planning, and appropriate reflection on these aspects in the report.

All group members are expected to attend the weekly lab sessions and to be present at the demonstration.

## 5: Participation and Fair Warning

This assignment is a core piece of coursework and it is NOT optional. Any student who does not complete the assignment, or makes an inadequate contribution to their group, will not be able to complete the module and gain the credits.

If a member of your group does not attend or participate in the work, and/or you have trouble contacting them, please raise this issue as soon as possible.

## 6: Academic Integrity

There are certain expectations regarding academic integrity which must be met:

- This is a group project and all group members are expected to contribute fairly to the work undertaken.
- It is permitted to discuss your work with other groups, however, the work progressed by each group must be its own — copying from other groups is not allowed. It is expected that groups will develop different designs.
- Any other code / subsystems which are integrated into your solution, such as reference designs, should be clearly indicated and the source clearly referenced.
- All text in the written submission should be the work of the group — copying from internet sources, books, the work of other students, etc. is not permitted and will be treated very seriously. If you need to include statements from other sources, clearly indicate this using quotation marks, and provide a reference.
- Copying from the lecture notes is strongly discouraged too — always write in your own words.
- Diagrams should be created for the purpose, rather than copied from the lecture notes or internet sources. If reusing a diagram is unavoidable, then the source must be referenced as a minimum requirement.

- Please be aware that, as a group project, all members of the group are jointly responsible for the submission. If you have any doubts about the conduct of another group member, particularly with respect to academic honesty, please address this prior to submitting any work.