E158 - VLSI Final Project: Tic-Tac-Toe

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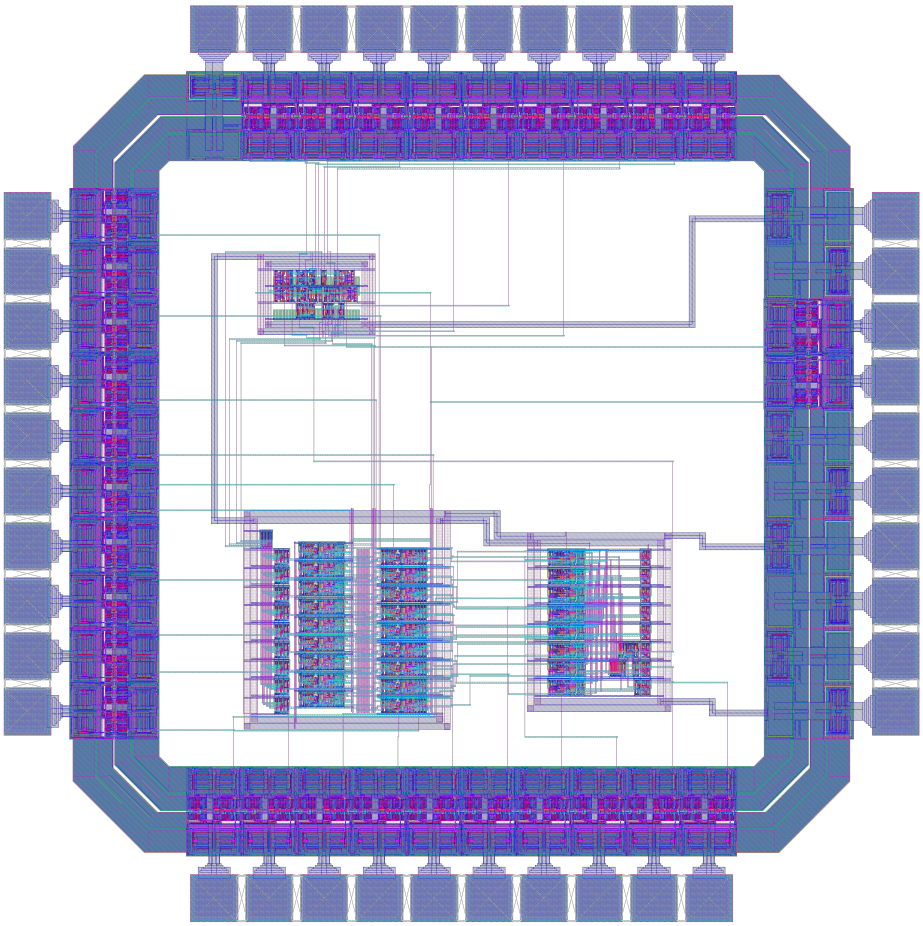

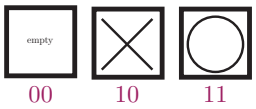

Figure 1: Each cell of the game board is represented using two bits. The MSB is used to describe if the cell has been played or not. The LSB is used to describe who played in the cell.

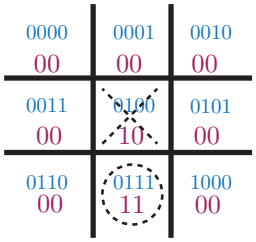

Figure 2: The playable game board is represented by 18-bits. Each pair of bits are used to describe a cell. Each cell holds a two bit value and is accessed with a 4-bit address.

1 Introduction

This project is a 3x3 game of Tic-tac-toe built on a 0.6 μm process on a 1.5×1.5 mm 40-pin MOSIS "TinyChip". The goal of this project was to create a Tic-Tac-Toe board which is able to monitor the state of a game and return the win/loose/draw state of the game after each player's move. Specifically, for each player's turn, the game records the player's inputs and at the end of the game determines if the game is done and who the winner is. The game allows two players to play against each other. Each of the nine spaces can be "X", "O" or blank.

1.1 Game representation

The Tic-tac-toe game board is represented by 8 cells. Each cell is either empty, a cross or a circle using 2-bits as shown in fig. 1. Thus, the game board is represented by an array of 18-bits as shown in fig. 2.

1.2 Architecture

The architecture consists of 3 main modules, one of which was synthesized, and two other were hand laid.

1.2.1 Memory Array

The memory array remembers the status of the tic-tac-toe game board through sequential logic. It consists of enable reset flip-flops and a 4 to 8 bit decoder.

1.2.2 Check Win Status

The win status module is a combinational logic block that checks the win state of the tic-tac-toe board. There are two custom made leaf cells in this module. This cell is very repetitive and can be organised as a datapath.

1.2.3 Game Controller

The game controller module is a finite state machine which switches between players, player input and game board. This module will be synthesized as the structure is more irregular and harder to be hand laid.

Table 1: List of I/O pins for a total of 40 pins

Function (*Name*)	I/O type	Bus Width	Description
Power (*vdd*)	Input/Output	1 (x4)	Provides power
Ground (*gnd*)	Input/Output	1 (x5)	Ground
Reset (*reset*)	Input	1	Resets the board to empty
Clock (*ph1, ph2*)	Input	2	Two phase clock
First Player (*isPlayer1Start*)	Input	1	Determines which player plays "X" or "O"
Write Confirmation (*playerWrite*)	Input	1	Confirms the current player input
Input Position (*playerInput*)	Input	4	Indicates which position on the game board the player played
Winner (*winner*)	Output	2	Displays `11` if player 1 wins, `10` if player 2 wins, and `01` if there is a draw
Game State (*gameState*)	Output	2	Indicates which player's turn it is to play or if the game is done
Game Board (*gBoard*)	Output	18	Displays the current state of the game

2 Specifications

The chip has a total of 31 I/O pins plus 5 GND pins and 4 VDD pins. User input is a 4-bit vector (`playerInput<3:0>`) to describe the cell number at which to play. The write input signals the game controller that the playerInput is ready to read/write. `gameState<1:0>` is used to represent the state of the game: player 1's turn, player 2's turn or end. As the name implies `winner<1:0>` describes who won the game: player 1, player 2, tie when the game is not done. To prevent hold time issues, the system will be using two non-overlapping clocks. Thus, the chip uses a two-phase clock with pins `ph1` and `ph2`. A list of all inputs can be found in table 1.

3 Floorplan

Figure 4 shows the chip floorplan for the tic-tac-toe chip including the pad frame. The top-level blocks are the *game controller*, the *datapath* and the *memory*. A wiring channel is located between the controllers and datapath and between the datapah and memory to provide room to route control signals to the datapath. The *pad frame* includes 40 I/O pads, which are wired to the pins on the chip package. As listed in table 1, there are 31 pads used for signal; the remainder are V_{DD} and GND. Figure 3 shows the pinout diagram indicating names and pin numbers for each pin.

The floorplan is drawn to estimated scale size in fig. 4. The chip is designed in a 0.6 μm process on 1.5x1.5 mm die so the die is 5000 λ on a side. Each pad is $750\lambda \times 350\lambda$ [1].

3.1 Slice Plans

Both the memory array and the win logic were laid out with 8 words of 2-bit length. A slice plan for the datapath is shown in fig. 5.

4 Verification

All Verilog code successfully simulates using their respective testbenches and sets of testvectors. All schematics were also successfully tested against the same testbenches.

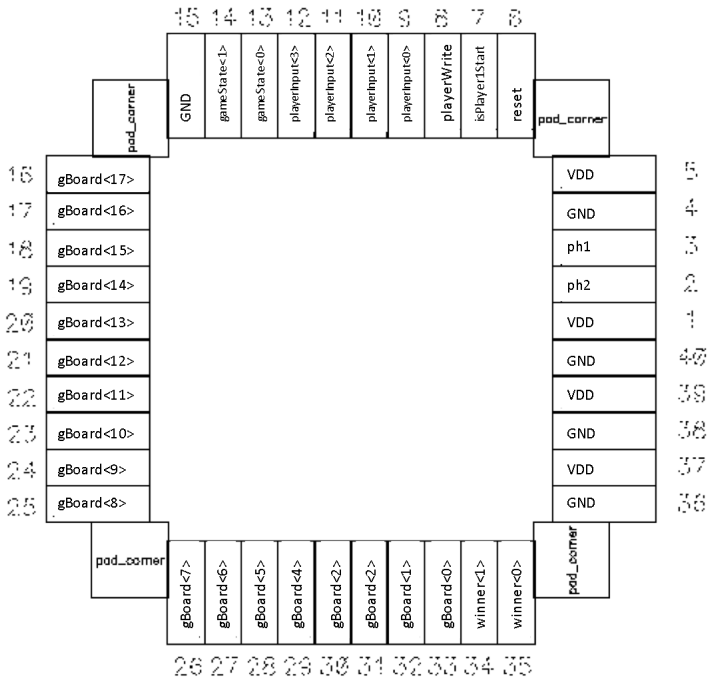

Figure 3: Tic-tac-toe pinout diagram

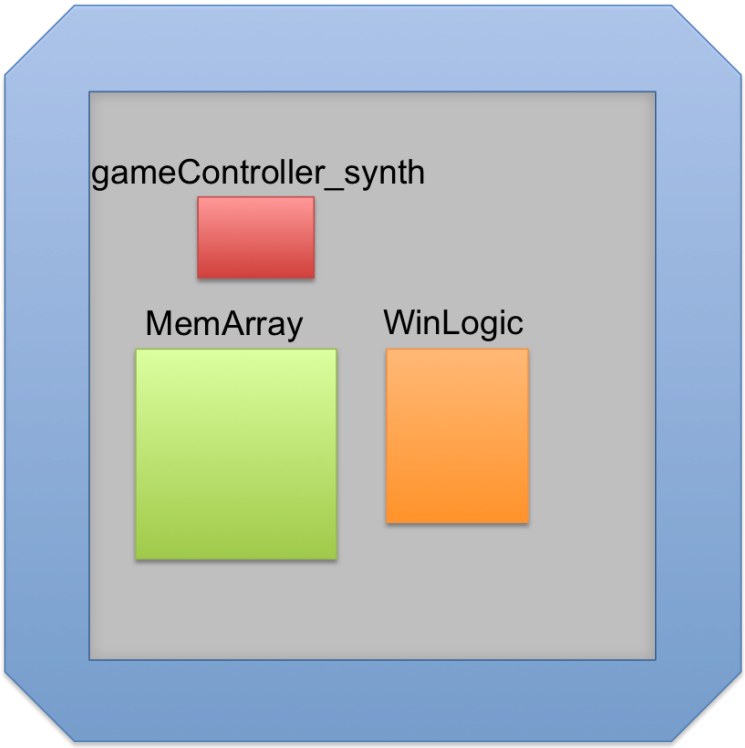

Figure 4: Tic-tac-toe floorplan

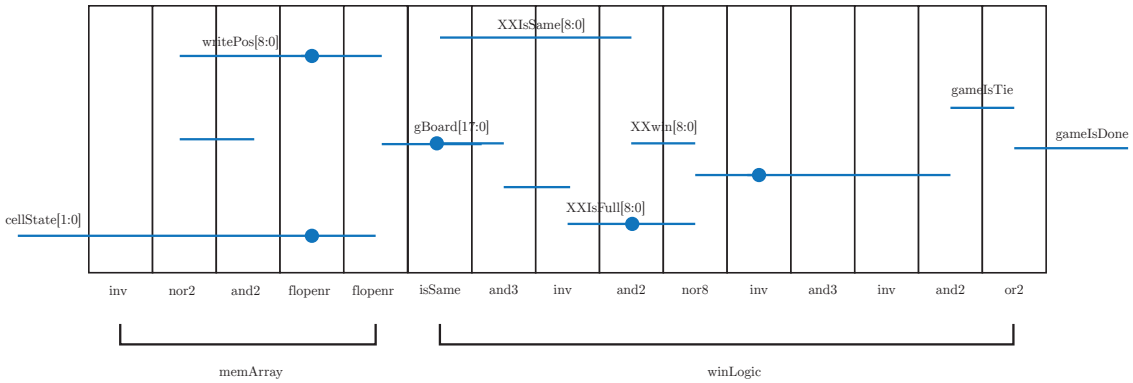

Figure 5: Slice plan for the datapath includes both the *memArray* and the *winLogic*

Table 2: Table of design time for each component

Component	Time Spent (hrs)
Project Proposal	7
Verilog	30
Schematic	20
Layout	40
Total Time spent:	**97**

Every layout component of the system passed DRC and LVS. The exported GDS chip passes DRC with 144 errors related to optional rule 10.4 about spacing from the pad to unrelated metal.

4.1 Postfabrication test plan

If the chip was to be fabricated, recommended would include:

1. V_DD and GND test by appliying power to the chip.
2. inspecting the clock ($ph1$ and $ph2$)
3. connecting switches to inputs and leds to outputs and run parts or all of the test vectors.

5 Summary

5.1 Design Time

A summary of design time spent on each component of the project is shown in table 2

5.2 File Locations

References

[1] David Harris & Sarah Harris, *Digital Design and Computer Architecture*, Morgan Kaufmann; 2nd edition, 2012.

[2] Crowley, Kevin & Siegler, Robert S. *Flexible Strategy Use in Young Children's Tic-Tac-Toe*, Cognitive Science; Issue 4, Volume 2, 1993.

[3] Max Korbel & Ian Jimenez *Simplified Checkers*, E158: Introduction to CMOS VLSI Design Lab Report, 2011.

Table 3: File locations for each component

Item	Location
Verilog testbench	https://github.com/glegrain/Tic-tac-toe
Testvectors	https://github.com/glegrain/Tic-tac-toe
Synthesis Results	/home/glegrain/IC_CAD/cadence/texttt*.rep, *pow
GDS	/home/glegrain/IC_CAD/cadence/chip.gds
Cadence Libraries	/home/glegrain/IC_CAD/cadence
PDF of chip plot	https://github.com/glegrain/Tic-tac-toe/report/chip-layout.png
Final Report	

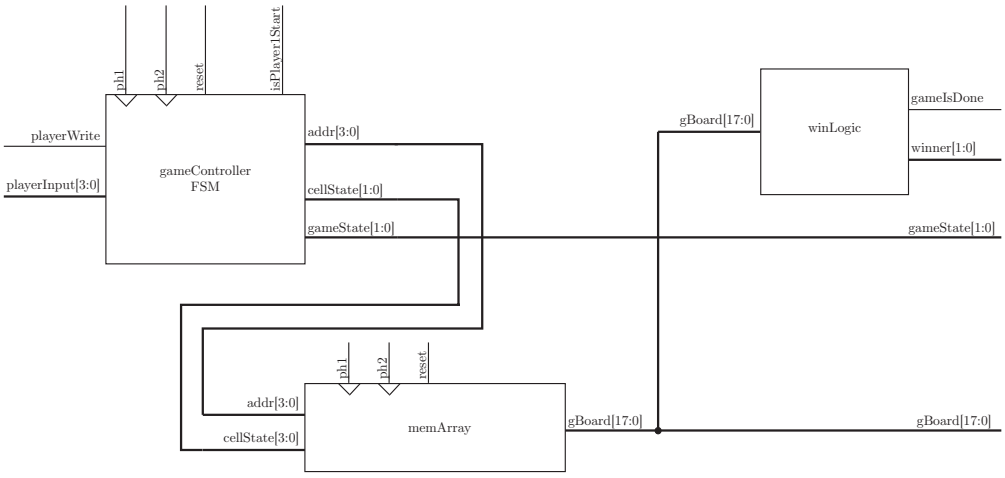

Figure 6: Top Level Block Diagram of the Tic-tac-toe architecture.

Appendices

A Logic Design

A top level diagram in fig. 6 show the different blocks of the architecture.

The blocks are described in each of the sections below. The game controller is in charge of controlling which player is writing to the game board. Player 1 and player 2 enters the address they want to play at, which updates to the memory FF block when it is their respective turn and a write switch is activated. The datapath uses combinational logic determine the winning/losing status of the players.

A.1 Memory Array

The *Memory array* is an array of 18-bit flip-flops (9 words of 2-bits) to store the state of the game board. The memory array incorporates a row decoder using the address (`addr[3:0]` to activate one of the rows by asserting the wordline (`cellState[1:0]`). The decoder logic for the memory can be seen in figure 7.

The decoder logic will be using an estimate of 4 cells per "write" to enable each pairs of flip-flop. Thus, the decoder logic will be using an estimate of 4×9 logic gates which rounds to a rough size estimate of $1000\lambda \times 188\lambda$. The flip-flop array height estimate is $18 \times 100\lambda = 1800\lambda$ and the width is 300λ wide . The total size estimate for the memory block rounded up to $2000\lambda \times 600\lambda$.

A.2 Win logic

Using only the game Board memory array, the win logic checks if a column, row or diagonal is full by looking at the MSB of each cell. If yes, then the logic checks if all the cells in the column, row or diagonal are all the same by looking at the LSB of each cell using a custom leaf cell called `isSame` described in sec. A.3. The

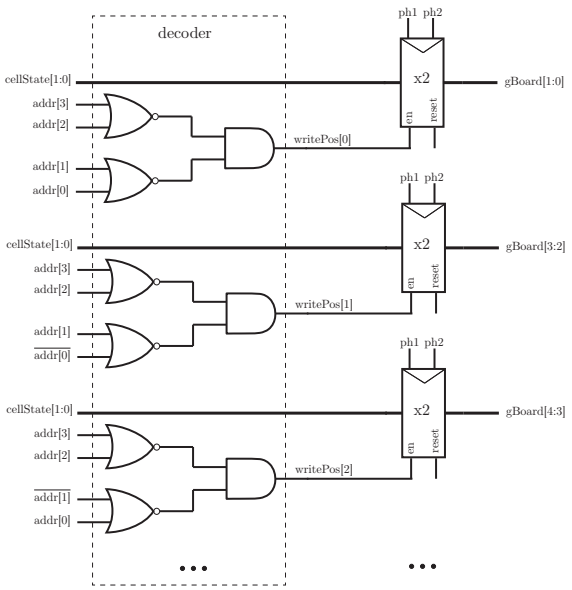

Figure 7: Memory array block made from 18 D-Flip-flops.The row decoder uses the address (`addr[3:0]` to activate one of the rows by asserting the wordline (`cellState[1:0]`).

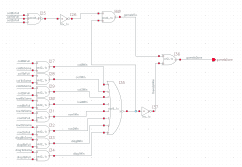

Figure 8: winLogic row, column diagonal check

win logic is also able to determine who is the winner is by checking if each row, column or diagonal has the same cell. Partial schematics for the win logic module can be found in fig. 8, fig. 9 and fig. 10.

A.3 `isSame` leaf cell

CMOS logic is used to check if 3 bits are identical. This cell is used to determine if the cells are taken by the same agent. The CMOS schematic can be seen in fig. 11.

A.4 FSM desgin: Game Controller

The *Game Controller* contains a finite state machine (FSM) to decide when each player has to play and whether or not the game is done. A state transition diagram for the game controller FSM is shown in figure 12.

B Code, testbenches and test vectors

For clarity reasons, only the chip testbench and testvectors are provided here. All other test files can be found in the paths described in sec. 5.2.

../chip$_t$*b.sv../chip.tv../chip.sv../memArray.sv../winLogic.sv../gameController.sv*

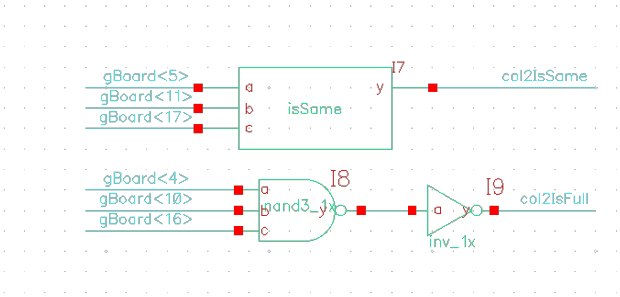

Figure 9: winLogic isSame and isFull check from game-board

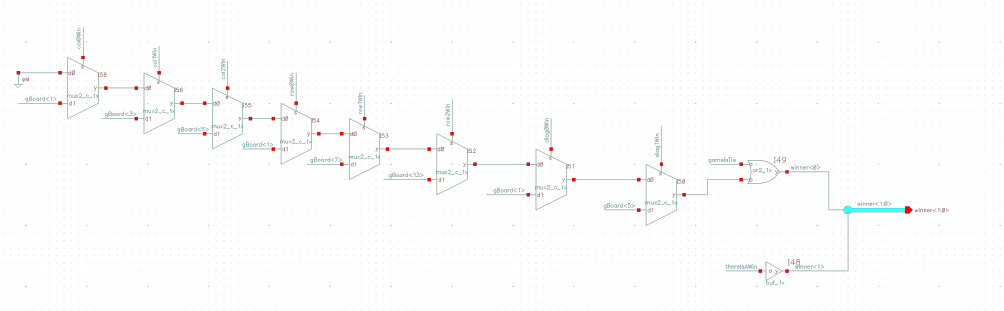

Figure 10: winLogic winner select block

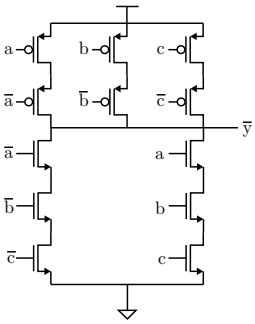

Figure 11: isSame leaf cell logic

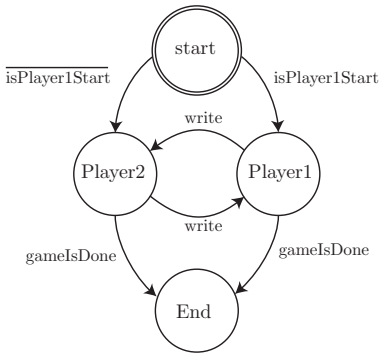

Figure 12: Game Controller Finite-State-Machine

C Schematics & layouts

C.1 gameController

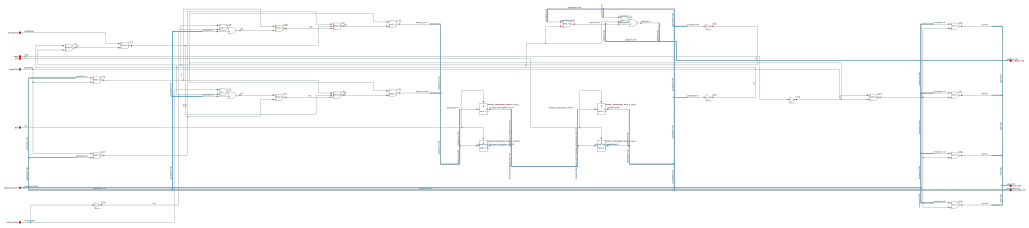

Figure 13: gameController synthetized schematic

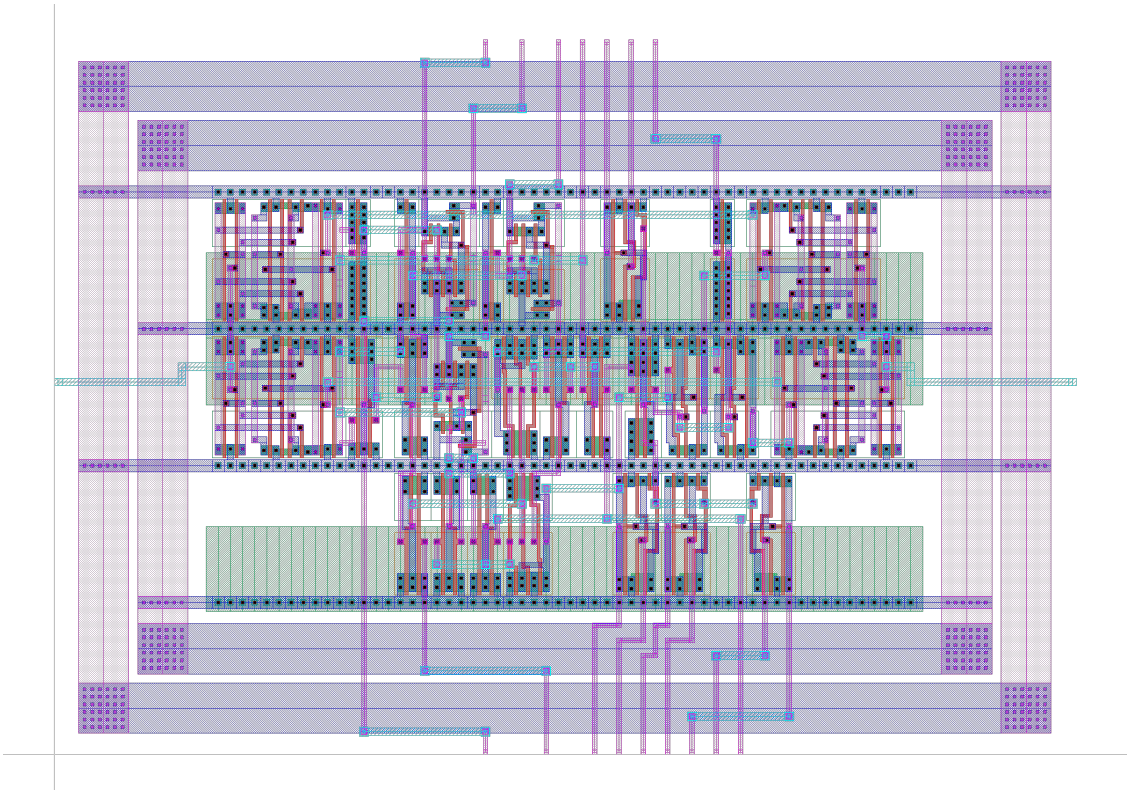

Figure 14: gameController synthetized layout

C.2 winLogic

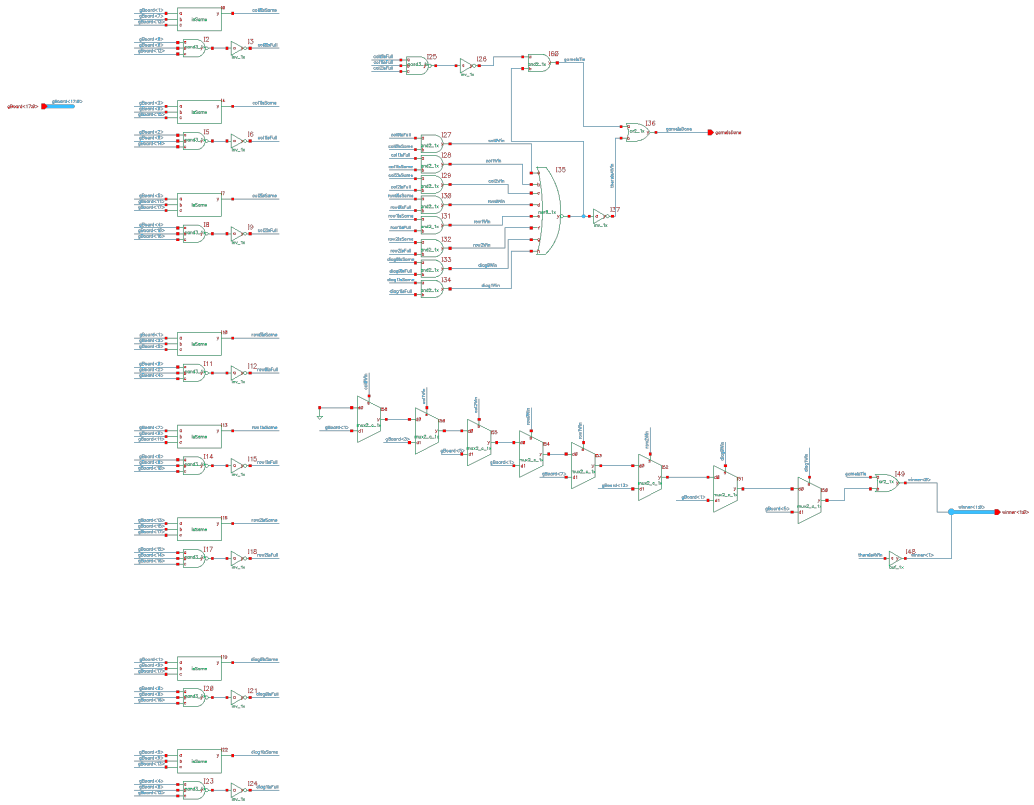

Figure 15: winLogic schematic

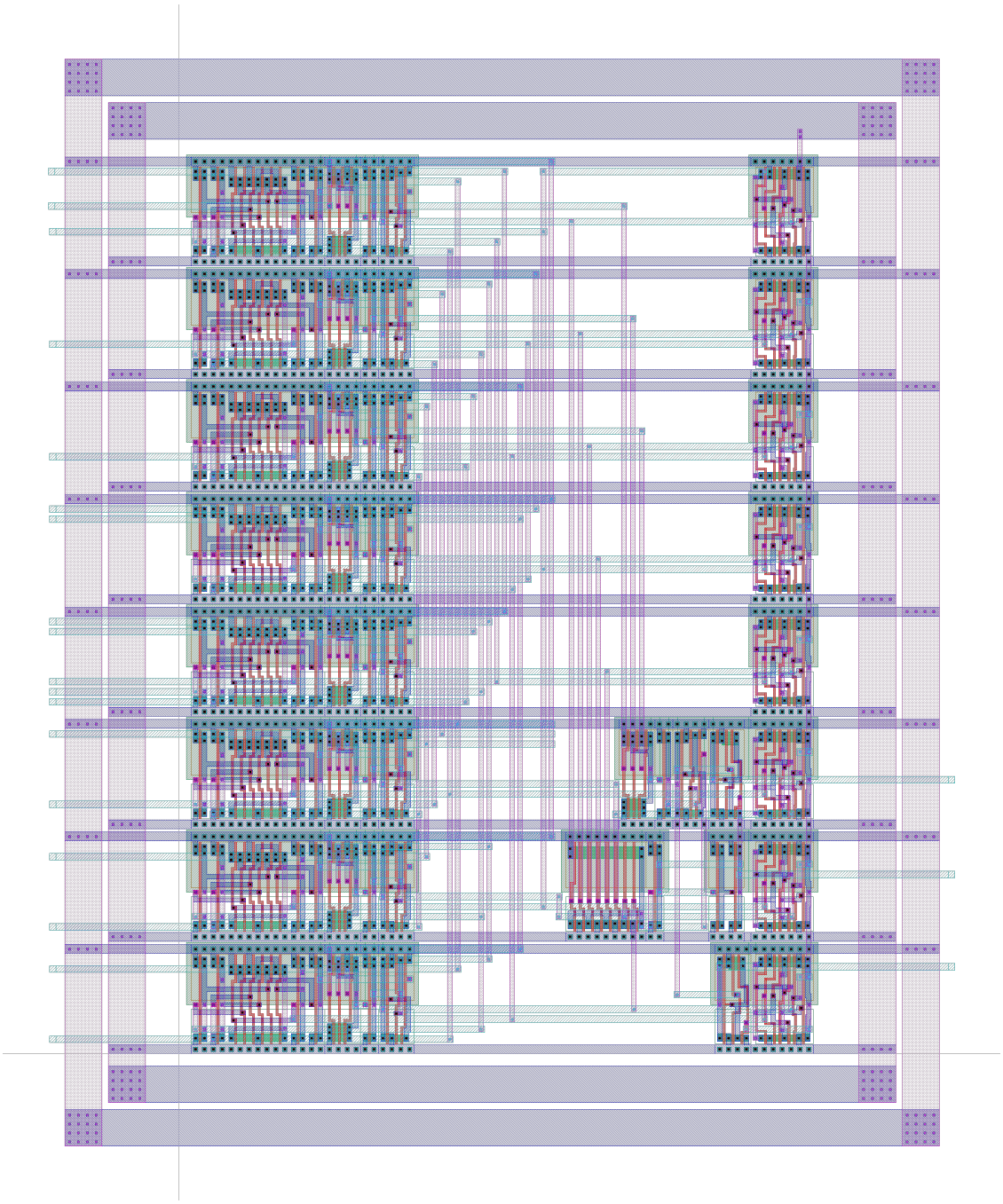

Figure 16: winLogic layout

C.2.1 iSame leaf cell

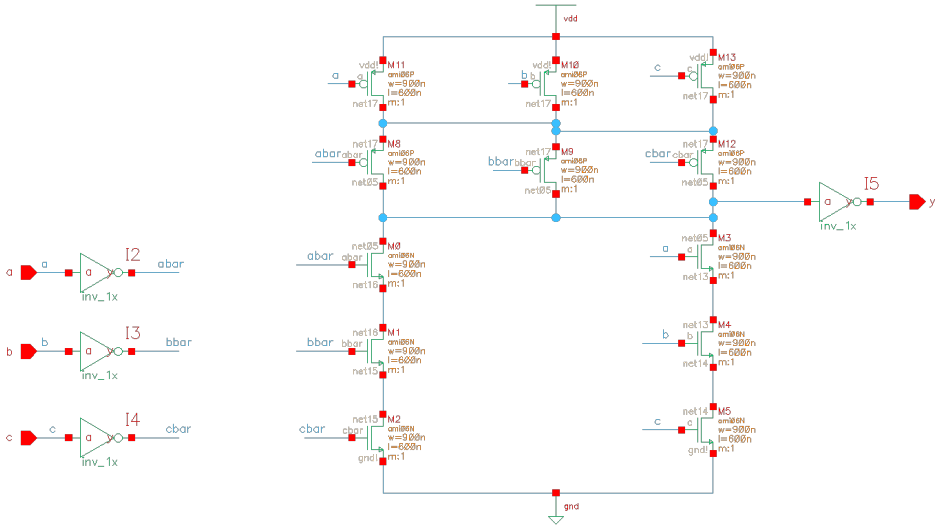

Figure 17: isSame leaf cell schematic

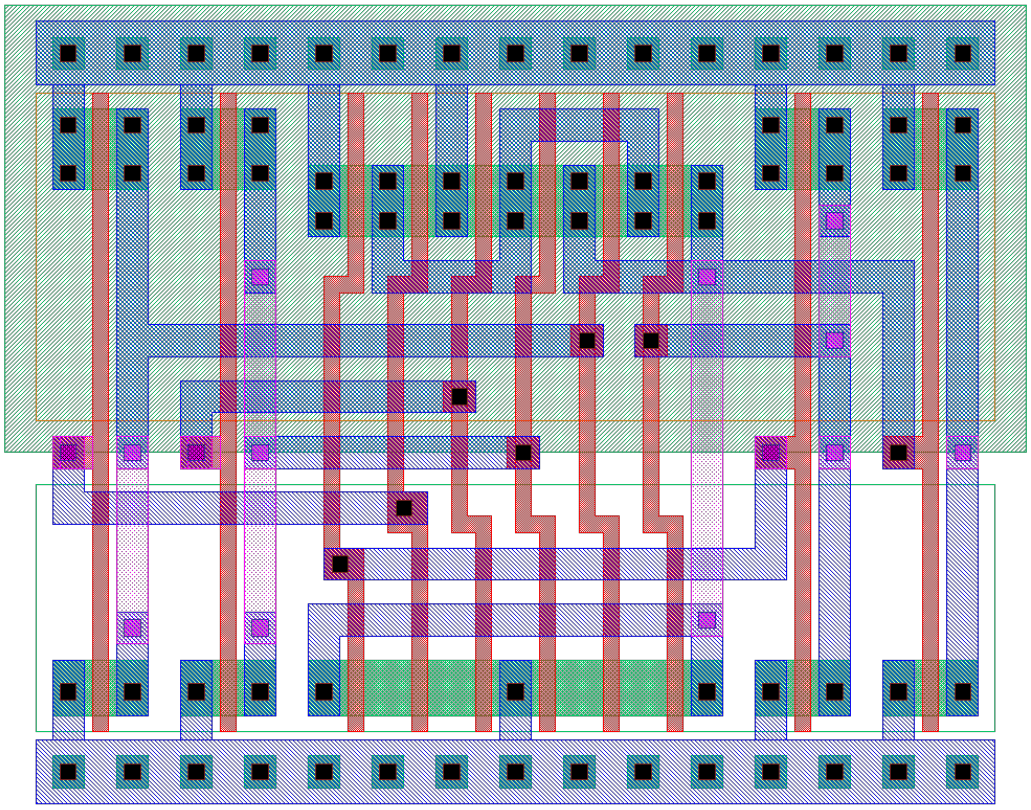

Figure 18: isSame leaf cell layout

C.2.2 nor8_1x leaf cell

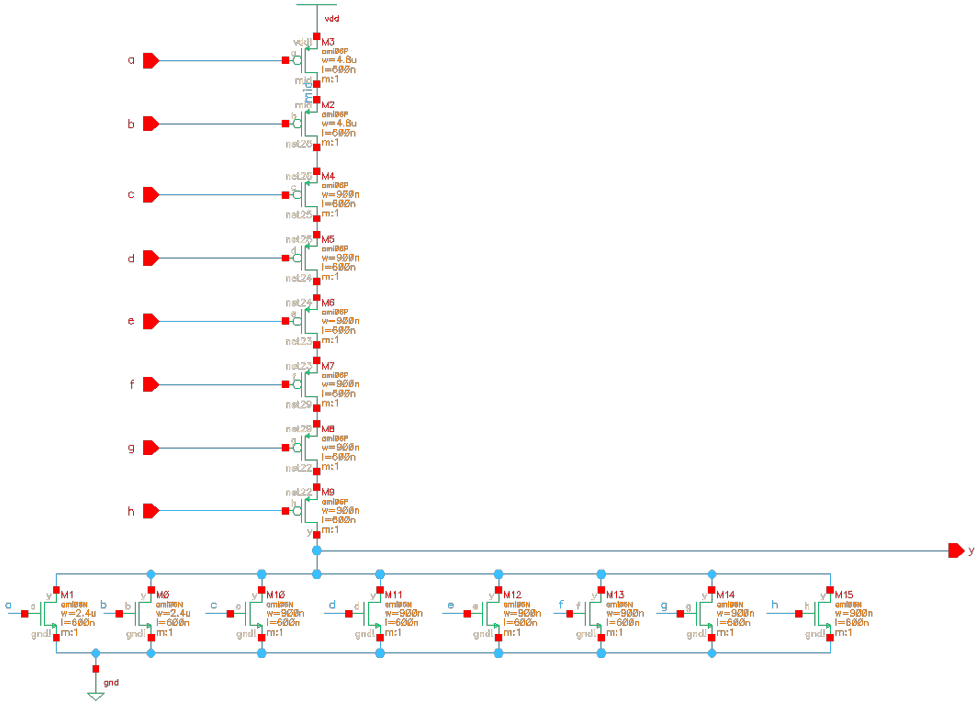

Figure 19: nor8_1x cmos schematic

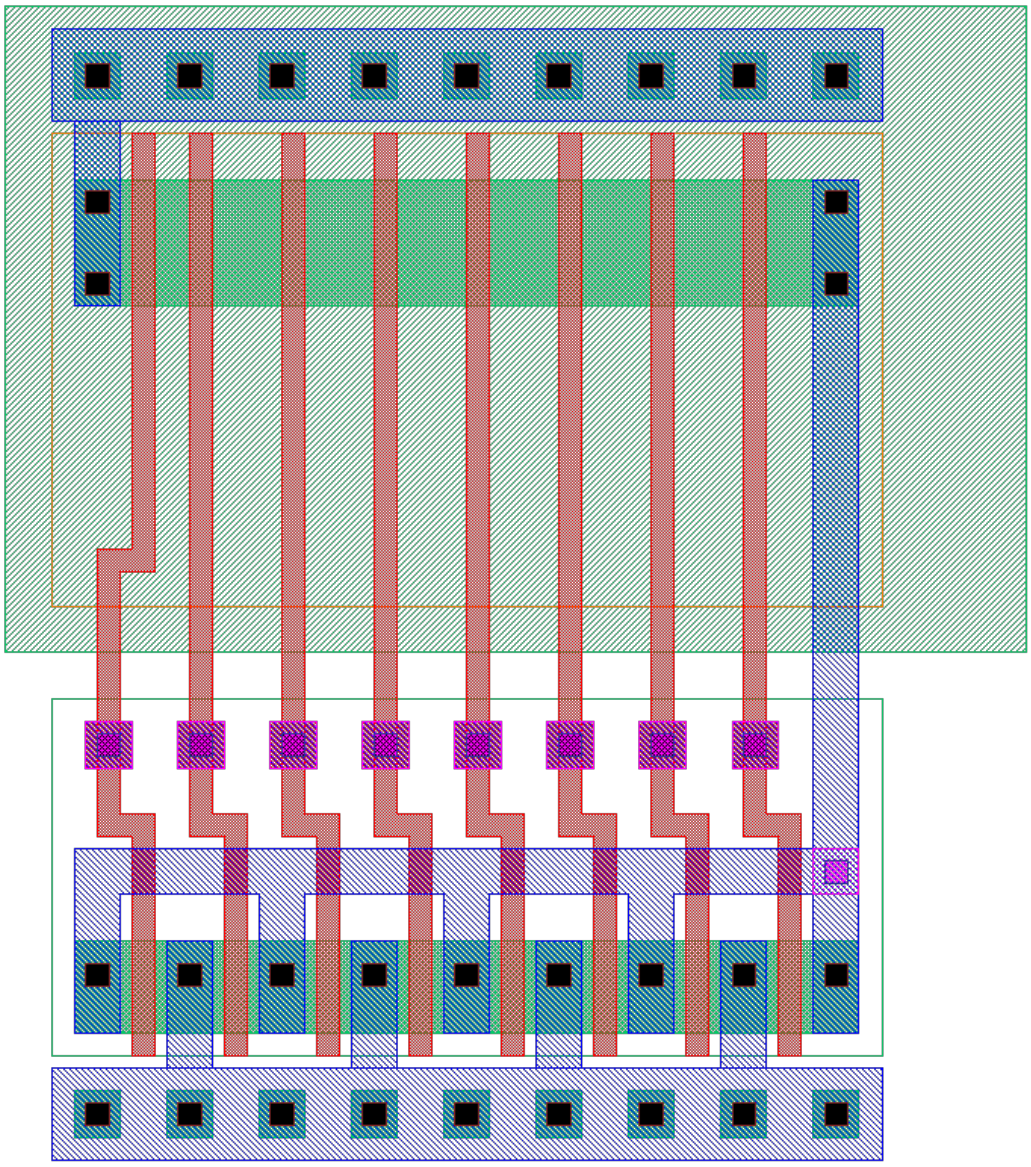

Figure 20: nor8_1x layout

C.3 memArray

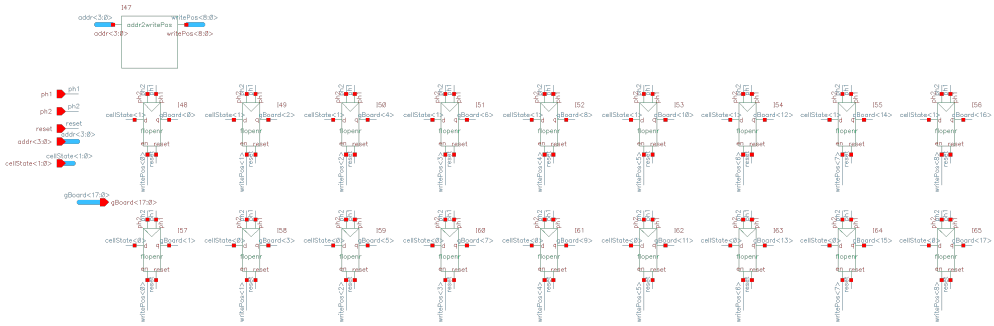

Figure 21: memArray schematic

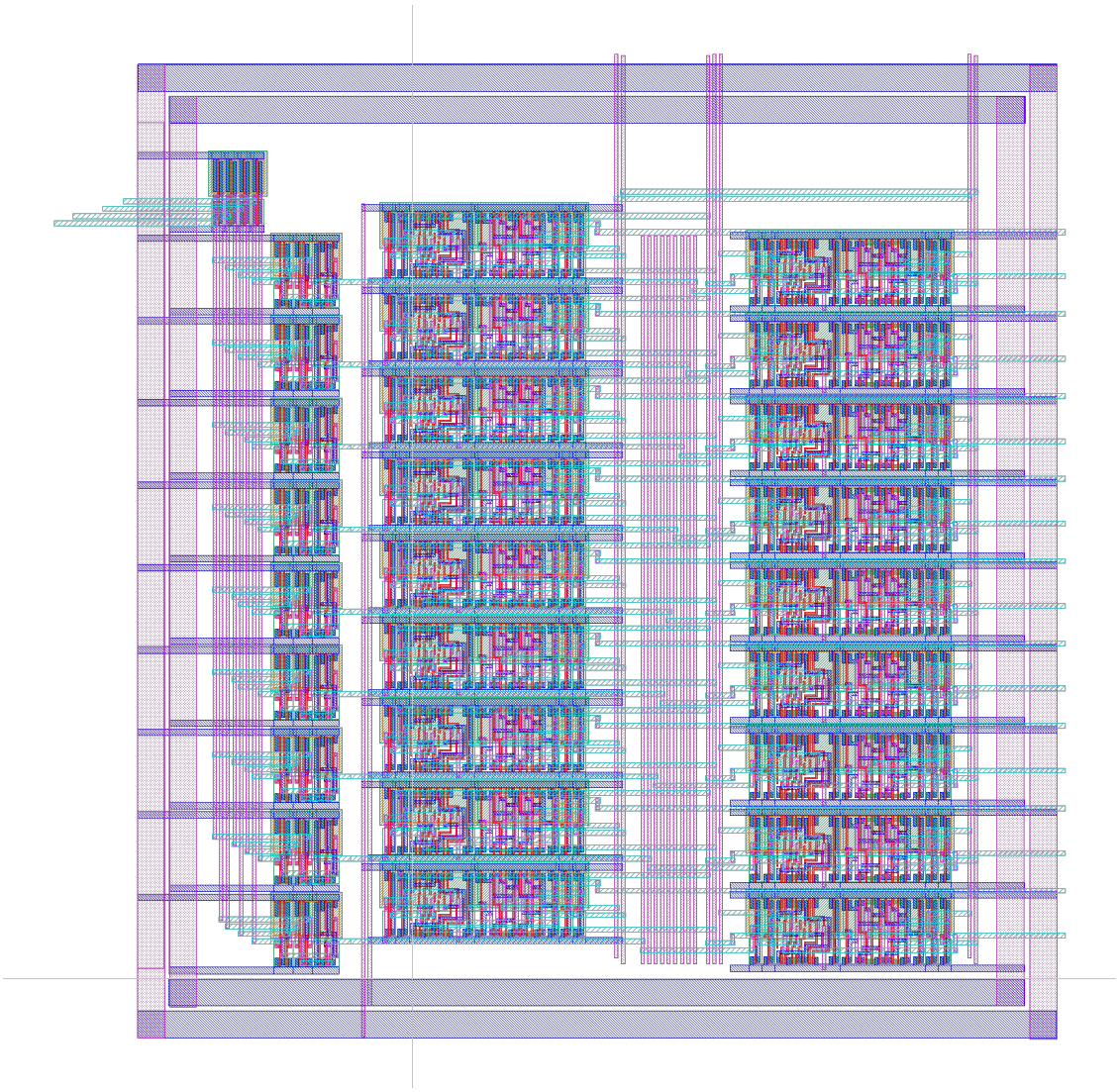

Figure 22: memArray layout

C.3.1 addr2pos

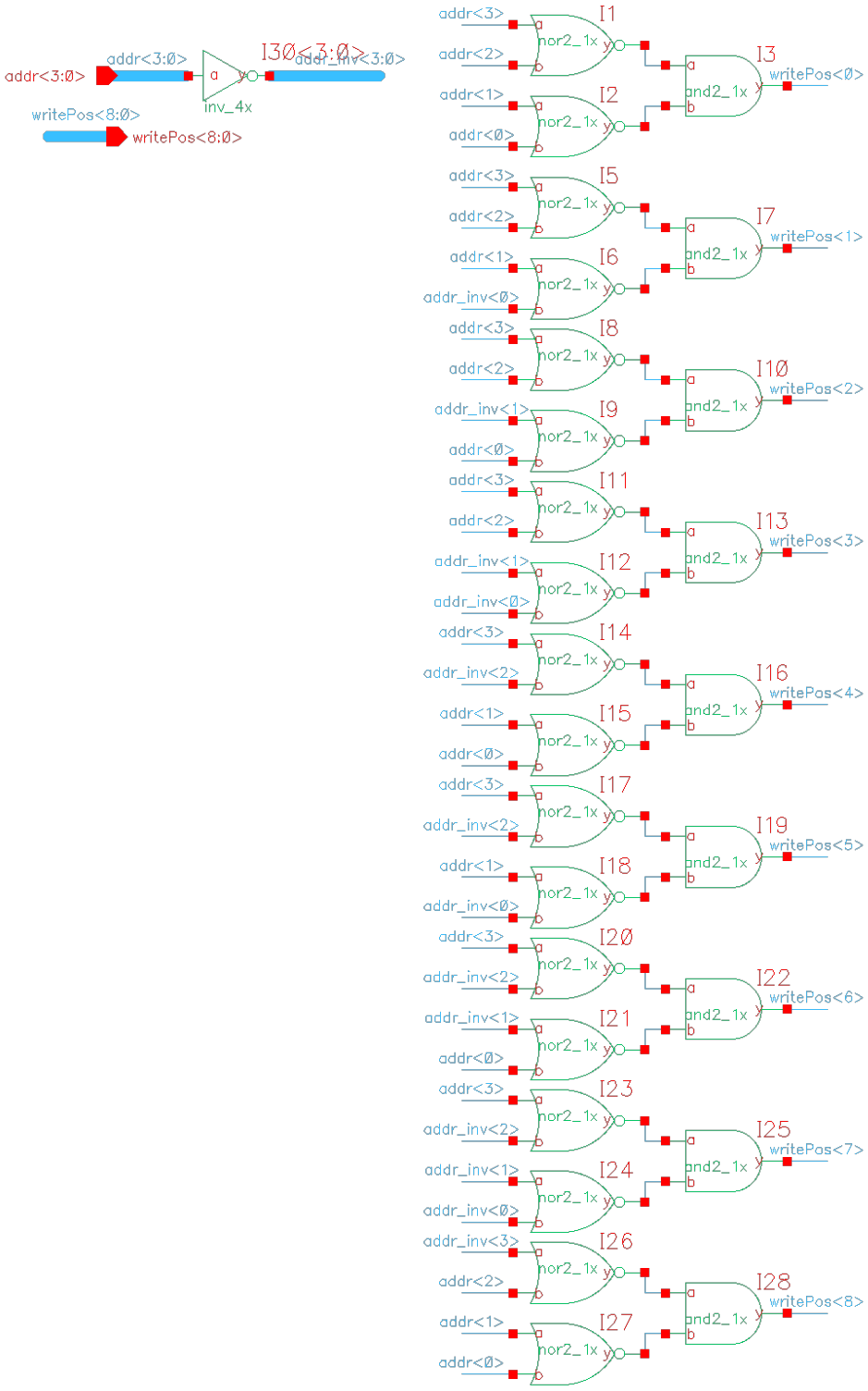

Figure 23: addr2writePos layout

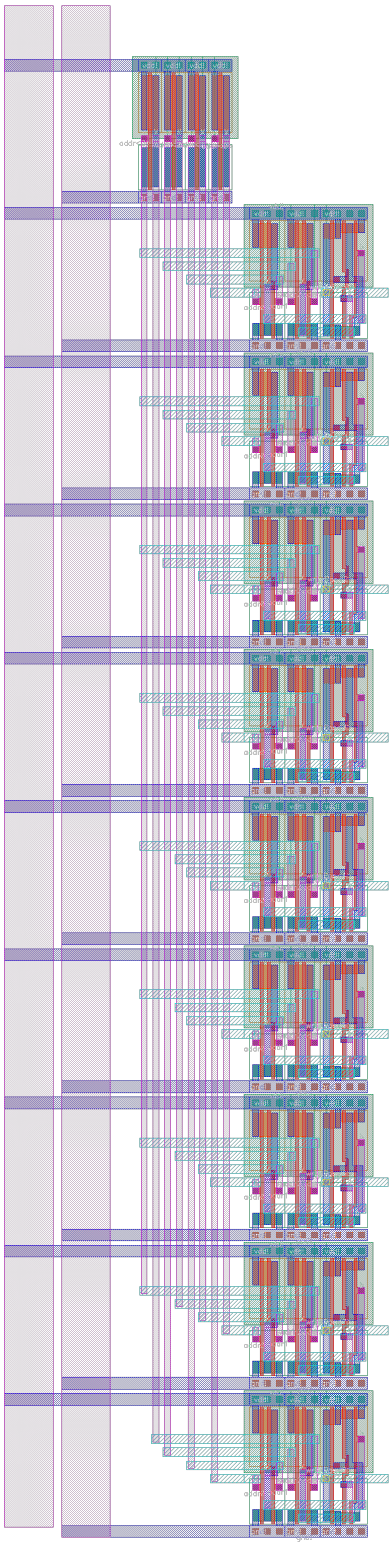

Figure 24: addr2writePos layout

C.3.2 flopenr

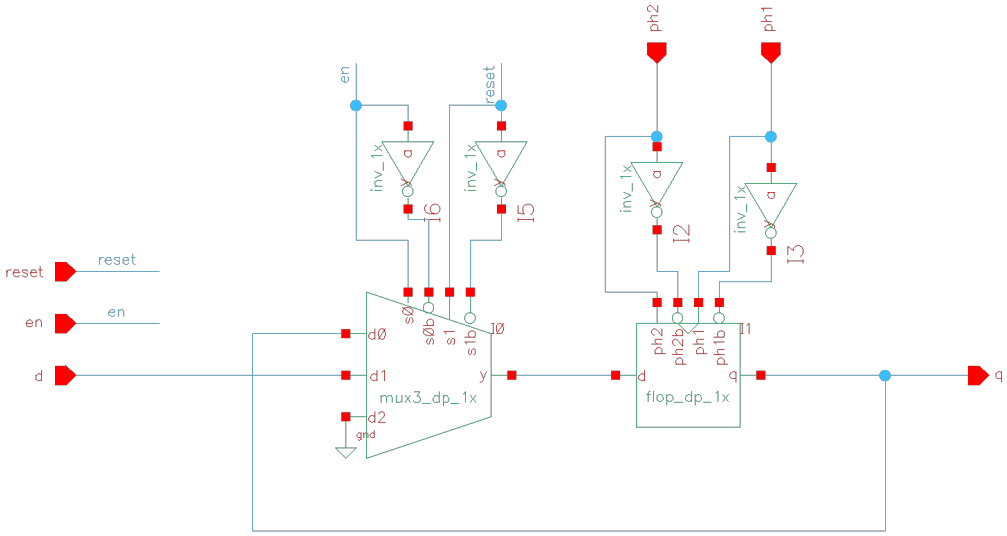

Figure 25: flopenr layout

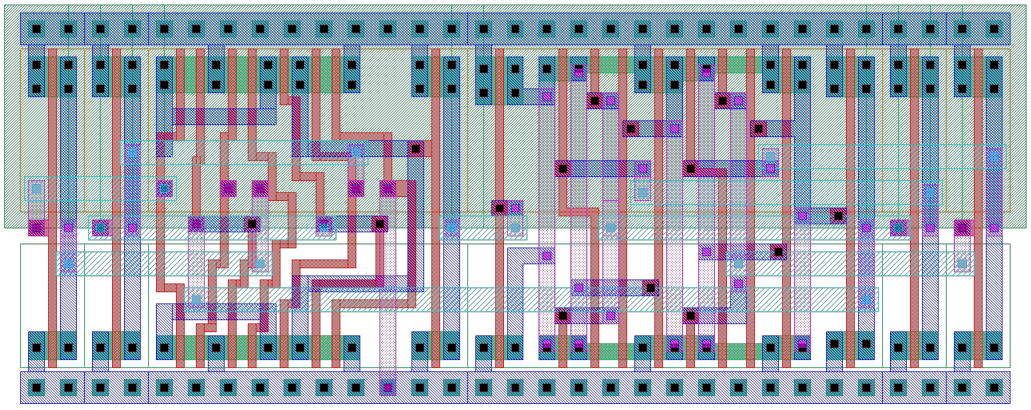

Figure 26: flopenr layout

C.4 Padframe

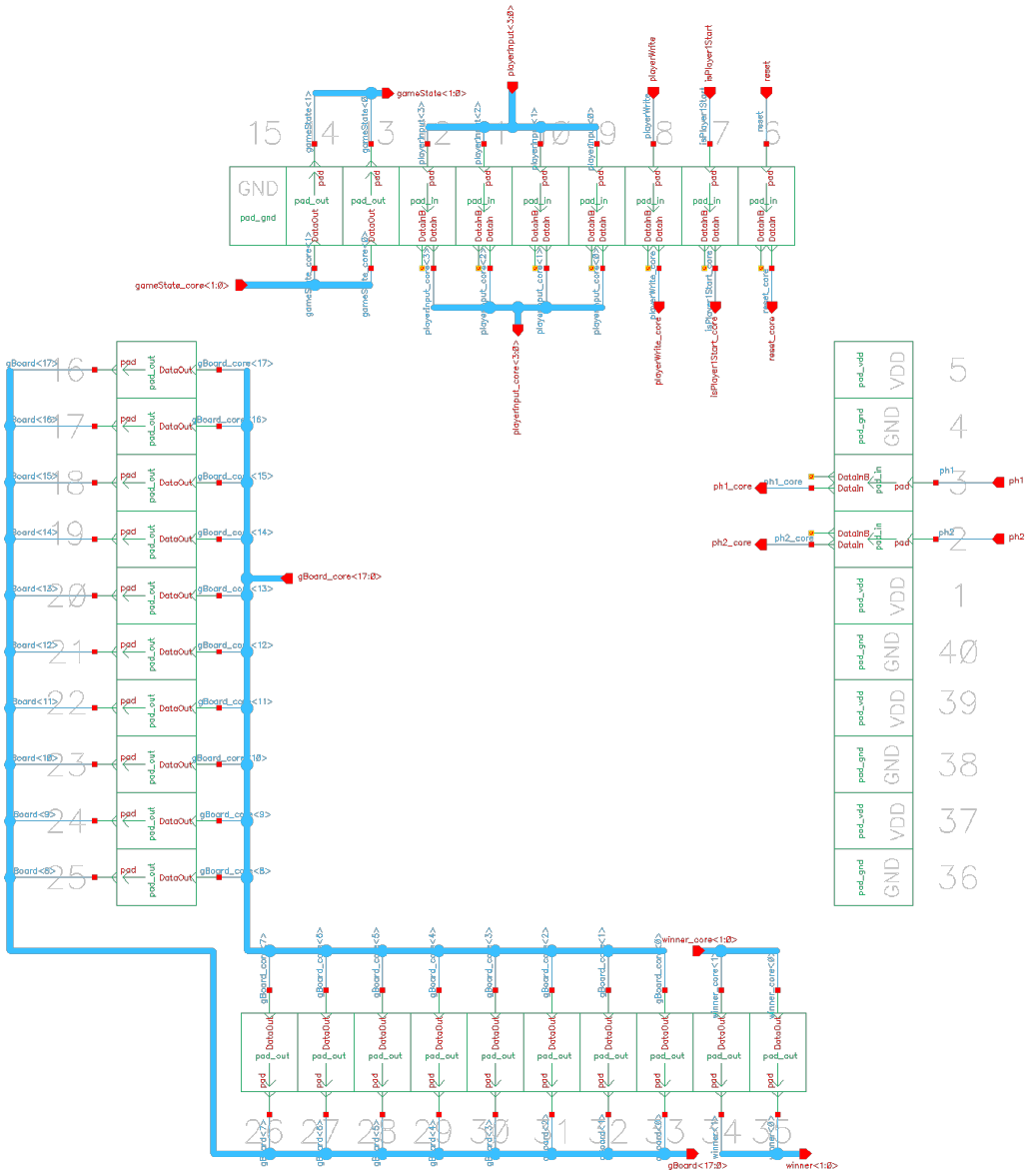

Figure 27: Padframe schematic

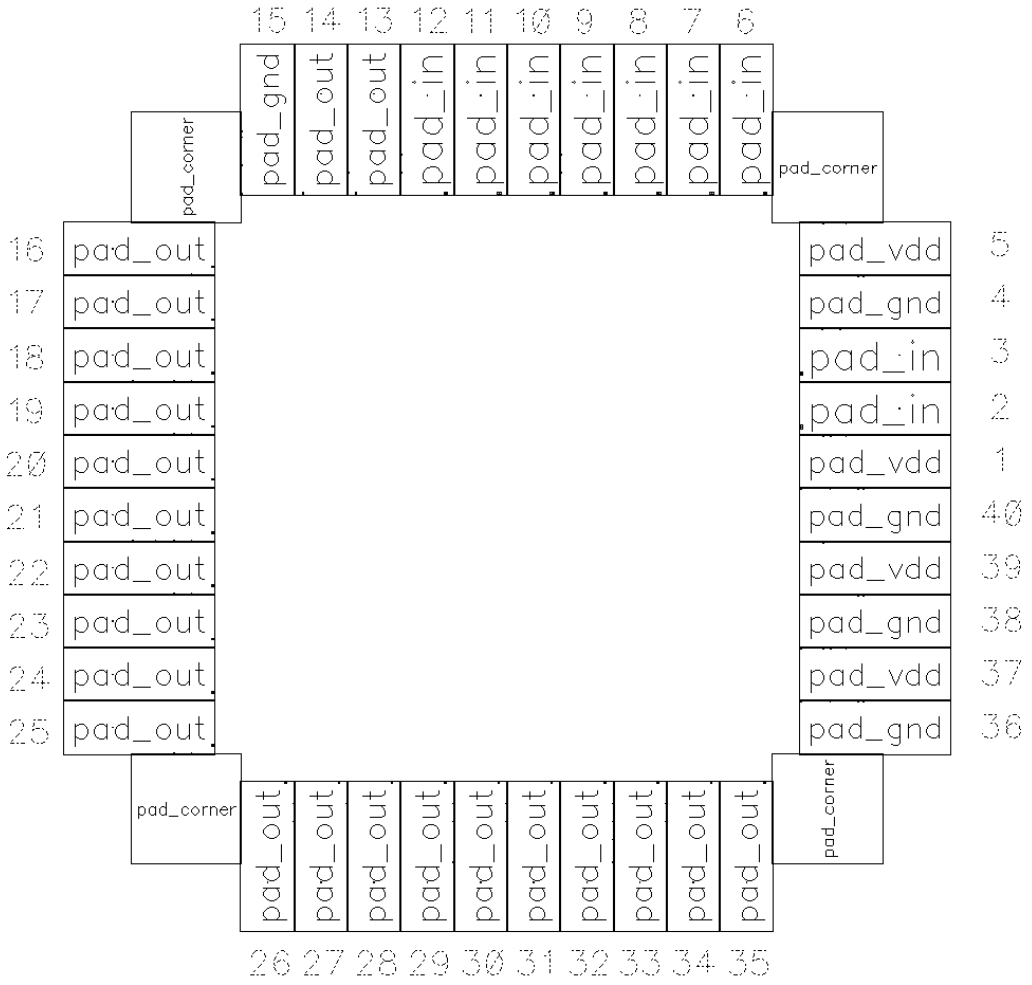

Figure 28: Padframe layout

C.5 chip

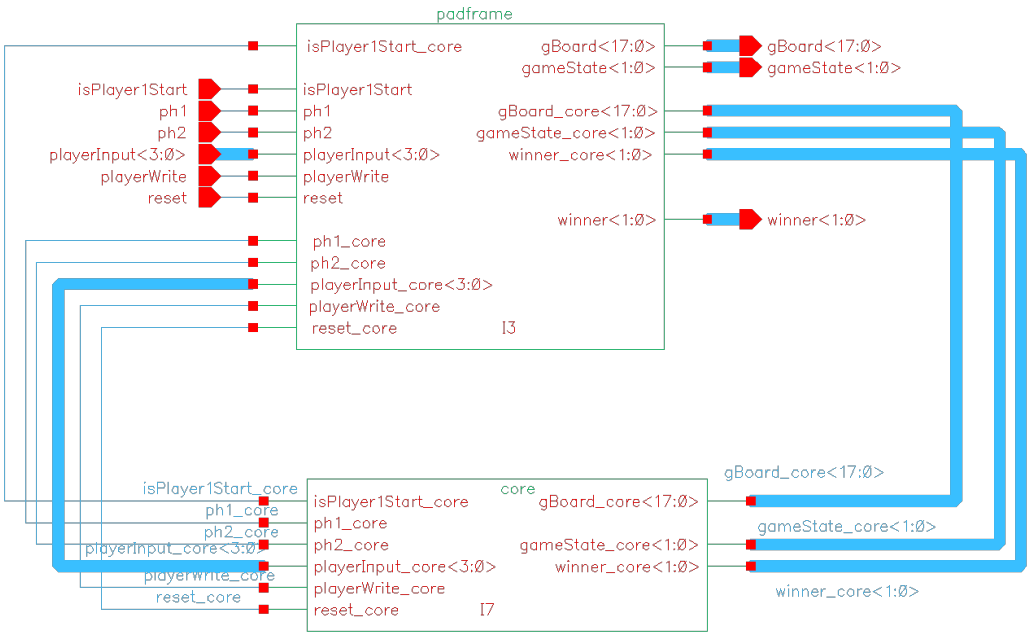

Figure 29: Chip schematic

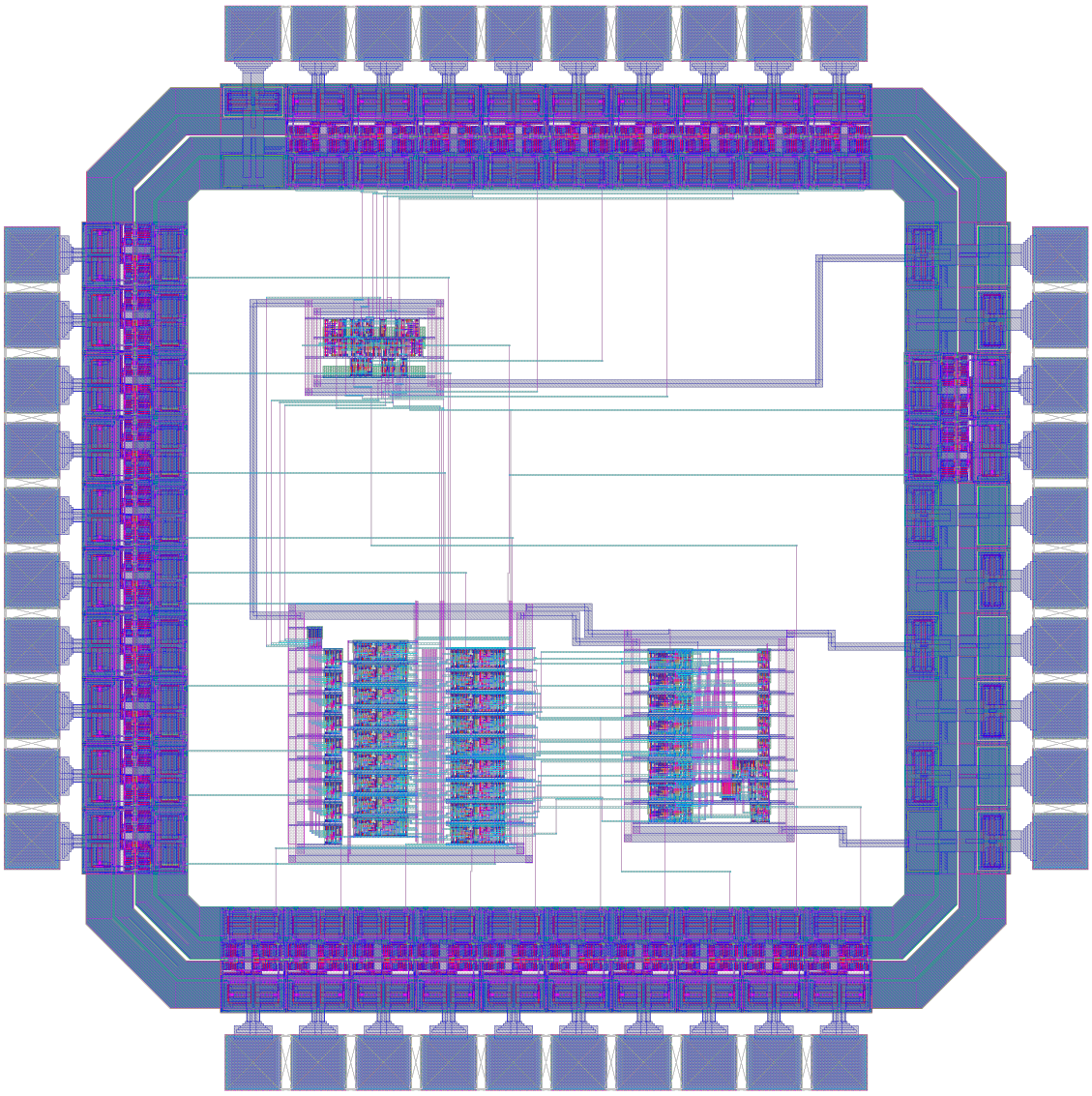

Figure 30: Chip layout