Lab Notebook

FPGA Capstone Project

Academic Integrity

By signing below you acknowledge the CU Honor Code, "On my honor, as a University of Colorado Boulder student I have neither given nor received unauthorized assistance" applies to this assignment.

Signed: _Glenn Frey Olamit_____

Module 1

Setup

Author: Glenn Frey Olamit
Date: January 27, 2022
Procedure/Description of Test: SETUP AND TEST THE DE10-LITE DEVELOPMENT KIT

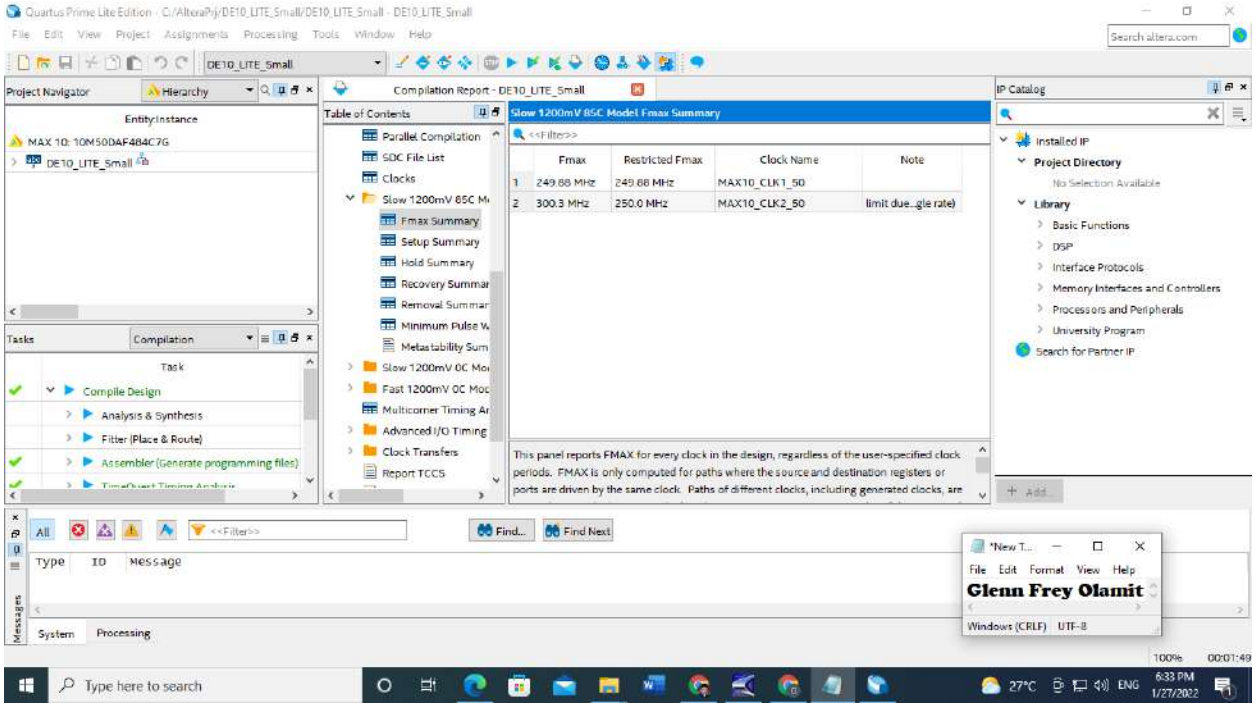
Observations:

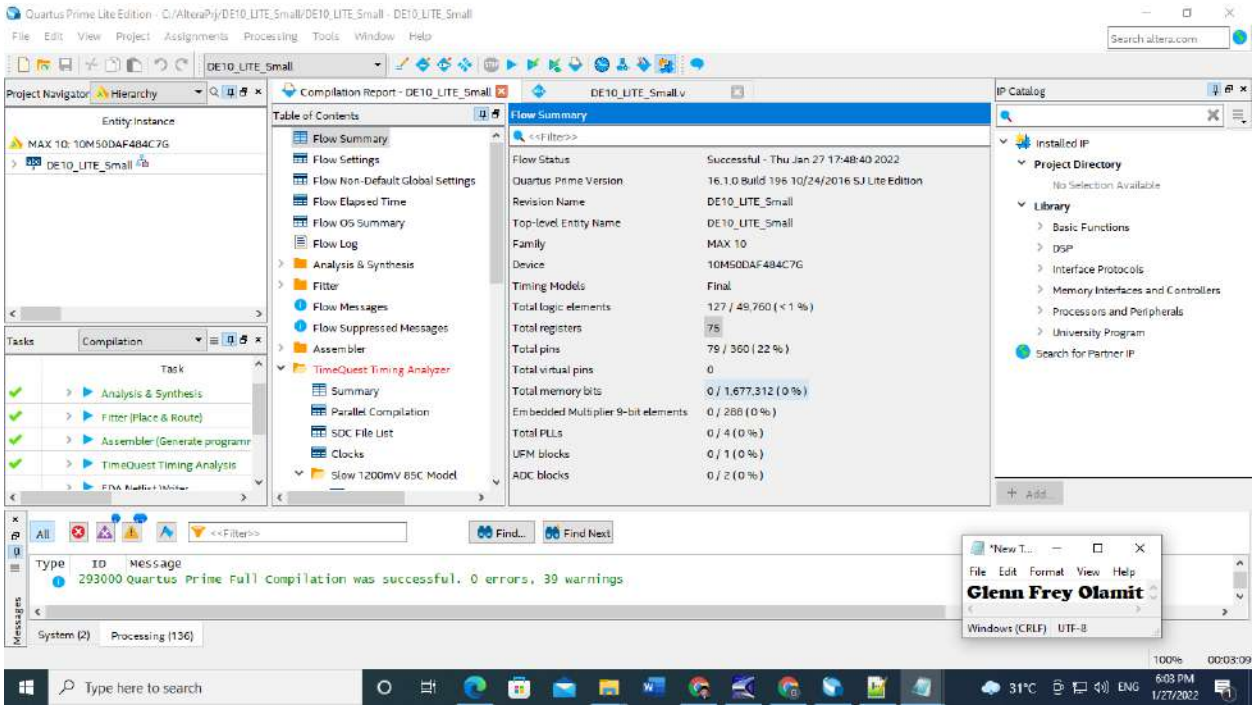
1. In my first compilation of project DE10_LITE_Small I received an error saying "SW not defined line 73". So I entered "input [9:0] SW" in DE10_LITE_Small.v and recompiled.
2. In project DE10_LITE_Default I see a request to upgrade IP.
3. I also received an error saying "Error (16031): Current Internal Configuration mode does not support memory initialization or ROM. Select Internal Configuration mode with ERAM." I resolved this error by changing configuration mode from Single Uncompress Image to Single Uncompress Image with Memory Initialization in the Assignments->Device->Device and Pin Options-> Configuration-> Configuration mode.
4. Upon powering on the board, all six of the seven-segment displays are cycling through hex 0-F continuously. The LED pattern of light is alternating from odd to even.

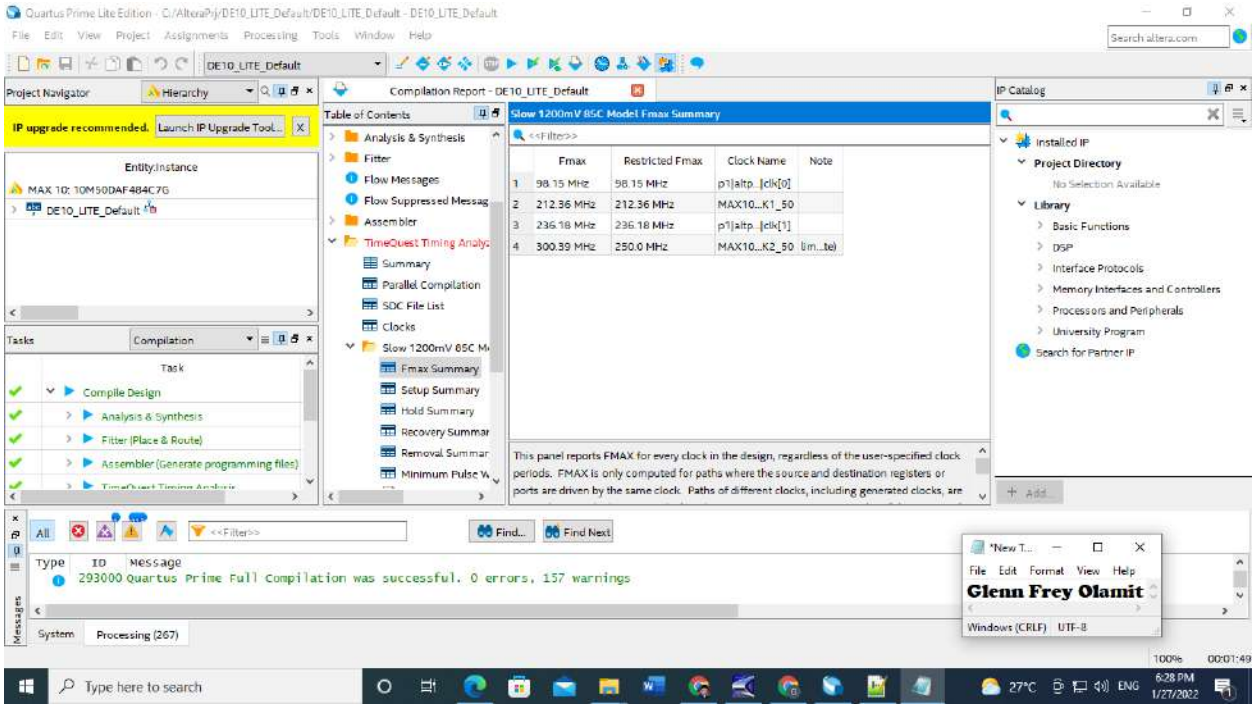
Data:

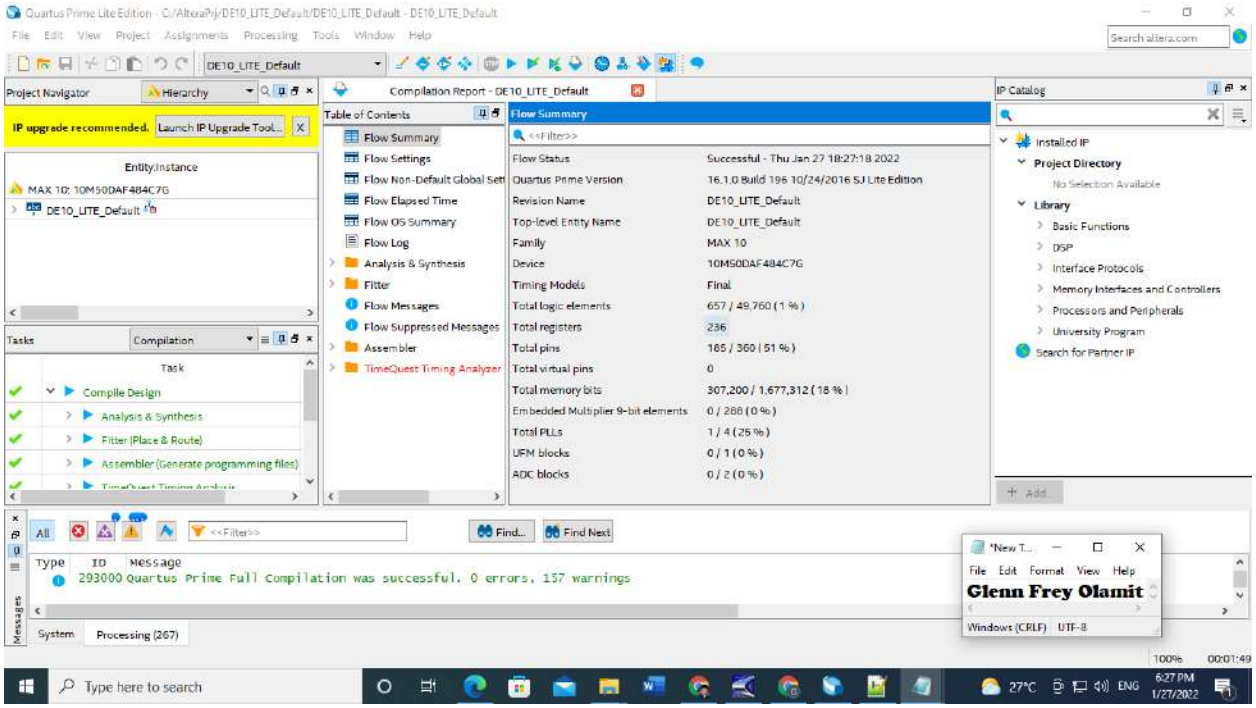
Fmax, logic utilization, and number of flip-flops.

Images/Drawings:






Slow 1200mV 85C Model Fmax Summary
Fmax
Restricted Fmax
Clock Name
Note
1 98.15 MHz 98.15 MHz p1|altp_|clk[0]
2 212.36 MHz 212.36 MHz MAX10...K1_50
3 236.18 MHz 236.18 MHz p1|altp_|clk[1]
4 300.39 MHz 250.0 MHz MAX10...K2_50
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are
293000 Quartus Prime Full Compilation was successful. 0 errors, 157 warnings
Glenn Frey Olamit
Type here to search


Flow Summary
Flow Status Successful - Thu Jan 27 18:27:18 2022
Quartus Prime Version 16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name DE10_LITE_Default
Top-level Entity Name DE10_LITE_Default
Family MAX 10
Device 10M50DAF484C7G
Timing Models Final
Total logic elements 657 / 49,760 (1 %)
Total registers 236
Total pins 165 / 360 (51 %)
Total virtual pins 0
Total memory bits 307,200 / 1,677,312 (18 %)
Embedded Multiplier 9-bit elements 0 / 288 (0 %)
Total PLLs 1 / 4 (25 %)
UFM blocks 0 / 1 (0 %)
ADC blocks 0 / 2 (0 %)
293000 Quartus Prime Full Compilation was successful. 0 errors, 157 warnings
Glenn Frey Olamit
Type here to search

Results:

DE10_LITE_Small	
Fmax	249.88 MHz
Logic Utilization %	127 / 49,760 (< 1 %)
# Flip-Flops	75

DE10_LITE_Default	
Fmax	212.36 MHz
Logic Utilization %	657 / 49,760 (1 %)
# Flip-Flops	236

Questions:

1. Record your observations of the board behavior once the FPGA is programmed. Does it behave as you might expect?

DE10_LITE_Small: The six seven-segment displays are still continuously cycling through hex 0-F, but in LEDs only 5 and 6 are lit. Yes I expected this based on the code.

DE10_LITE_Default: The six the seven-segment displays are cycling through hex 0-F continuously. The LED pattern of light is alternating from odd, even, to all continuously. Yes I expected this based on the code.

Conclusions: Using system builders speed up the project. After correcting the error, compiling and downloading the file the FPGA development board works as expected.

Lessons Learned (What did you learn?):

I learned how to use system builder to speed up project development in altera MAX 10. I learn to use Programmer Tool to program FPGA. I learn how to troubleshoot problems in the code using debug console, reports and observing the FPGA board. Check the number of synthesized flip-flops and logic elements and find Fmax. And lastly, setup and test the DE10-LITE development kit.

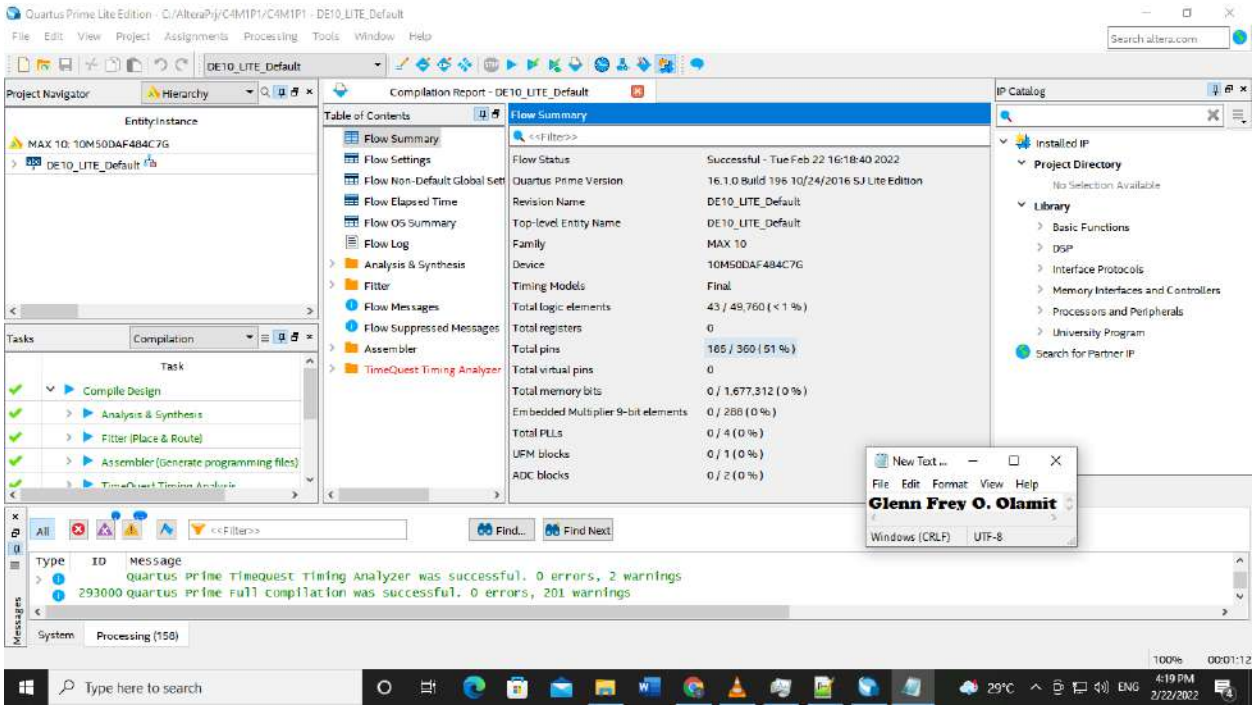
Part 1

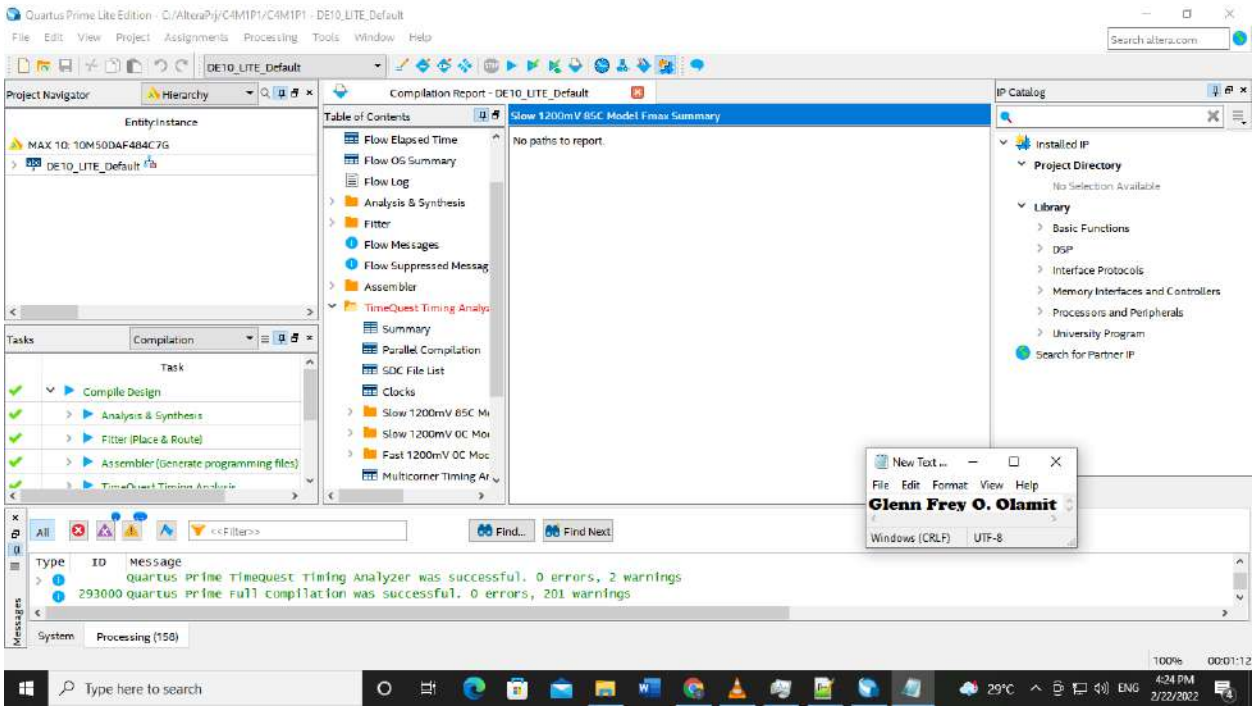
Author: Glenn Frey Olamit
Date: February 22, 2022
Procedure/Description of Test:
To display on the 7-segment displays HEX1 and HEX0 the values set by the switches SW7-0. Let the values denoted by SW7-4 and SW3-0 be displayed on HEX1 and HEX0, respectively. Your circuit should be able to display the digits from 0 to 9, and should treat the valuations 1010 to 1111 as don't cares.

Observations:
Once the board is programmed, the first two 7-segment displays "0"‟0". Then by flipping the switches on or off the seven segment display the value in BCD format with a maximum display value of "9"‟9".

Data:
Fmax, logic utilization, and number of flip-flops used

Images/Drawings:




Quartus Prime Lite Edition - C:/AlteraPrj/C4M1P1/C4M1P1 - DE10_LITE_Default
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Hierarchy
Entity:Instance
MAX 10: 10M50DAF484C7G
DE10_LITE_Default
Compilation Report - DE10_LITE_Default
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Clocks
Slow 1200mV 85C Model Fmax Summary
No paths to report.
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
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Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
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Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
New Text ...
File Edit Format View Help
Glenn Frey O. Olamit
Windows (CRLF) UTF-8
Find... Find Next
Type ID Message
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 2 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 201 warnings
System Processing (158)
Type here to search
29°C
ENG
4:24 PM
2/22/2022


Download DE10-Lite CD
http://de10-lite.terasic.com/cd
terasic
DE10-Lite

Results:

Fmax	NA
Logic Utilization %	43/39760 (<1%)
# Flip-Flops	0

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect? Yes the board behavior is as I expected.
2. Explain the reason for the number of flip-flops used in the design. I use the if else statement in my design which is implemented in a multiplexer which is composed of a logic gate, not a flip-flop which uses a clock.

Conclusions: I was able to design combinational circuits that can perform binary-to-decimal number conversions from binary-coded-decimal (BCD) switch to 7 segment display in DE-10 Lite.

Lessons Learned (What did you learn?): I learned to connect the vhd file to the top level verilog file by instantiating the vhd file in the verilog code. With that I was able to connect inputs and outputs of DE-10 lite to the FPGA logic. I also learned to design combinational circuits that can perform binary-to-decimal number conversions from binary-coded-decimal (BCD) switch to 7 segment display.

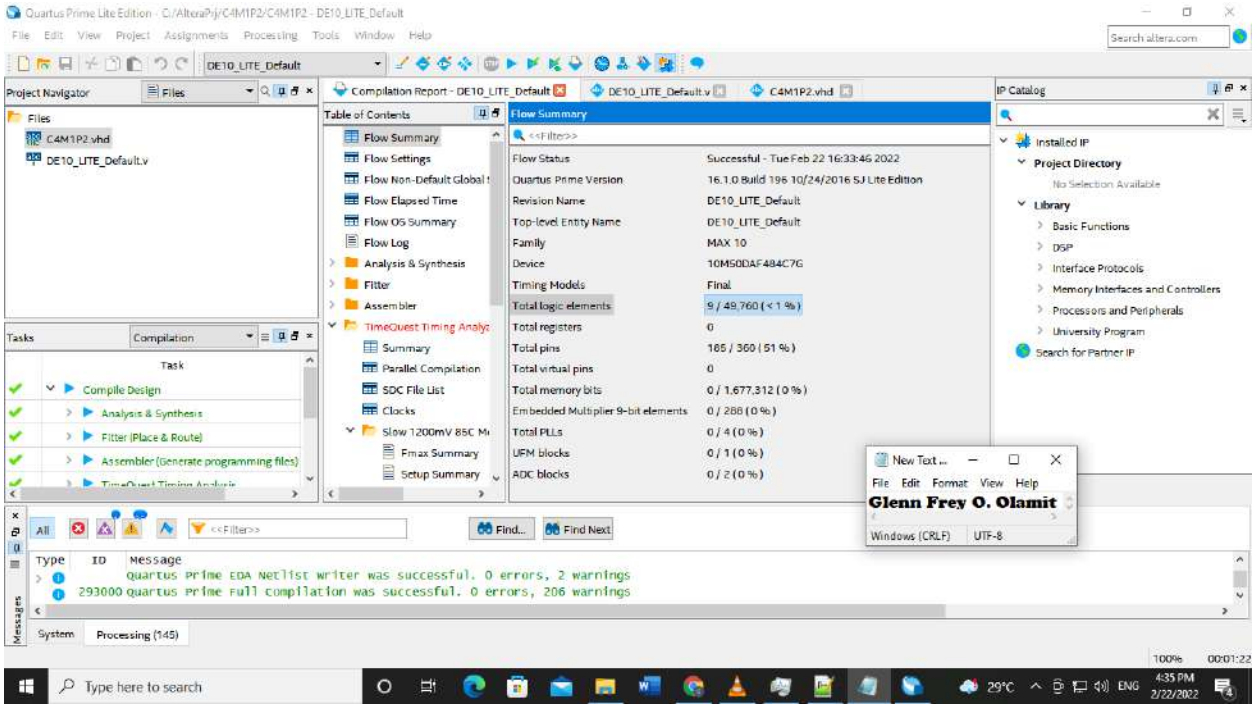
Part 2

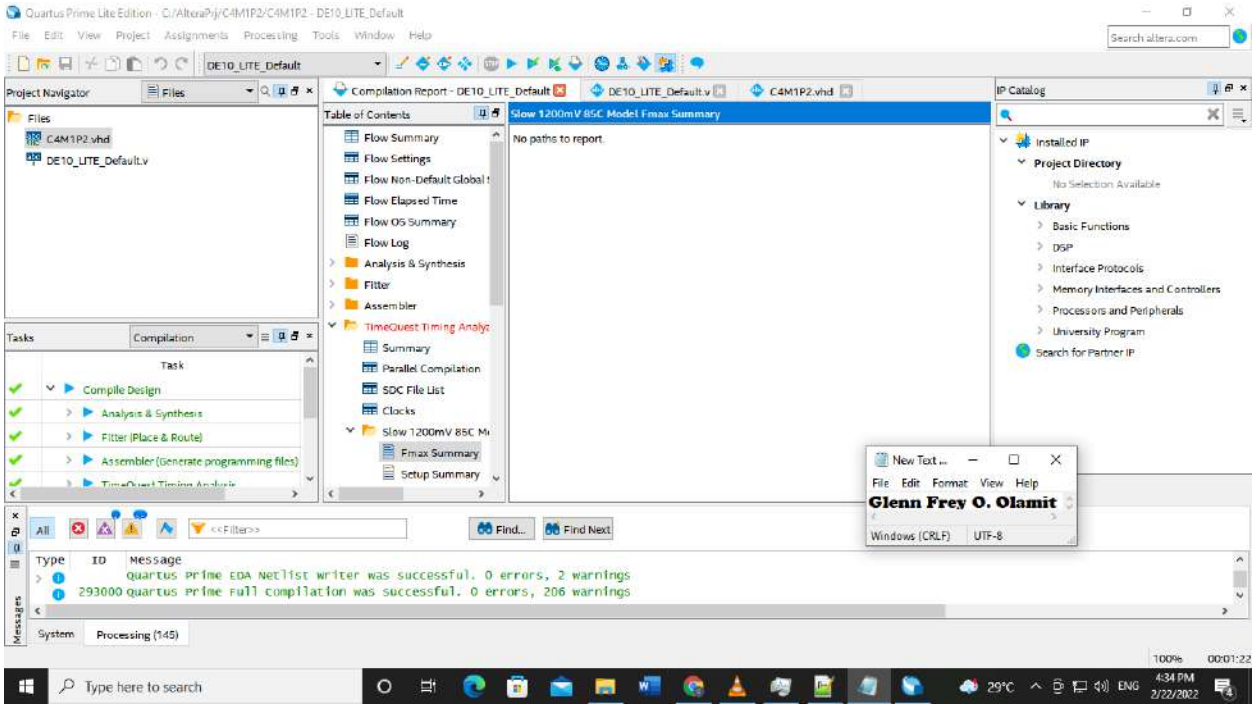
Date: February 28,1990
Procedure/Description of Test:
Design a circuit that converts a four-bit binary number V = v3v2v1v0 into its two-digit decimal equivalent D = d1d0.

Observations:
This circuit uses less logic elements than in Part 1. The circuit design using the boolean logic for the function A circuit. The board functions as expected after programmed.

Data: Fmax, logic utilization, and number of flip-flops

Images/Drawings:




Quartus Prime Lite Edition - C:/AlteraPrj/C4M1P2/C4M1P2 - DE10_LITE_Default
Project Navigator
Files
C4M1P2.vhd
DE10_LITE_Default.v
Compilation Report - DE10_LITE_Default
DE10_LITE_Default.v
C4M1P2.vhd
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Slow 1200mV 85C Model Fmax Summary
No paths to report.
IP Catalog
Installed IP
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Processors and Peripherals
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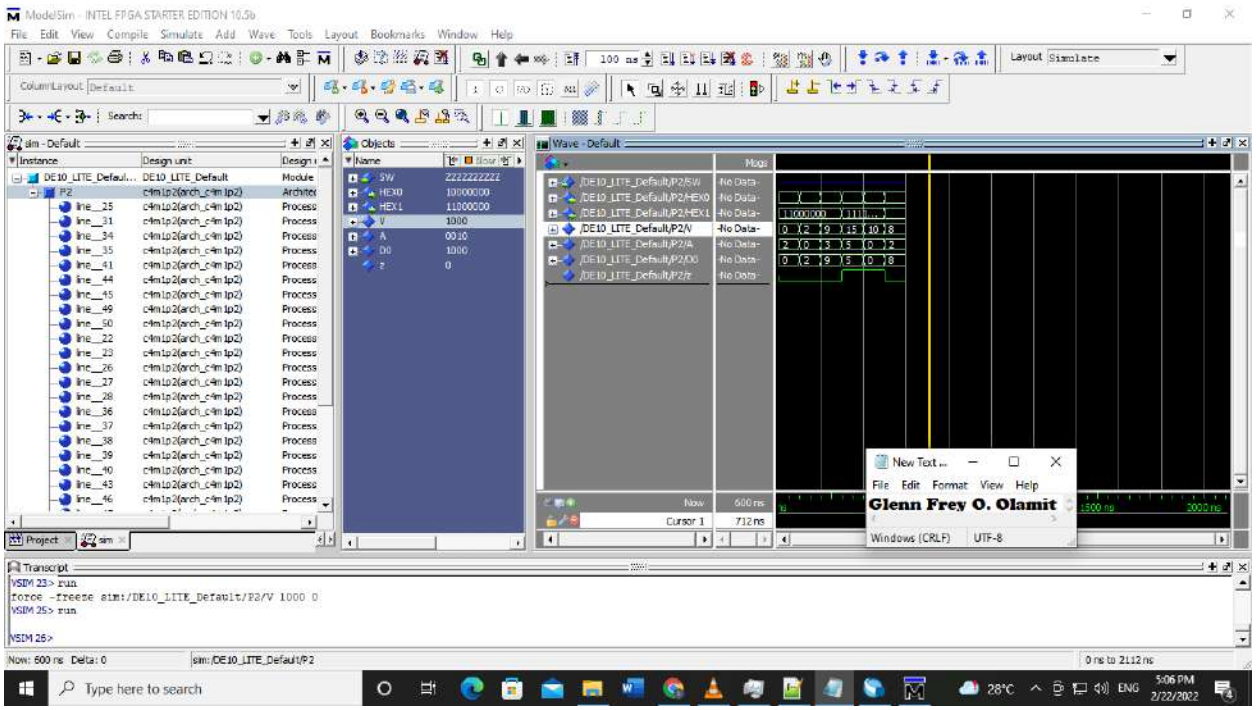
Fitter (Place & Route)
Assembler (Generate programming files)
New Text ...
File Edit Format View Help
Glenn Frey O. Olamit
Windows (CRLF) UTF-8
Find...
Find Next
Type ID Message
Quartus Prime EDA Netlist Writer was successful. 0 errors, 2 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 206 warnings
System
Processing (145)
Type here to search
29°C
ENG
4:34 PM
2/22/2022


ModelSim - INTEL FPGA STARTER EDITION 10.5b
sim - Default
Objects
Wave - Default
New Text ...
File Edit Format View Help
Glenn Frey O. Olamit
Windows (CRLF) UTF-8
Transcript
VSIM 23> run
force -freeze sim:/DE10_LITE_Default/P2/V 1000 0
VSIM 25> run
VSIM 26>
Type here to search
28°C
ENG
5:06 PM
2/22/2022

Results:

Fmax	NA
Logic Utilization %	(<1%)
# Flip-Flops	0
With V = 0, z	0
With V = 0, A	2
With V = F, z	1
With V = F, A	5

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?Yes the board behaves as expected.
2. Does this design use more or less logic than the design in Part 1? Why? Yes because this design is implemented using select statements and boolean logic rather than if-else statements which is easy to code and analyze but is not efficient.

Conclusions: The circuit is quite challenging but I was able to implement BCD using multiplexer, comparator, boolean logic(circuit A) and display using a seven segment decoder.

Lessons Learned (What did you learn?): I learn to implement BCD using multiplexer, comparator, boolean logic(circuit A) and display in a seven segment decoder using boolean logic.

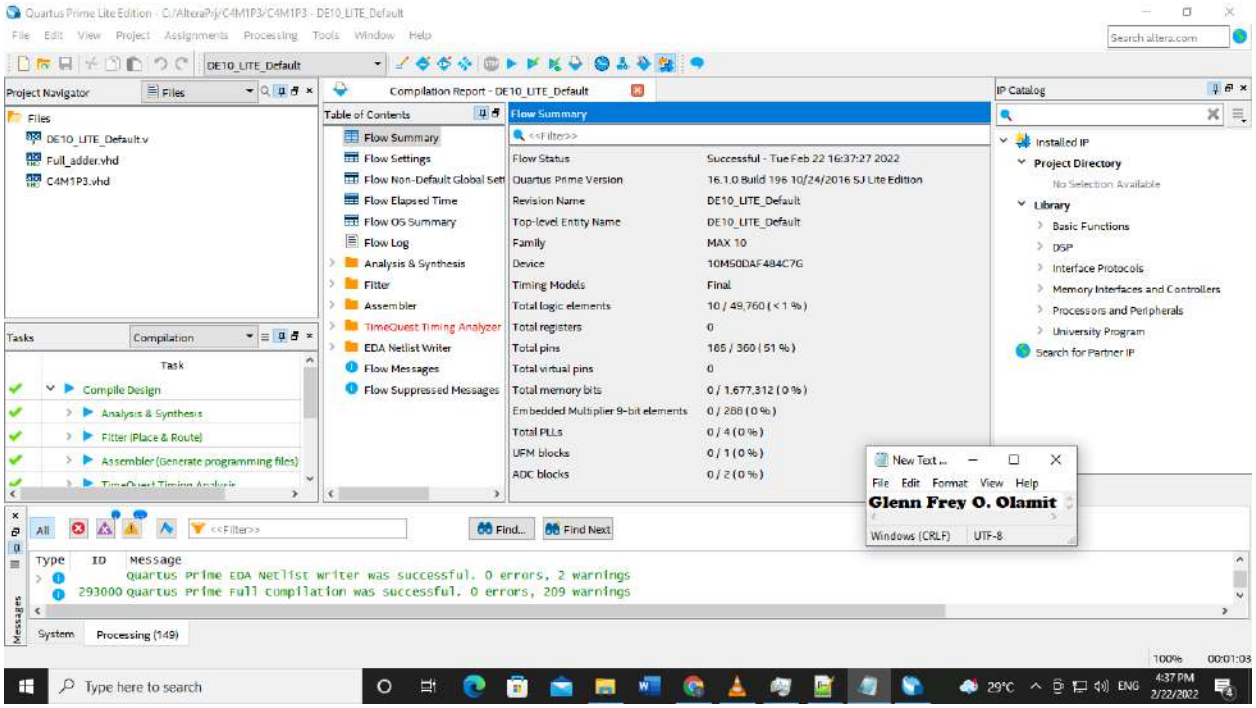
Part 3

Date: February 22, 1990
Procedure/Description of Test:
Write VHDL code to implement a 4-bit ripple carry full adder. Table 1 shows the required output values. A partial design of this circuit is given in Figure 1. It includes a comparator that checks when the value of V is greater than 9, and uses the output of this comparator in the control of the 7-segment displays. You are to complete the design of this circuit. The output z for the comparator circuit can be specified using a single Boolean expression, with the four inputs V3-0. Design this Boolean expression by making a truth table that shows the valuations of the inputs V3-0 for which z has to be 1.

Observations:
The LED 4-0 lights up according to the sum of the binary value of SW 7-4, SW 3-0, and SW 8.

Data:
Fmax, logic utilization, and determining the number of flip-flops

Images/Drawings:


Quartus Prime Lite Edition - C:/AlteraPrj/C4M1P3/C4M1P3 - DE10_LITE_Default
Project Navigator
Files
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Full_adder.vhd
C4M1P3.vhd
Compilation Report - DE10_LITE_Default
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Flow Suppressed Messages
Flow Summary
Flow Status Successful - Tue Feb 22 16:37:27 2022
Quartus Prime Version 16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name DE10_LITE_Default
Top-level Entity Name DE10_LITE_Default
Family MAX 10
Device 10M50DAF484C7G
Timing Models Final
Total logic elements 10 / 49,760 (< 1 %)
Total registers 0
Total pins 185 / 360 (51 %)
Total virtual pins 0
Total memory bits 0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements 0 / 288 (0 %)
Total PLLs 0 / 4 (0 %)
UFM blocks 0 / 1 (0 %)
ADC blocks 0 / 2 (0 %)
IP Catalog
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Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
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Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
New Text ...
File Edit Format View Help
Glenn Frey O. Olamit
Windows (CRLF) UTF-8
Find...
Find Next
Type ID Message
Quartus Prime EDA Netlist Writer was successful. 0 errors, 2 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 209 warnings
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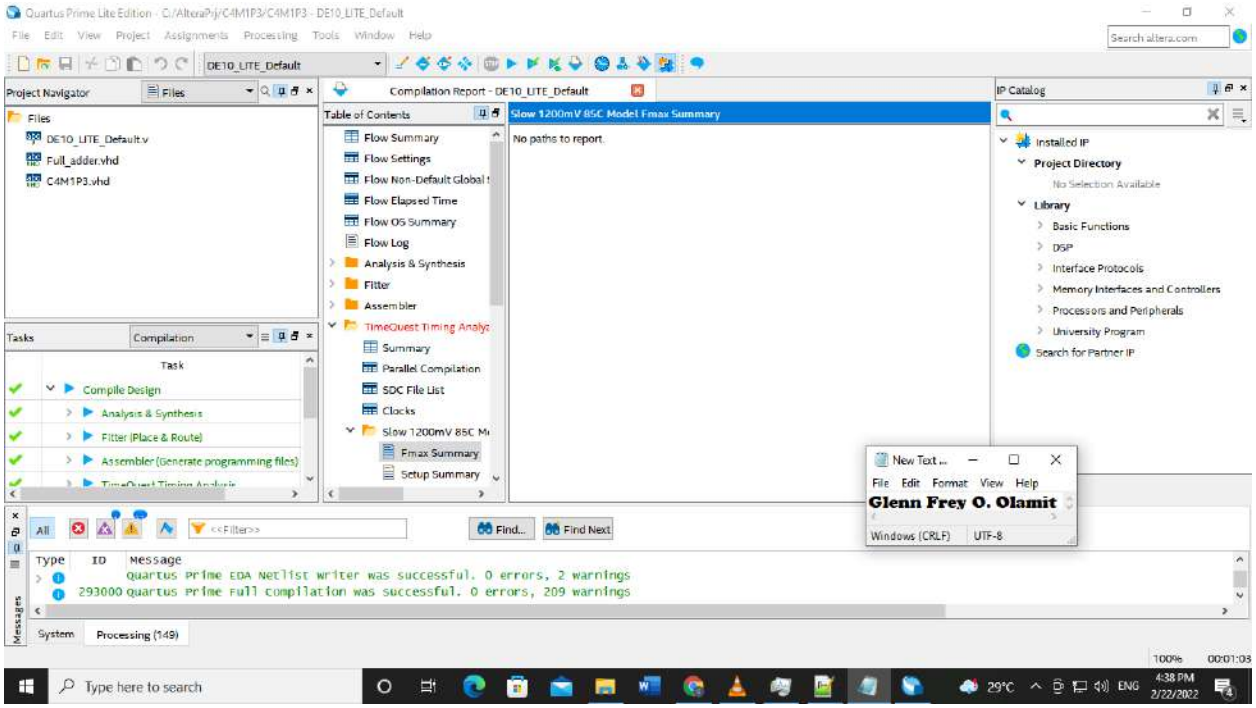
Processing (149)
Type here to search
4:37 PM
2/22/2022


Quartus Prime Lite Edition - C:/AlteraPrj/C4M1P3/C4M1P3 - DE10_LITE_Default
Project Navigator
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Full_adder.vhd
C4M1P3.vhd
Compilation Report - DE10_LITE_Default
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Slow 1200mV 85C Model Fmax Summary
No paths to report.
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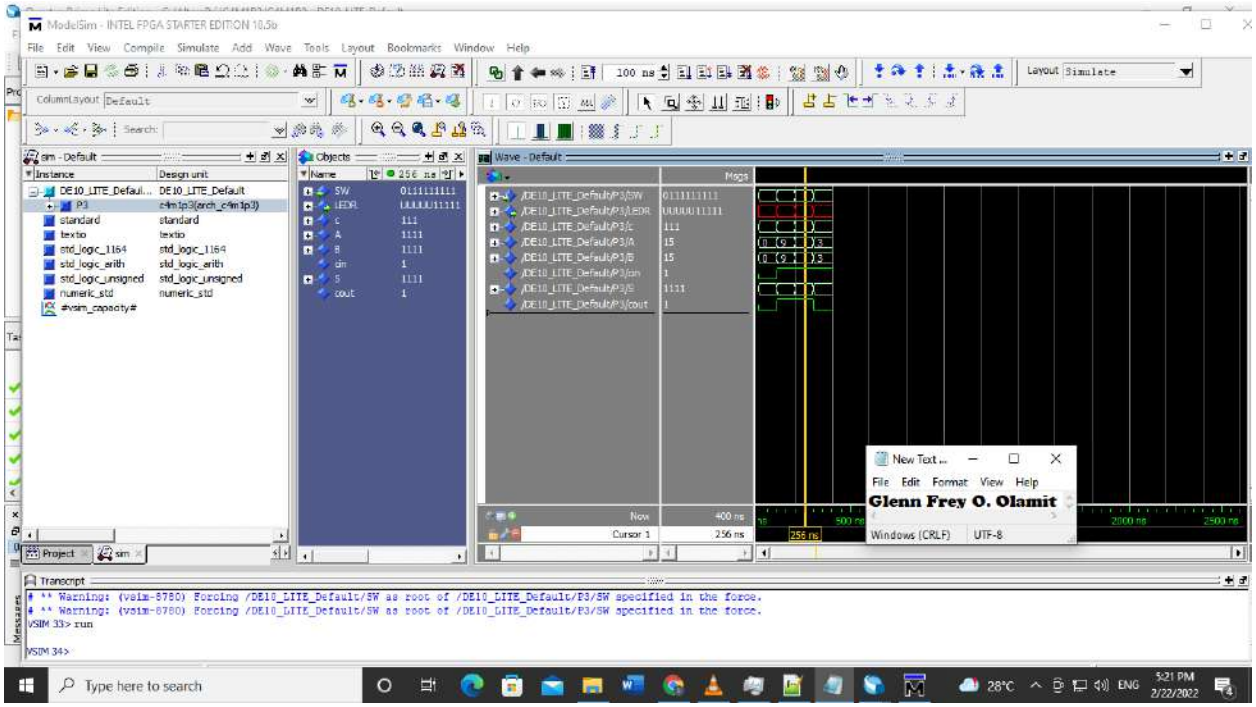
Fitter (Place & Route)
Assembler (Generate programming files)
New Text ...
File Edit Format View Help
Glenn Frey O. Olamit
Windows (CRLF) UTF-8
Find...
Find Next
Type ID Message
Quartus Prime EDA Netlist Writer was successful. 0 errors, 2 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 209 warnings
System
Processing (149)
Type here to search
4:38 PM
2/22/2022


ModelSim - INTEL FPGA STARTER EDITION 10.5b
Glenn Frey O. Olamit
** Warning: (vsim-8780) Forcing /DE10_LITE_Default/SW as root of /DE10_LITE_Default/P3/SW specified in the force.
** Warning: (vsim-8780) Forcing /DE10_LITE_Default/SW as root of /DE10_LITE_Default/P3/SW specified in the force.
VSIM 33> run
VSIM 34>
Type here to search


Download DE10-Lite CD
http://de10-lite.terasic.com/cd
DE10-Lite

Results:

Fmax	NA
Logic Utilization %	(<1%)
#Flip-Flops	0

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect? Yes the board behaves as expected.

Conclusions: The circuit has no flip-flops. The Four bit ripple carry adder can be implemented by instantiating four full adders in the vhdl code.

Lessons Learned (What did you learn?): I learned to design a Four bit ripple carry adder using four full adders in DE10-Lite.

Part 4

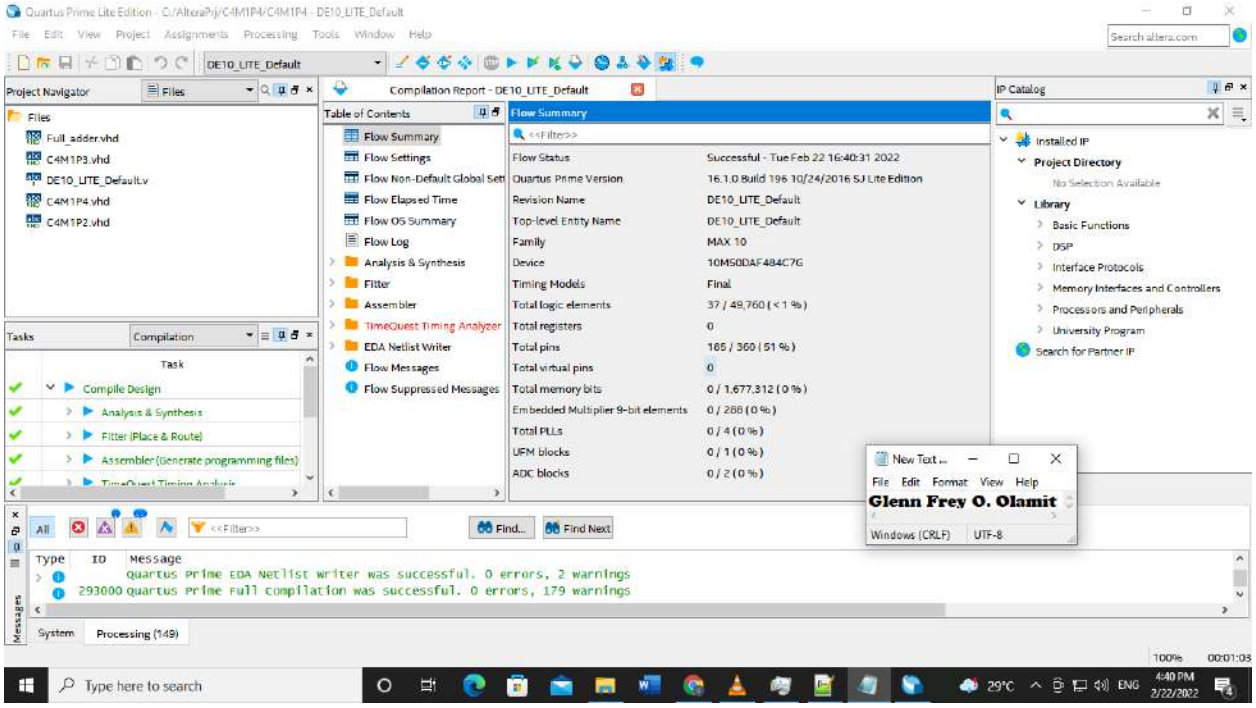
Date: February 22, 2022
Procedure/Description of Test:
You are to design a circuit that adds the two BCD digits. The inputs to your circuit are the numbers X and Y, plus a carry-in, cin. When these inputs are added, the result will be a 5-bit binary number. But this result is to be displayed on 7-segment displays as a two-digit BCD sum S1S0. For a sum equal to zero you would display S1S0 = 00, for a sum of one S1S0 = 01, for

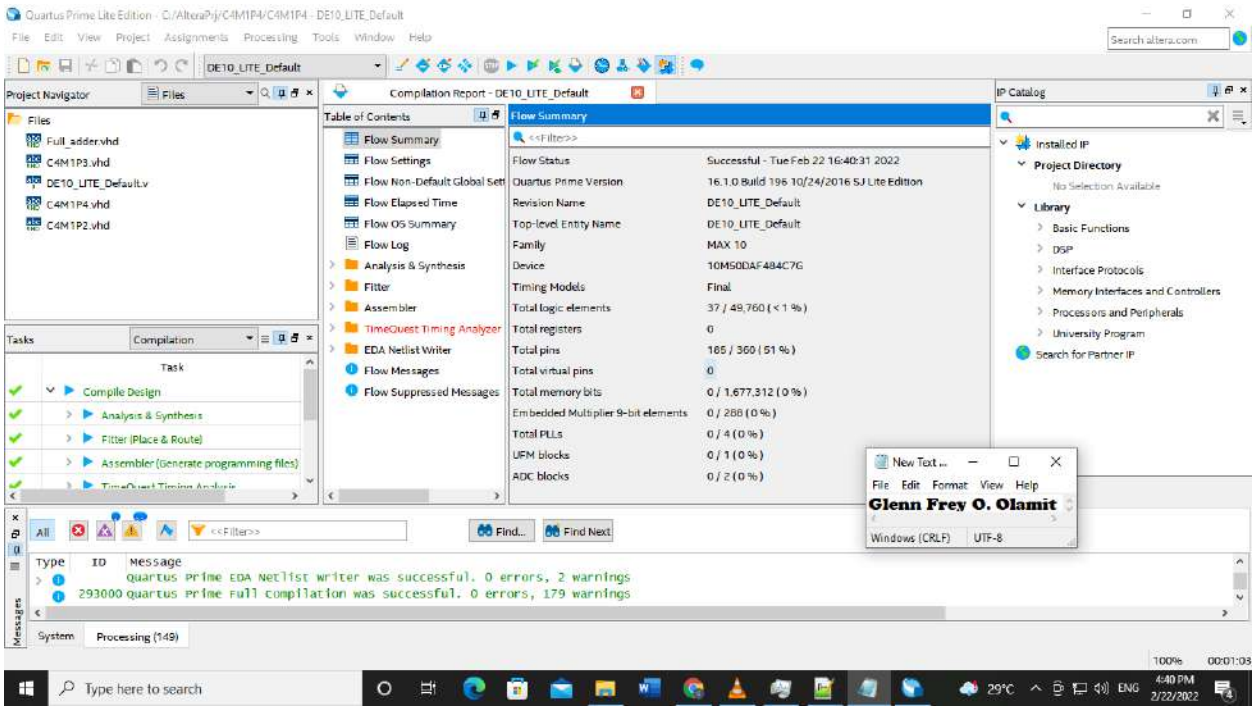
nine S1S0 = 09, for ten S1S0 = 10, and so on. Note that the inputs X and Y are assumed to be decimal digits, which means that the largest sum that needs to be handled by this circuit is S1S0 = 9 + 9 + 1 = 19.

Observations:
7-segment display for both operands and sum works as expected. The design is challenging but it connects all that I learned from the previous projects.

Data:
logic cells and logic utilization.

Images/Drawings:




Quartus Prime Lite Edition - C:/AlteraPrj/C4M1P4/C4M1P4 - DE10_LITE_Default
Project Navigator
Files
Full_adder.vhd
C4M1P3.vhd
DE10_LITE_Default.v
C4M1P4.vhd
C4M1P2.vhd
Compilation Report - DE10_LITE_Default
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Flow OS Summary
Flow Log
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Assembler
TimeQuest Timing Analyzer
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Flow Status Successful - Tue Feb 22 16:40:31 2022
Quartus Prime Version 16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name DE10_LITE_Default
Top-level Entity Name DE10_LITE_Default
Family MAX 10
Device 10M50DAF484C7G
Timing Models Final
Total logic elements 37 / 49,760 (< 1 %)
Total registers 0
Total pins 185 / 360 (51 %)
Total virtual pins 0
Total memory bits 0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements 0 / 288 (0 %)
Total PLLs 0 / 4 (0 %)
UFM blocks 0 / 1 (0 %)
ADC blocks 0 / 2 (0 %)
IP Catalog
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New Text ...
Glenn Frey O. Olamit
Windows (CRLF) UTF-8
Find...
Find Next
Type ID Message
Quartus Prime EDA Netlist Writer was successful. 0 errors, 2 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 179 warnings
System
Processing (149)
Type here to search
29°C
ENG
4:40 PM
2/22/2022


Download DE10-Lite CD
http://de10-lite.terasic.com/cd
terasIC
DE10-Lite

Results:

# Logic Cells	37
Logic Utilization %	<1%

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?Yes, the board behaves as expected.

Conclusions:

I was able to design a circuit that performs two decimal digits and display the sum and its value. Previous Projects were utilized.

Lessons Learned (What did you learn?):

I learned to design a circuit that performs two decimal digits and displays the sum and its value in a seven segment display in DE10-Lite. I learned to connect multiple vhdl files together.

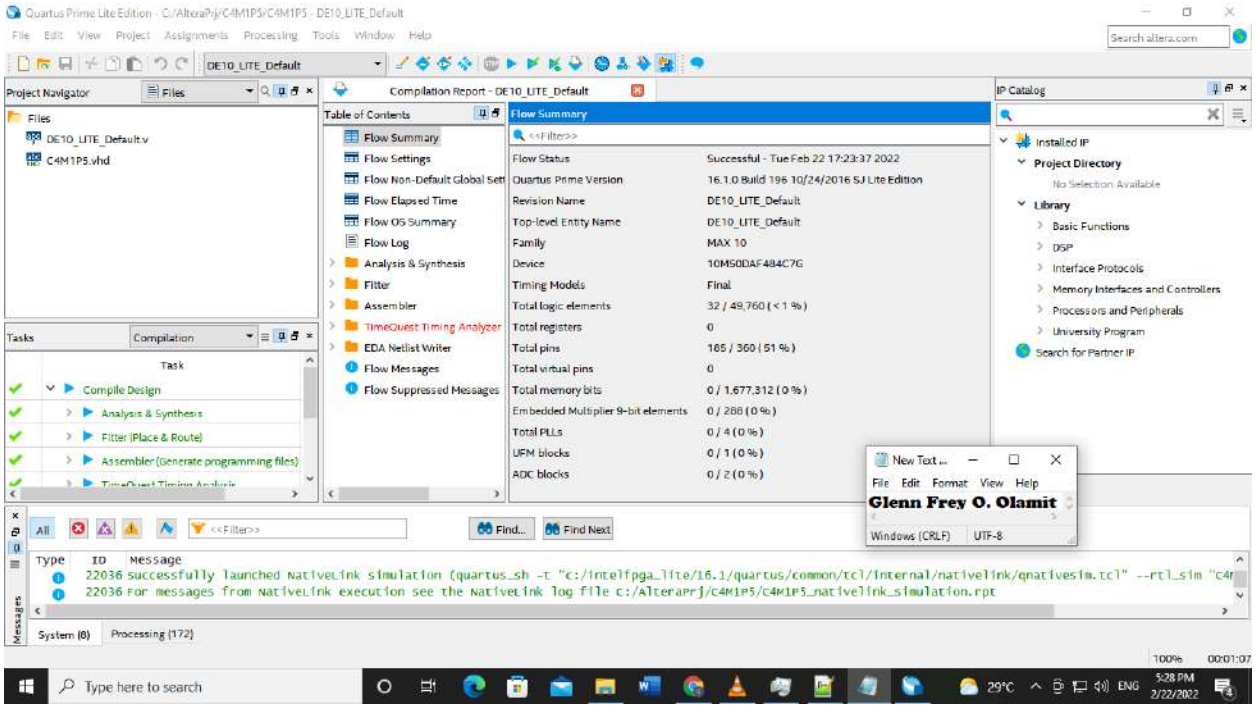
Part 5

Date: February 22, 2022
Procedure/Description of Test:
In Part IV you created VHDL code for a BCD adder. A different approach for describing the adder in VHDL code is to specify an algorithm like the one represented by the following pseudo-code: 1 T0 = A + B + c0 2 if (T0 > 9) then 3 Z0 = 10; 4 c1 = 1; 5 else 6 Z0 = 0; 7 c1 = 0; 8 end if 9 S0 = T0 - Z0 10 S1 = c1 It is reasonably straightforward to see what circuit could be used to implement this pseudo-code. Lines 1 and 9 represent adders, lines 2-8 correspond to multiplexers, and testing for the condition T0 > 9 requires comparators. You are to write VHDL code that corresponds to this pseudo-code. Note that you can perform addition operations in your VHDL code instead of the subtraction shown in line 9. The intent of this part of the exercise is to examine the effects of relying more on the VHDL compiler to design the circuit by using IF-ELSE statements along with the VHDL > and + operators.

Observations:
The code is simple and easy to design. The end result is the same circuit and function as Part 4.

Data:
number of logic cells and percent utilization of logic

Images/Drawings:


Quartus Prime Lite Edition - C:/AlteraPrj/C4M1P5/C4M1P5 - DE10_LITE_Default
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EDA Netlist Writer
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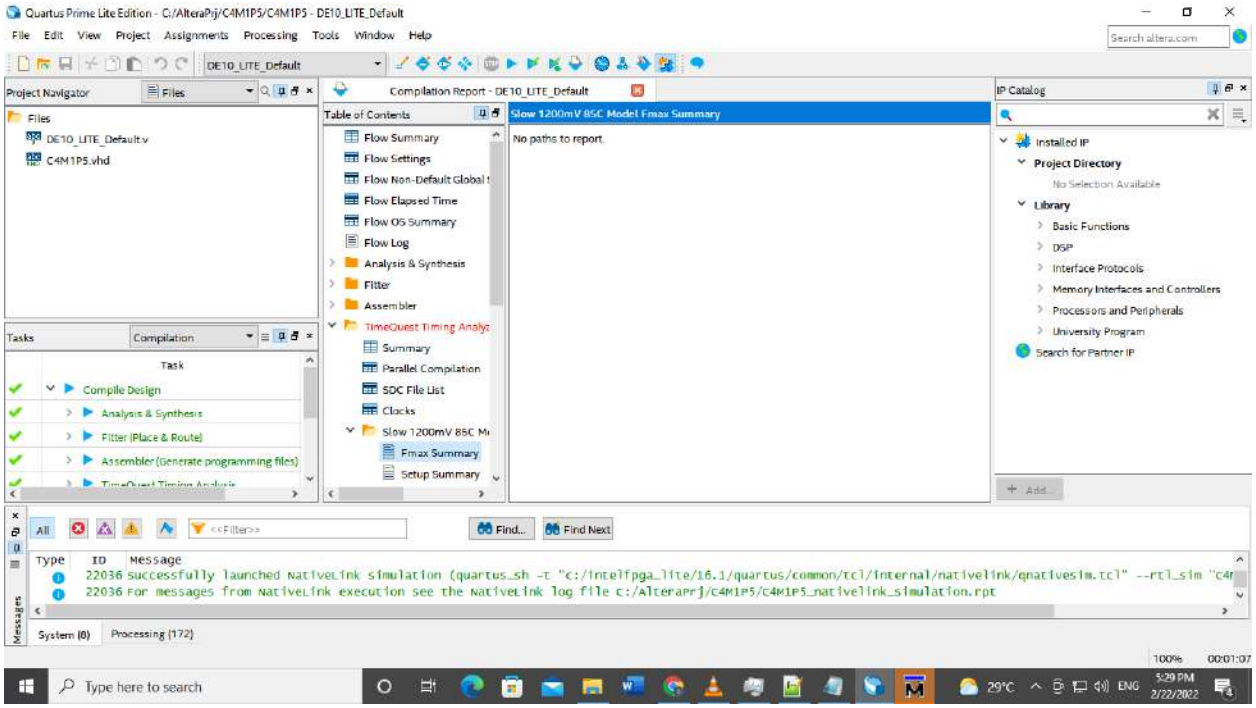
Flow Suppressed Messages
Flow Summary
Flow Status Successful - Tue Feb 22 17:23:37 2022
Quartus Prime Version 16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name DE10_LITE_Default
Top-level Entity Name DE10_LITE_Default
Family MAX 10
Device 10M50DAF484C7G
Timing Models Final
Total logic elements 32 / 49,760 (< 1 %)
Total registers 0
Total pins 185 / 360 (51 %)
Total virtual pins 0
Total memory bits 0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements 0 / 288 (0 %)
Total PLLs 0 / 4 (0 %)
UFM blocks 0 / 1 (0 %)
ADC blocks 0 / 2 (0 %)
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
New Text ...
File Edit Format View Help
Glenn Frey O. Olamit
Windows (CRLF) UTF-8
Find... Find Next
Type ID Message
22036 Successfully launched NativeLink simulation (quartus_sh -t "c:/intelfpga_lite/16.1/quartus/common/tcl/internal/nativelink/qnativesim.tcl" --rtl_sim "C4
22036 For messages from NativeLink execution see the NativeLink log file c:/AlteraPrj/C4M1P5/C4M1P5_nativelink_simulation.rpt
System (0) Processing (172)
100% 00:01:07
Type here to search
29°C ENG 5:28 PM 2/22/2022


Quartus Prime Lite Edition - C:/AlteraPrj/C4M1P5/C4M1P5 - DE10_LITE_Default
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
DE10_LITE_Default
Project Navigator
Files
DE10_LITE_Default.v
C4M1P5.vhd
Compilation Report - DE10_LITE_Default
Table of Contents
Slow 1200mV 85C Model Fmax Summary
No paths to report.
Flow Summary
Flow Settings
Flow Non-Default Global
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
TimeQuest Timing Analyz
Summary
Parallel Compilation
SDC File List
Clocks
Slow 1200mV 85C M
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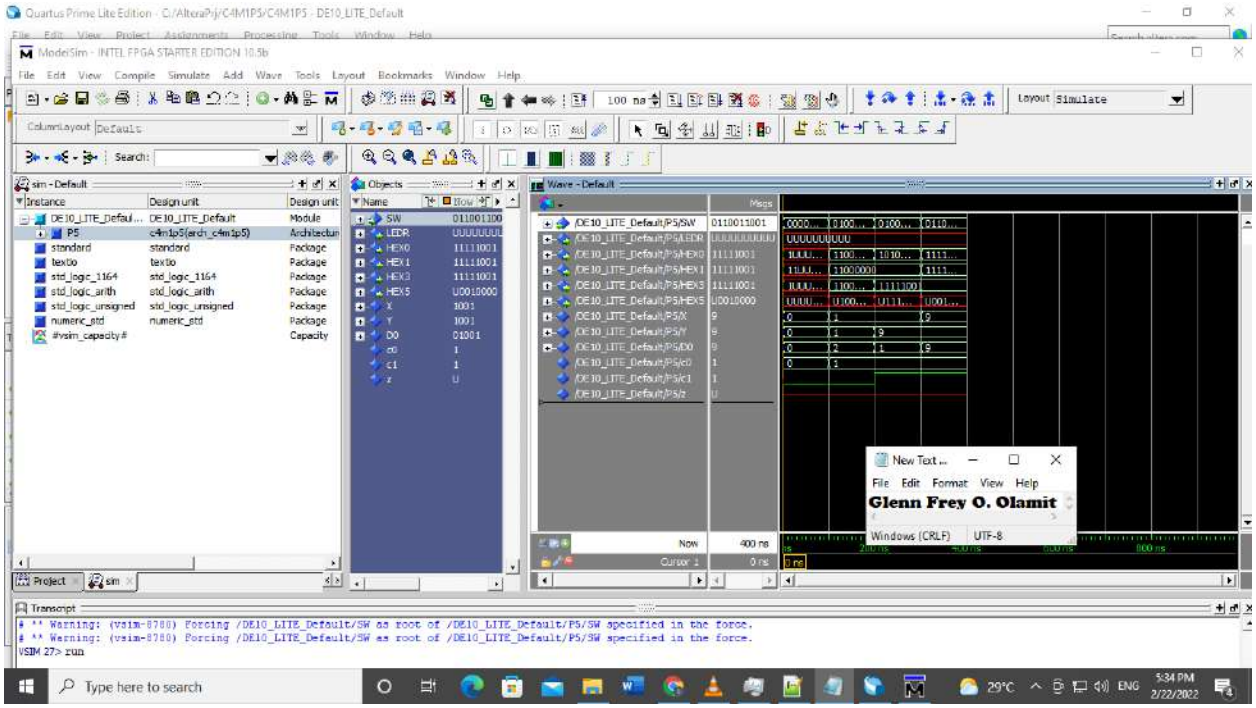
Assembler (Generate programming files)
Find... Find Next
Type ID Message
22036 Successfully launched NativeLink simulation (quartus_sh -t "c:/intelfpga_lite/16.1/quartus/common/tcl/internal/nativelink/qnativesim.tcl" --rtl_sim "C4
22036 For messages from NativeLink execution see the NativeLink log file c:/AlteraPrj/C4M1P5/C4M1P5_nativelink_simulation.rpt
System (0) Processing (172)
100% 00:01:07
Type here to search
29°C ENG 5:29 PM 2/22/2022


Quartus Prime Lite Edition - C:/AlteraPrj/C4M1P5/C4M1P5 - DE10_LITE_Default
ModelSim - INTEL FPGA STARTER EDITION 10.5b
Glenn Frey O. Olamit
** Warning: (vsim-8780) Forcing /DE10_LITE_Default/SW as root of /DE10_LITE_Default/P5/SW specified in the force.
** Warning: (vsim-8780) Forcing /DE10_LITE_Default/SW as root of /DE10_LITE_Default/P5/SW specified in the force.
VSIM 27> run
Type here to search


Download DE10-Lite CD
http://de10-lite.terasic.com/cd
terasIC
DE10-Lite

Results:

# Logic Cells	32
Logic Utilization %	<1%
#Flip-Flops	0

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?Yes, the board behaves as expected.
2. How does this compare to the number of Logic Cells in Part 4? The same number of logic cells compared to Part 4.

Conclusions: Vhdl compiler is highly optimized in utilizing logic cells.

Lessons Learned (What did you learn?): I learned that the Vhdl compiler is highly optimized in utilizing logic cells.

Module 2

PWM

Author:
Date:
Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
% Logic Utilization	
Total registers	

Questions:

1. Did the LED change brightness depending on the setting of the first 3 switches?

Conclusions:

Lessons Learned (What did you learn?):

ADC

Author:
Date:
Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
%Logic Utilization	

Questions:

1. Does the board behave as you expected?

2. Is this a good voltmeter as is?

3. What could you change in either the board hardware or FPGA logic to make it perform better?

Conclusions:

Lessons Learned (What did you learn?):

Module 3

NIOS II Hardware Design

Author:
Date:
Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
Logic Utilization	

Questions:

1. What is the purpose of the Avalon Memory-Mapped Clock-Crossing Bridge?

Conclusions:

Lessons Learned (What did you learn?):

Module 4

NIOS II Software Design and System Test

Author:
Date:
Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
Logic Utilization	

Questions:

1. Is the control of the 10 LEDs implemented in hardware or in software?
2. Is the control of the 7-segment LEDs done by hardware or by software?
3. How much memory is required to run your Nios II program? Can you fit it into the onchip RAM if you redesign the onchip RAM block?
4. Your Nios II processor is running at what clock speed? How much faster can it run in your MAX10 design?

Conclusions:

Lessons Learned (What did you learn?):