Lab Notebook

FPGA Capstone Project

Academic Integrity

By signing below you acknowledge the CU Honor Code, "On my honor, as a University of Colorado Boulder student I have neither given nor received unauthorized assistance" applies to this assignment.

Signed: _Glenn Frey Olamit_____

Module 2

PWM

Author:Glenn Frey Olamit
Date: March 27, 2022
Procedure/Description of Test:

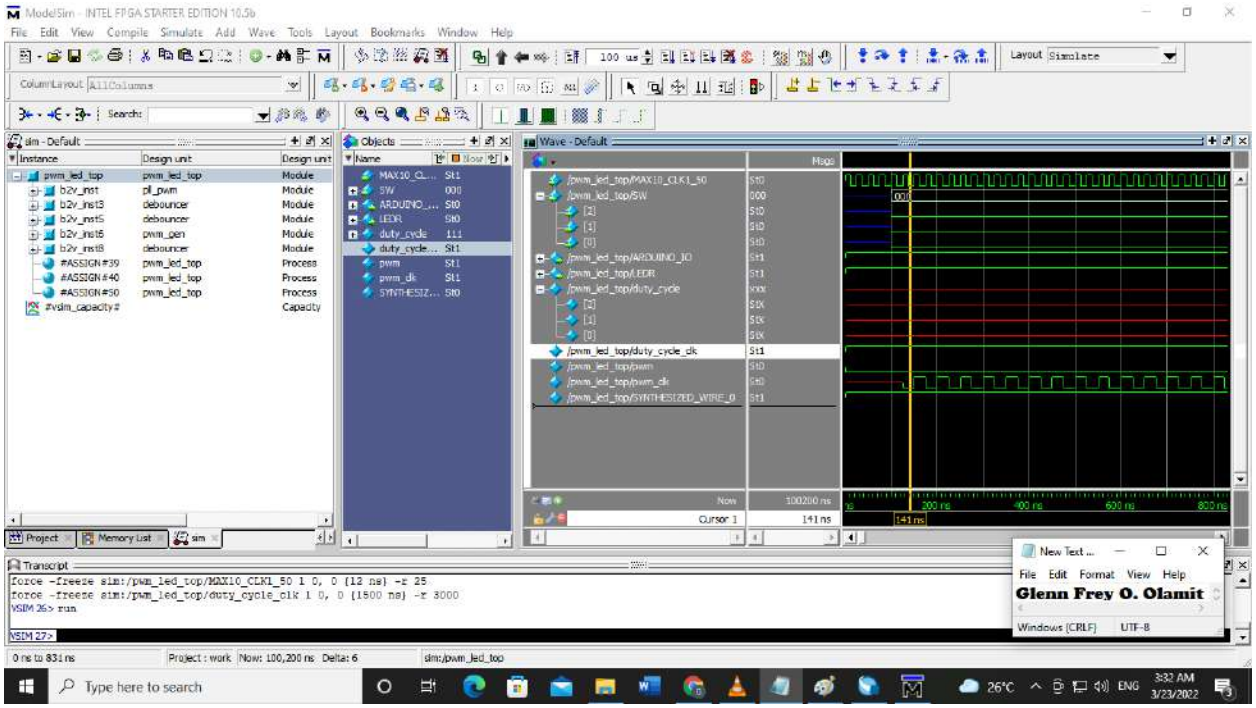
1. Compile design as per instruction, load into MAX10 SRAM.
2. Set different settings with the switches and observe LED

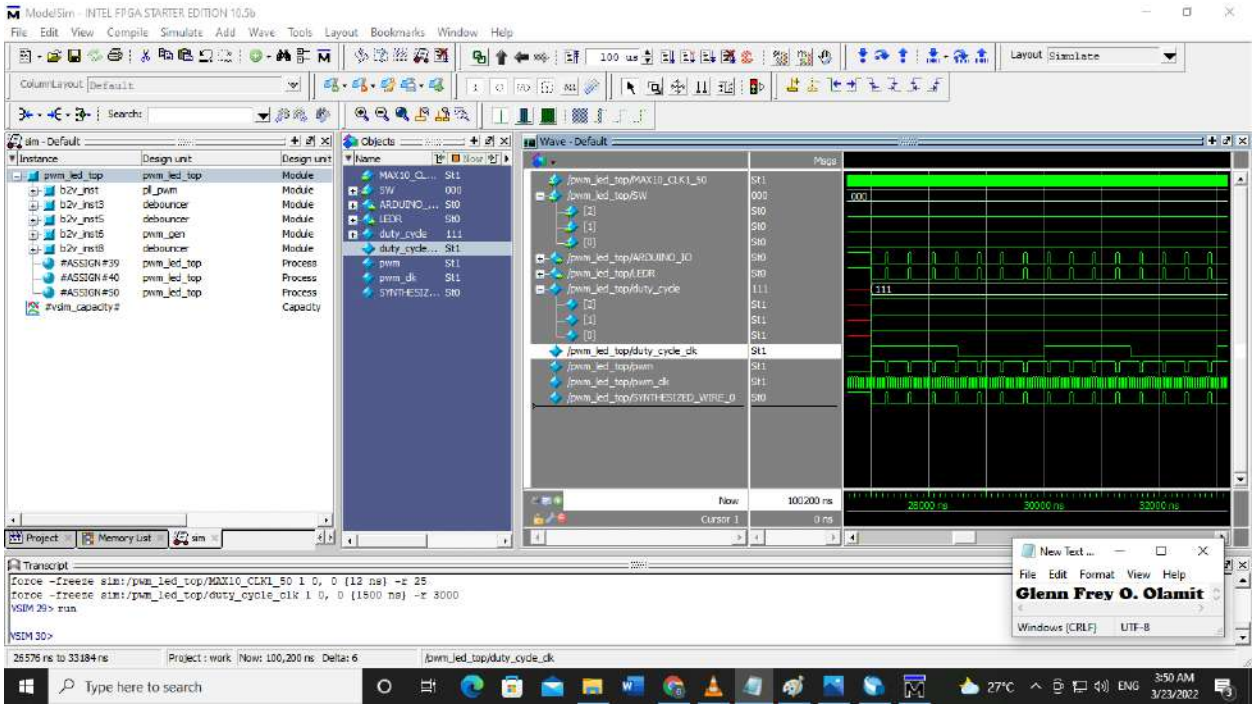
Observations:

The LED increases brightness as I change SW values from 000-111 , but never goes to zero (even if the SW are set to 000).

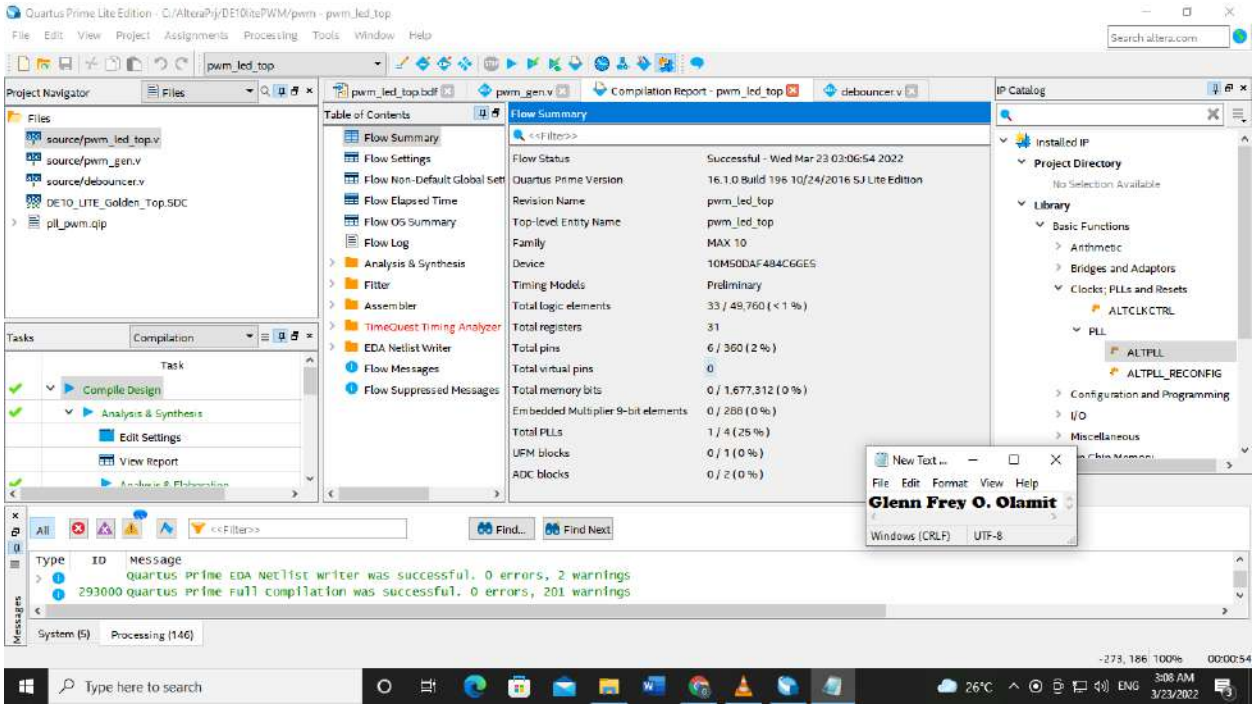
Data:

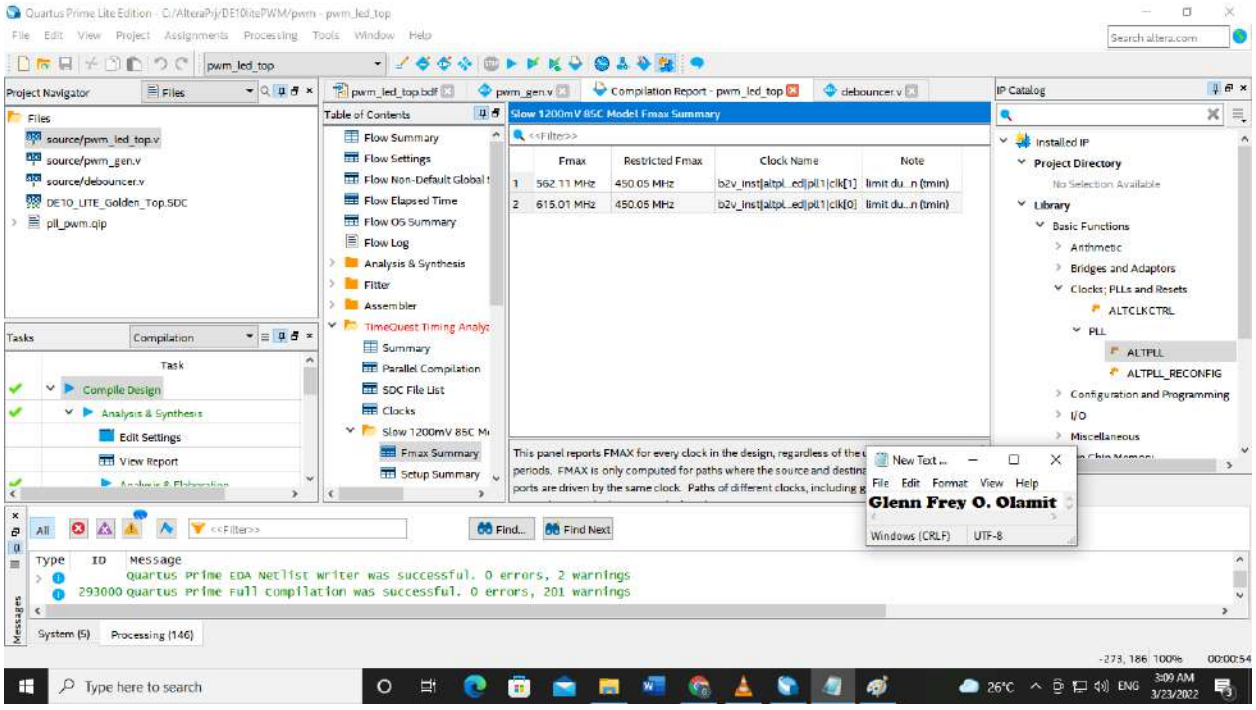
The simulation shows the following result:

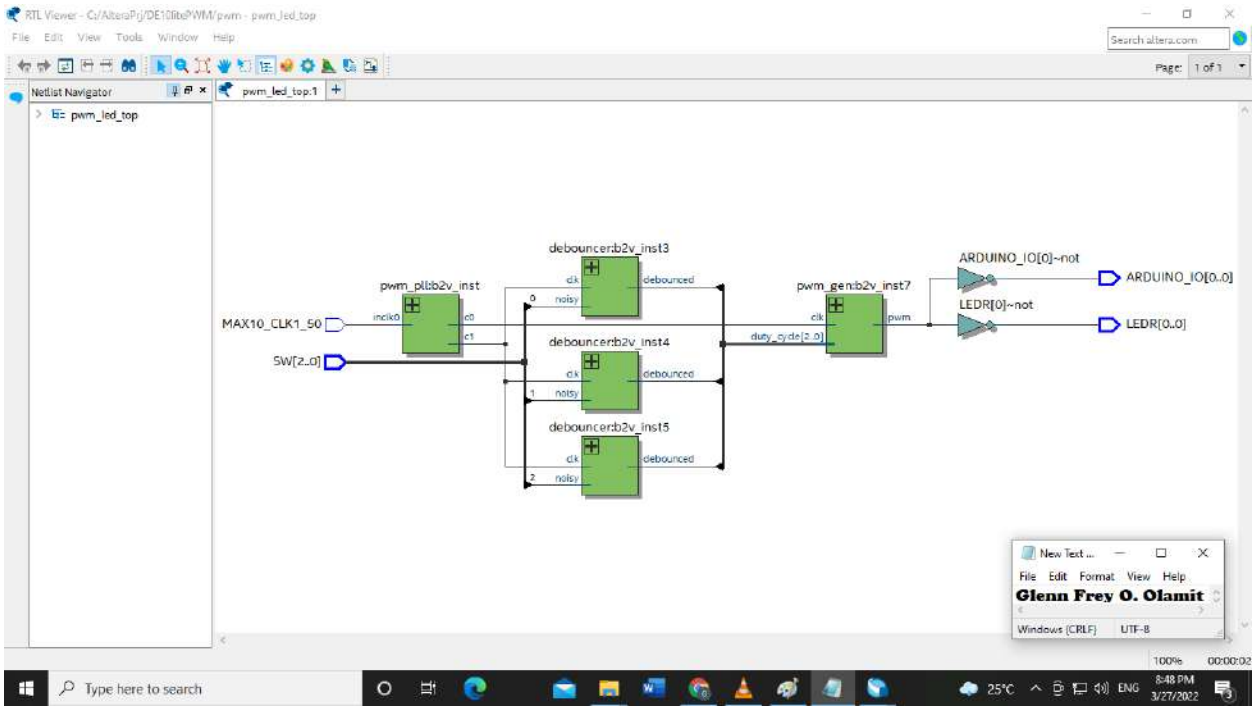

ModelSim - INTEL FPGA STARTER EDITION 10.5b
Glenn Frey O. Olamit
Type here to search


ModelSim - INTEL FPGA STARTER EDITION 10.5b
Glenn Frey O. Olamit
Type here to search

Images/Drawings:







Results:

Fmax	562.11 MHz (clk1) 615.01 MHz (clk0)
% Logic Utilization	<1%
Total registers	31

Questions:

1. Did the LED change brightness depending on the setting of the first 3 switches? Yes! it increases as you change value of switch from 000-111.

Conclusions: The circuit works fine.

Lessons Learned (What did you learn?): I learned how to transfer HDL code into a block diagram and vice versa. A very useful skill. Also I learned how to use PWM control in the FPGA.

ADC

Author: Glenn Frey Olamit
Date: March 28, 2022
Procedure/Description of Test:

3. Compile design as per instruction, load into MAX10 SRAM.
4. Observe Values on 7-segment display
5. Connect Jumper Cable
6. Observe Values on 7-segment display

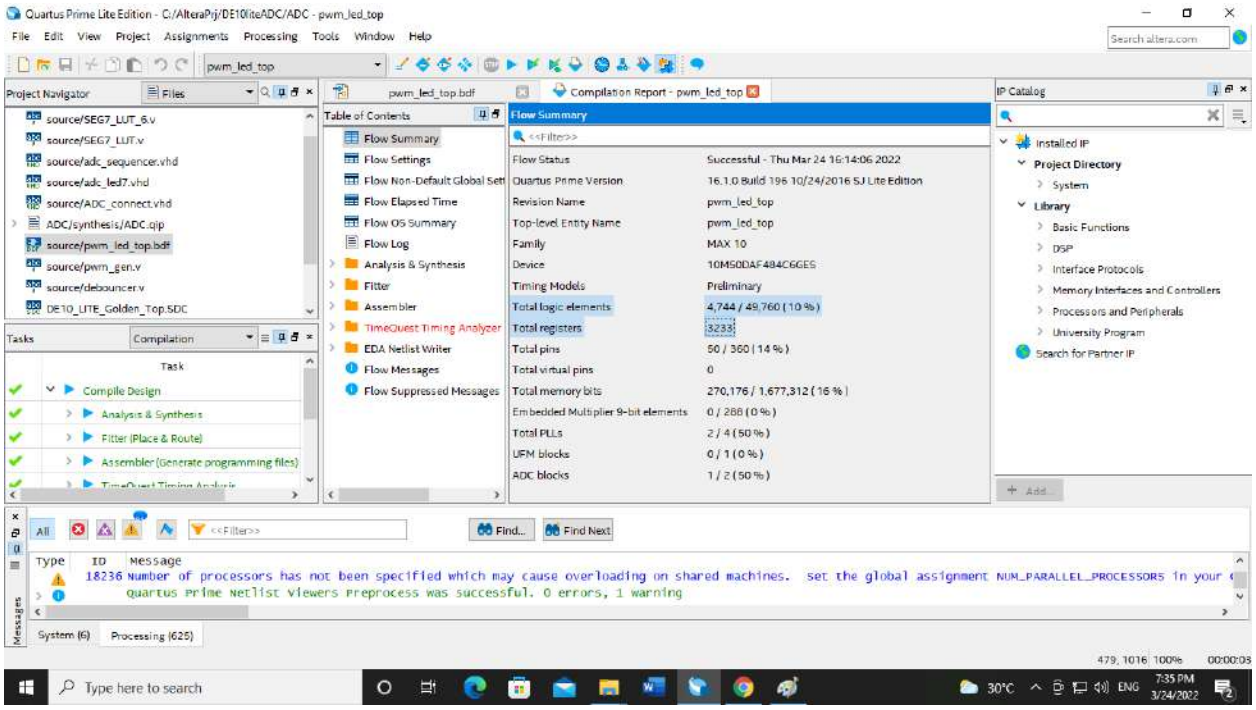
Observations:

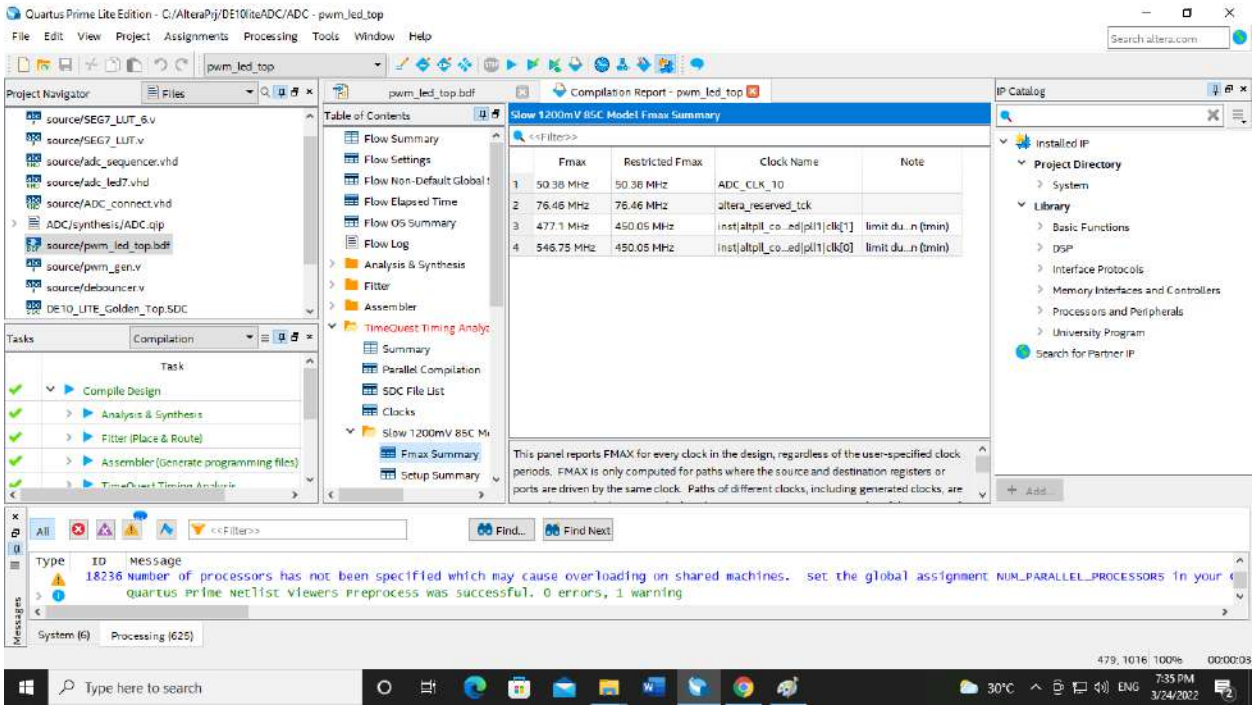
Without the jumper cable, all digits are zero, except the last one is changing very rapidly between 2 and 3 (it's changing so fast, it looks like a 6). With the jumper cable, the value is proportional to the input setting on the SW.

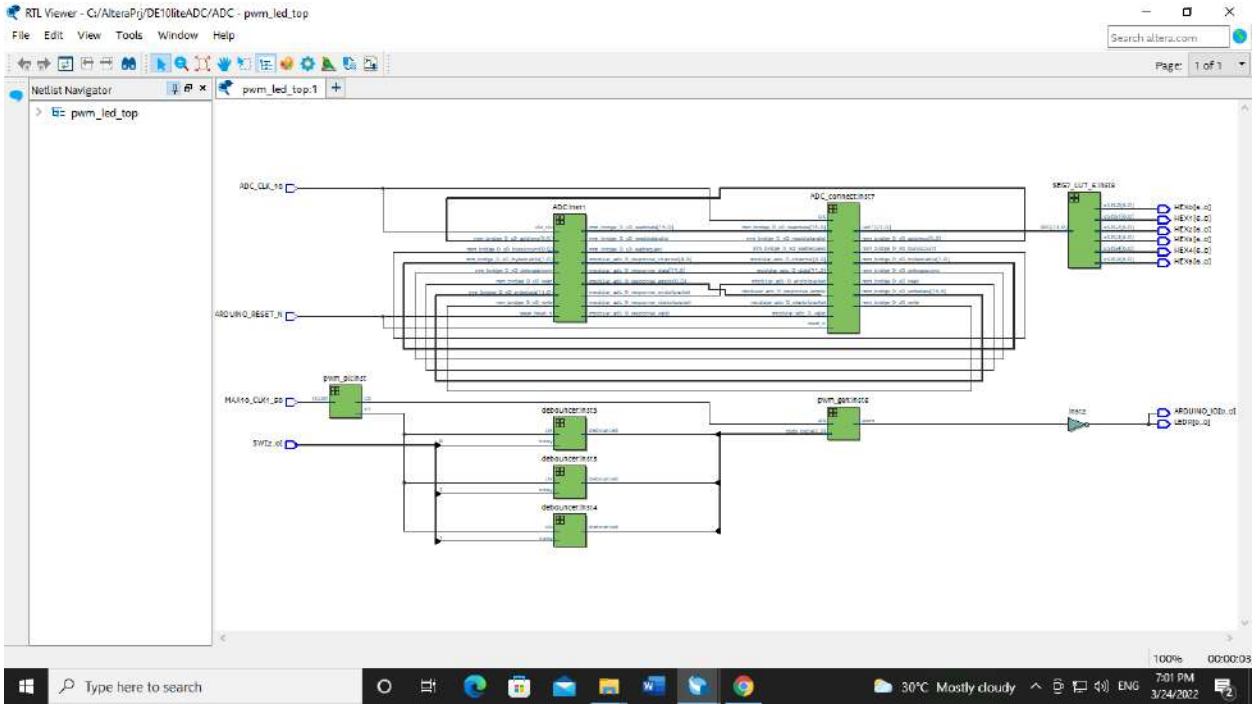
Data:

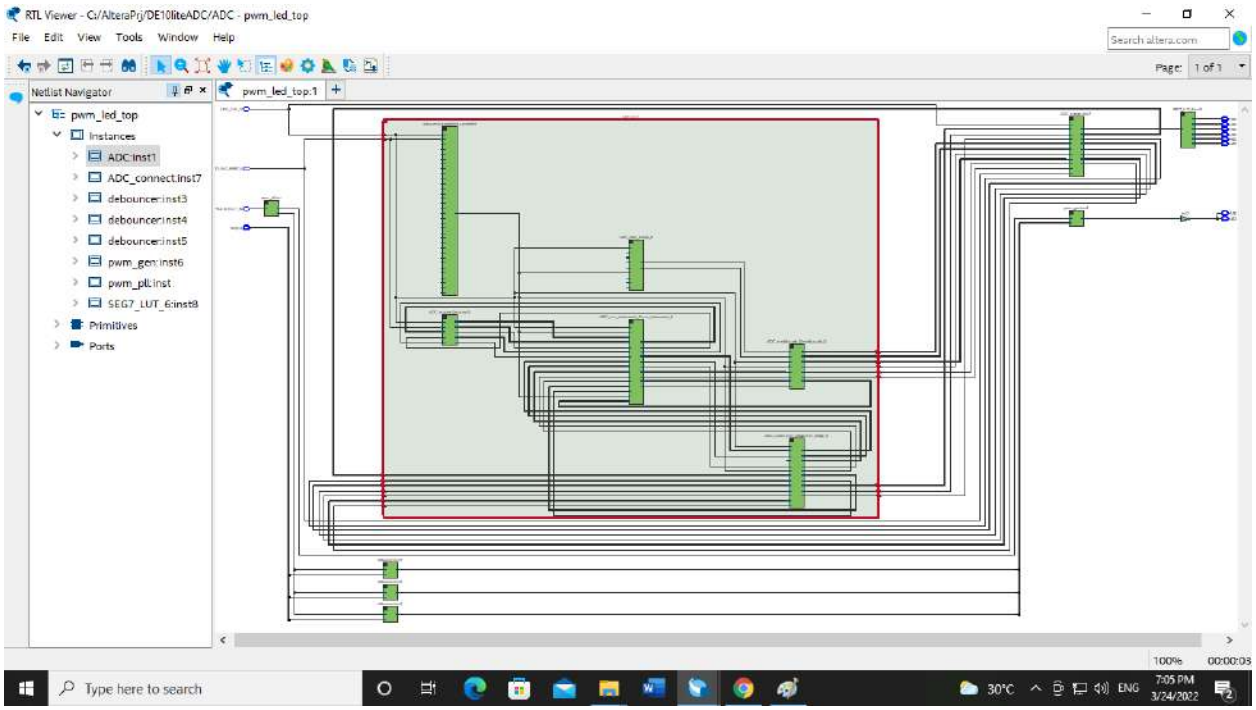
SW setting	Value Measured
000	0x0158
001	0x02A8
010	0x0498
011	0x0558
100	0x0658
101	0x0808
110	0x0968
111	0x0A68

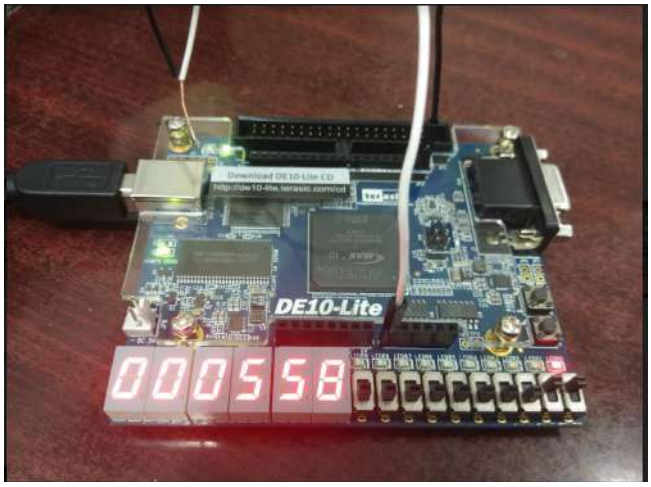
Images/Drawings:






RTL Viewer - C:/AlteraPrj/DE10liteADC/ADC - pwm_led_top
File Edit View Tools Window Help
Netlist Navigator
pwm_led_top
pwm_led_top:1
ADC_CLK_10
ARDUINO_RESET_N
SW[1..0]
Type here to search
30°C Mostly cloudy
ENG
7:01 PM
3/24/2022


RTL Viewer - C:/AlteraPrj/DE10liteADC/ADC - pwm_led_top
File Edit View Tools Window Help
Netlist Navigator
pwm_led_top
Instances
ADC:inst1
ADC_connect:inst7
debouncer:inst3
debouncer:inst4
debouncer:inst5
pwm_gen:inst6
pwm_pll:inst
SEG7_LUT_6:inst8
Primitives
Ports
pwm_led_top:1
Type here to search
30°C
ENG
7:05 PM
3/24/2022



Results:

Fmax	50.38 MHz
%Logic Utilization	10%
Total registers	3233

Questions:

1. Does the board behave as you expected? Yes, the board behaves correctly

2. Is this a good voltmeter as is? Only partly, since the values are changing so fast, they can't be seen, and the units are not in Volt, but in some raw value (0x000 to 0xFFF)

3. What could you change in either the board hardware or FPGA logic to make it perform better? A filter should be added, to reduce the noise in the last digit, and the value should be converted int Volt.

Conclusions:

The System works fine, but could still be improved.

Lessons Learned (What did you learn?):

How to build a system with Qsys. That the system built uses releatively many logic ressources. Hex Display shouldn’t be driven so fast, it makes it unreadable.