Lab Notebook

FPGA Capstone Project

Academic Integrity

By signing below you acknowledge the CU Honor Code, "On my honor, as a University of Colorado Boulder student I have neither given nor received unauthorized assistance" applies to this assignment.

Signed: _Glenn Frey Olamit_____

Module 3

NIOS II Hardware Design

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Date: March 28, 2022
Procedure/Description of Test:

Create a System on a Chip with NIOS II (1) Create QSys design
• Add 2 ALTPLLs with 3 and 1 clock outputs, and an additional clock source.
• Add NIOSII/f processing core. Note: Following instructions on p. 28 of the Project Guide, connected NIOS2 data master signal to pll_slave signals of both PLLs. This is in contradiction with the image on the same page, which shows instruction_master signal playing the same role.
• Add 16 KB RAM.
• Add an on-chip Flash memory.
• Add a memory-mapped clock-crossing bridge.
• Add a PIO Peripheral for LEDs.
• Add a PIO Peripheral for Slide Switches.
• Add an Interval Timer Peripheral.
• Add an SDRAM Controller.
• Add a SPI port for the Accelerometer.
• Add the ADC module. Note: the image on p. 44 of the Project Guide is missing adc_pll_locked connection.
• Add a JTAG to Avalon Master Bridge.
• Add the JTAG UART Peripheral.
• Add a System ID Peripheral.
• Connect IRQ lines.
• Created a common reset network.
• Automatically assign Base Addresses and Interrupt Priorities.

• Changed Reset and Exception Vector assignments for Nios II core.
• Named the exported signals.
• Generated the design.
(2) Use the Qsys design in the Quartus Prime project.
• Added Embed.qip file to the project.
• Instantiated the EEmbed module.
• Performed Analysis and Synthesis.
(3) Place and route the design.
(4) Programmed the DE10-LITE device
(5) Renamed the signals in preparation for the software build.

Observations:

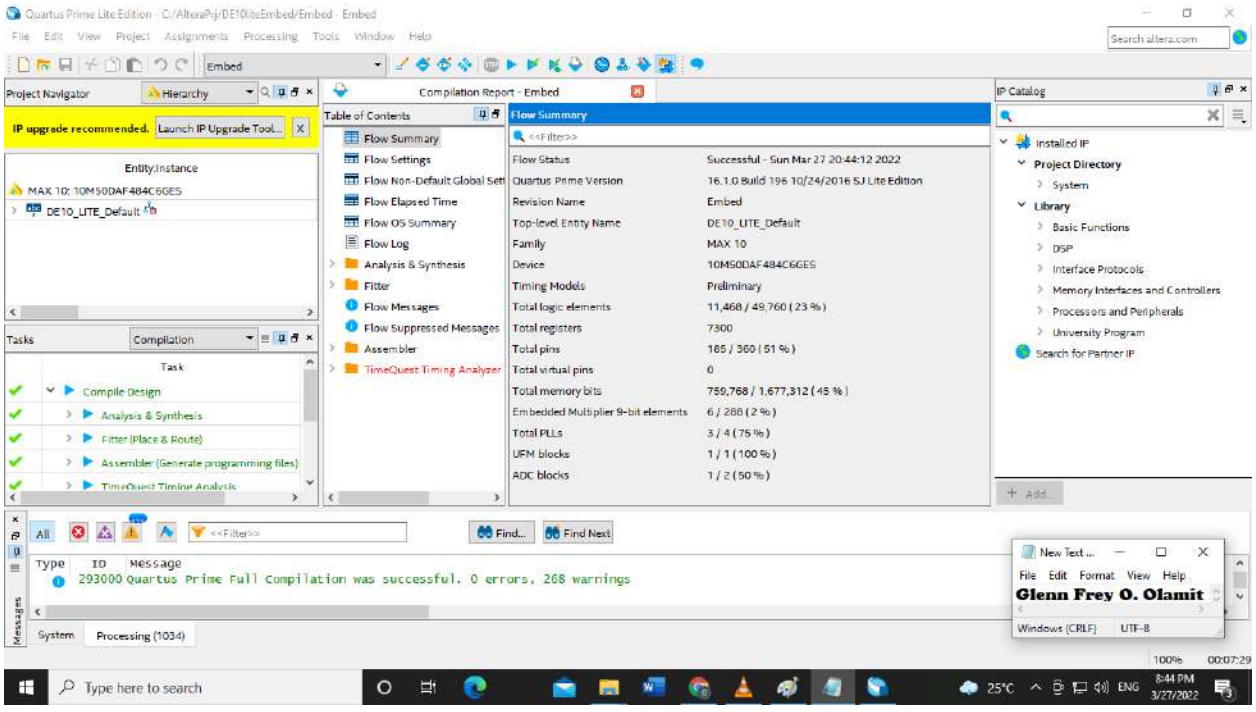
Automatically generated base addresses for Alt PLL 0, Alt PLL 1 are swapped in comparison to the ones presented in the table on p. 49-50 of the Project Guide. So are the base addresses for LED PIO and Slide PIO.

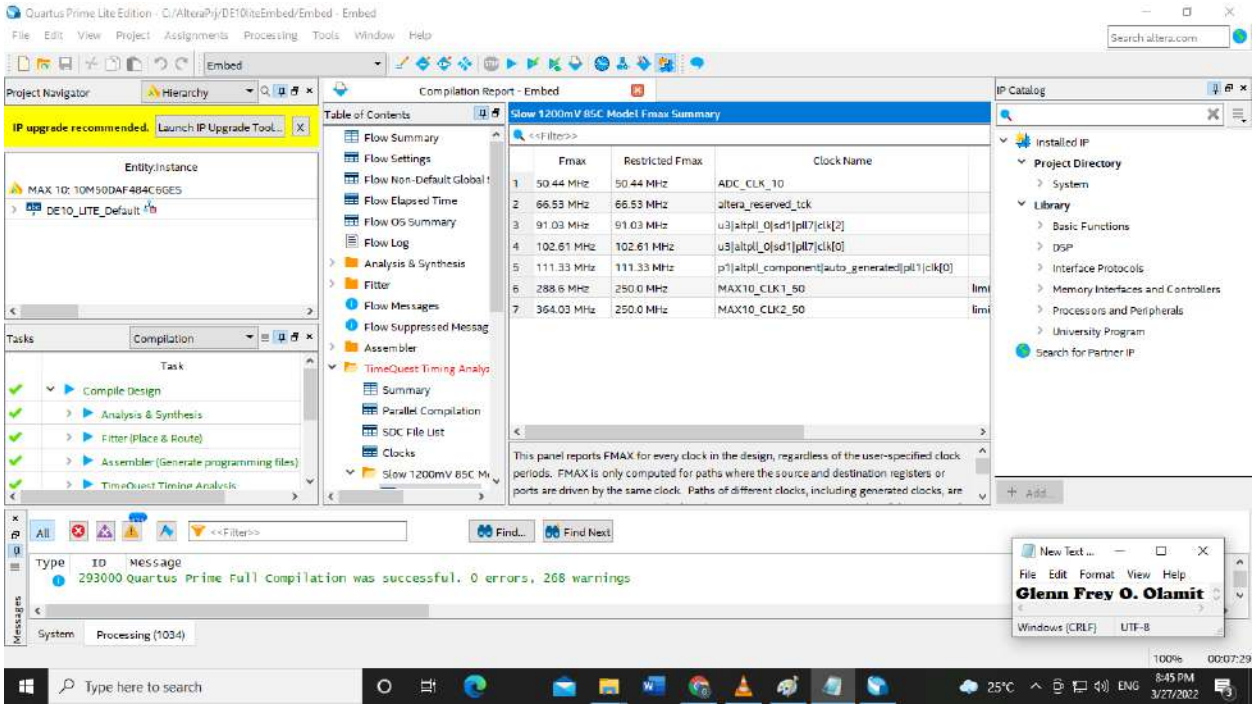
This difference is probably not essential. Automatically generated interrupt priorities differ from the ones manually selected on p. 20, item 20-2. As there is no software loaded into th Nios II processor core, the board functionality is limited.

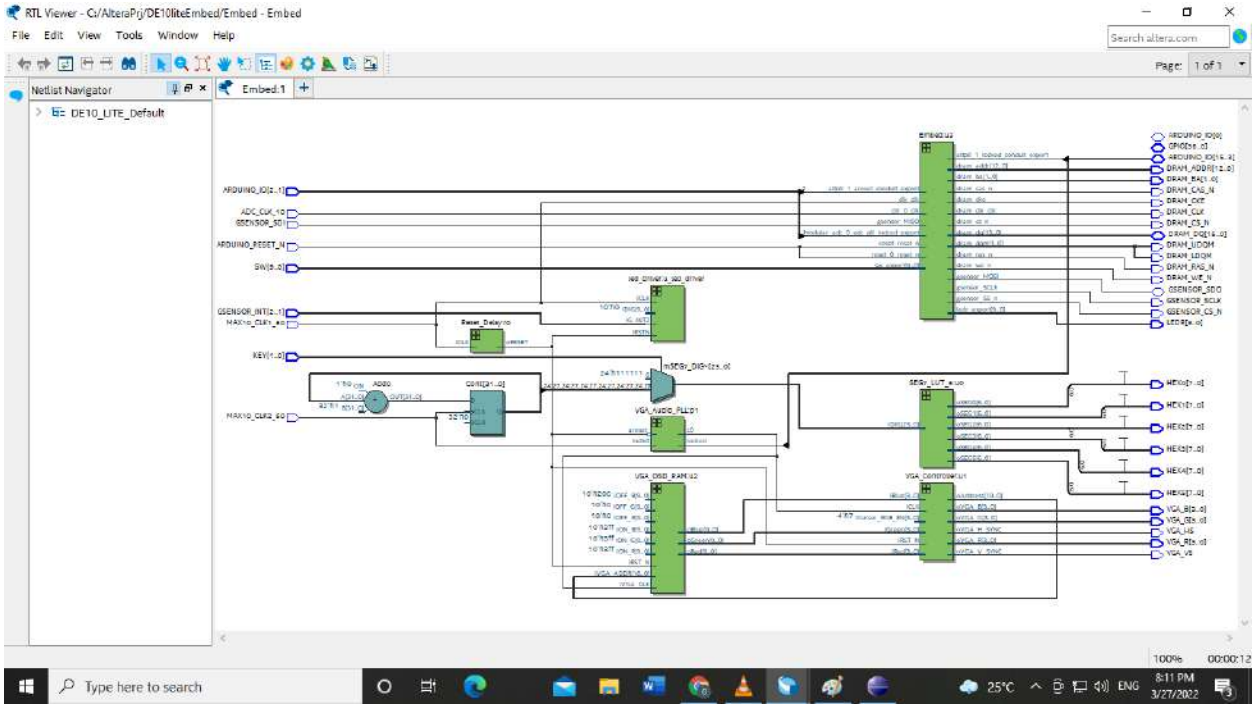
The only observable activity is the 0-F cycling of the 7-segment indicators. This probably remained from the default design configuration, as the Embed design does not drive the 7-segment indicators.

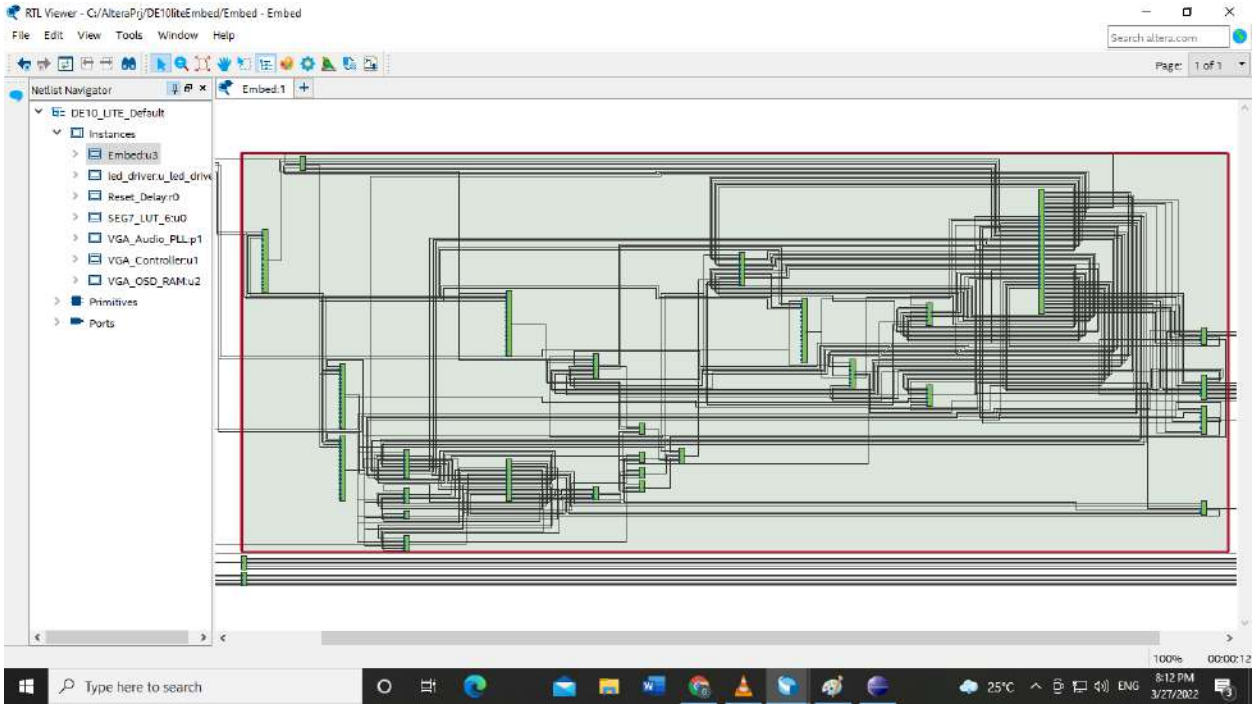
Data:

Images/Drawings:




Quartus Prime Lite Edition - C:/AlteraPrj/DE10liteEmbed/Embed - Embed
Compilation Report - Embed
Slow 1200mV 85C Model Fmax Summary
Fmax
Restricted Fmax
Clock Name
50.44 MHz
ADC_CLK_10
66.53 MHz
altera_reserved_tck
91.03 MHz
102.61 MHz
111.33 MHz
288.6 MHz
MAX10_CLK1_50
364.03 MHz
MAX10_CLK2_50
293000 Quartus Prime Full Compilation was successful. 0 errors, 268 warnings
Glenn Frey O. Olamit
Type here to search


RTL Viewer - C:/AlteraPrj/DE10liteEmbed/Embed - Embed
Netlist Navigator
DE10_LITE_Default
Type here to search



Results:

Fmax	50.44 Mhz
Logic Utilization	23%
Total registers	7300

Questions:

1. What is the purpose of the Avalon Memory-Mapped Clock-Crossing Bridge?

To move the data between fast (altpll_0.c0) and slow (altpll_0.c2) clock domains. “Fast” devices are Nios II, RAM, Flash and SDRAM memories and SPI port. “Slow” devices are led_pio, lide_pio, timer, jtag_uart and sysid.

Conclusions:

System-on-chip design successfully compiled. Assignment score is 98/100.

Lessons Learned (What did you learn?):

I learned how to build an embedded system by using the Qsys tool and instantiating it to the main Verilog (or VHDL) design, in this case DE10_Lite_Default.v file. When we are building a shared bus system we need to have a bridge to let devices at different speeds to communicate.