

# Lab Notebook

## FPGA Capstone Project

### Academic Integrity

*By signing below you acknowledge the CU Honor Code, "On my honor, as a University of Colorado Boulder student I have neither given nor received unauthorized assistance" applies to this assignment.*

Signed: Glenn Frey Olamit

## Module 2

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### PWM

Author: Glenn Frey Olamit

Date: March 27, 2022

Procedure/Description of Test:

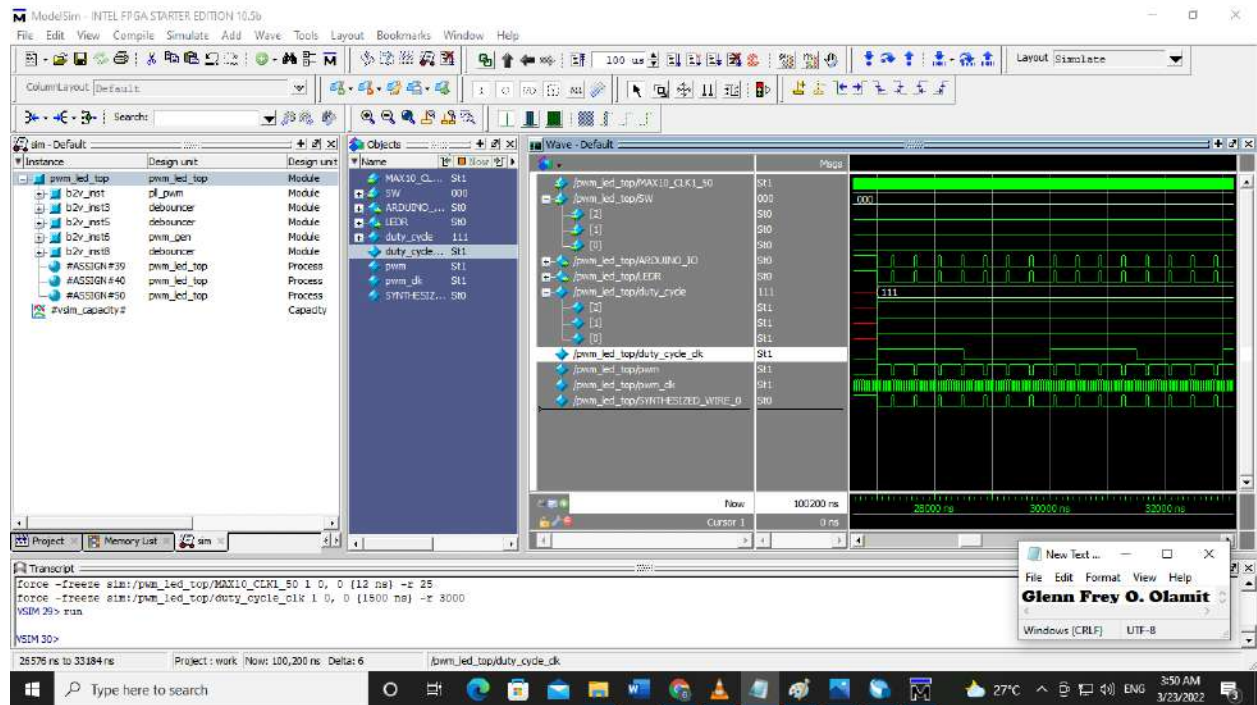
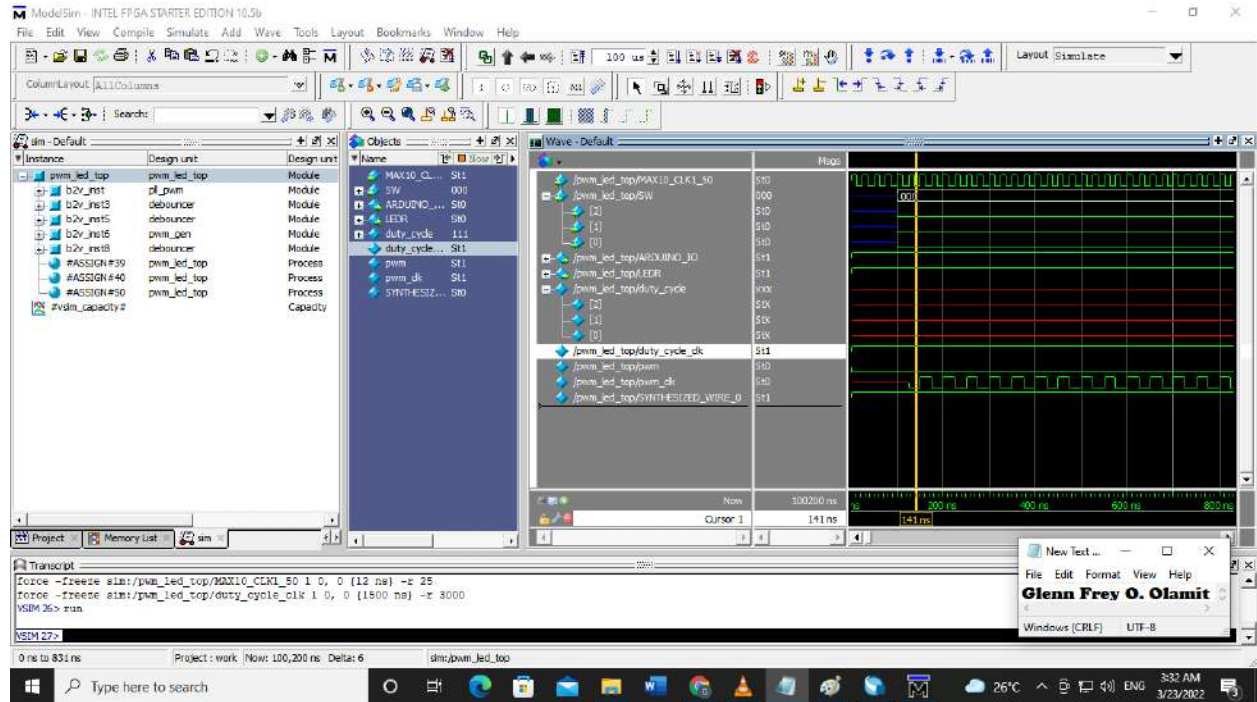
1. Compile design as per instruction, load into MAX10 SRAM.
2. Set different settings with the switches and observe LED

Observations:

The LED increases brightness as I change SW values from 000-111 , but never goes to zero (even if the SW are set to 000).

Data:

The simulation shows the following result:



## Images/Drawings:

The image displays two screenshots of the Quartus Prime Lite Edition software interface, showing the compilation process and timing analysis results for a project named 'pwm\_led\_top'.

**Top Screenshot:** The 'Flow Summary' window is open, showing the compilation status as 'Successful - Wed Mar 23 03:06:54 2022'. The summary includes the following details:

- Quartus Prime Version: 16.1.0 Build 196\_10/24/2016 SJ Lite Edition
- Revision Name: pwm\_led\_top
- Top-level Entity Name: pwm\_led\_top
- Family: MAX 10
- Device: 10M50DAF484CQGGS
- Timing Models: Preliminary
- Total logic elements: 33 / 49,760 (< 1 %)
- Total registers: 31
- Total pins: 6 / 360 (2 %)
- Total virtual pins: 0
- Total memory bits: 0 / 1,677,312 (0 %)
- Embedded Multiplier 9-bit elements: 0 / 288 (0 %)
- Total PLLs: 1 / 4 (25 %)
- UFM blocks: 0 / 1 (0 %)
- ADC blocks: 0 / 2 (0 %)

The 'Messages' window shows the following messages:

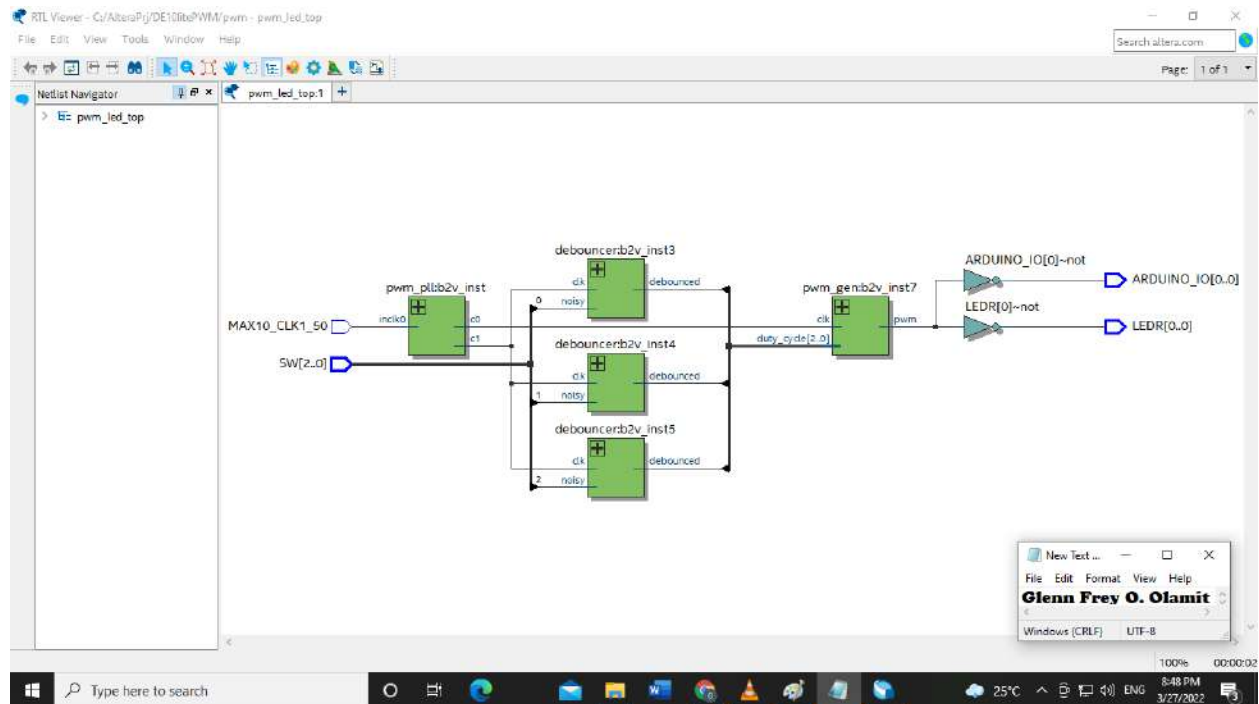
- quartus prime EDA Netlist writer was successful. 0 errors, 2 warnings
- 293000 quartus prime full compilation was successful. 0 errors, 201 warnings

**Bottom Screenshot:** The 'Slow 1200mV 85C Model Fmax Summary' window is open, showing the Fmax results for the design. The summary includes the following details:

	Fmax	Restricted Fmax	Clock Name	Note
1	562.11 MHz	450.05 MHz	b2v_inst[altpd_ed]pll1[clk1]	limit du_n (min)
2	615.01 MHz	450.05 MHz	b2v_inst[altpd_ed]pll1[clk0]	limit du_n (min)

The 'Messages' window shows the following messages:

- quartus prime EDA Netlist writer was successful. 0 errors, 2 warnings
- 293000 quartus prime full compilation was successful. 0 errors, 201 warnings



Results:

Fmax	562.11 MHz (clk1) 615.01 MHz (clk0)
% Logic Utilization	<1%
Total registers	31

### Questions:

1. Did the LED change brightness depending on the setting of the first 3 switches? Yes! it increases as you change value of switch from 000-111.

Conclusions: The circuit works fine.

Lessons Learned (What did you learn?): I learned how to transfer HDL code into a block diagram and vice versa. A very useful skill. Also I learned how to use PWM control in the FPGA.

## ADC

Author: Glenn Frey Olamit

Date: March 28, 2022

Procedure/Description of Test:

3. Compile design as per instruction, load into MAX10 SRAM.
4. Observe Values on 7-segment display
5. Connect Jumper Cable
6. Observe Values on 7-segment display

### Observations:

Without the jumper cable, all digits are zero, except the last one is changing very rapidly between 2 and 3 (it's changing so fast, it looks like a 6). With the jumper cable, the value is proportional to the input setting on the SW.

### Data:

SW setting	Value Measured
000	0x0158
001	0x02A8
010	0x0498
011	0x0558
100	0x0658
101	0x0808
110	0x0968
111	0x0A68



## Images/Drawings:

The image displays two screenshots of the Quartus Prime Lite Edition software interface, showing the compilation process and results for a project named 'pwm\_led\_top'.

**Top Screenshot:** The 'Flow Summary' window is open, showing the compilation status as 'Successful - Thu Mar 24 16:14:06 2022'. The summary includes the following details:

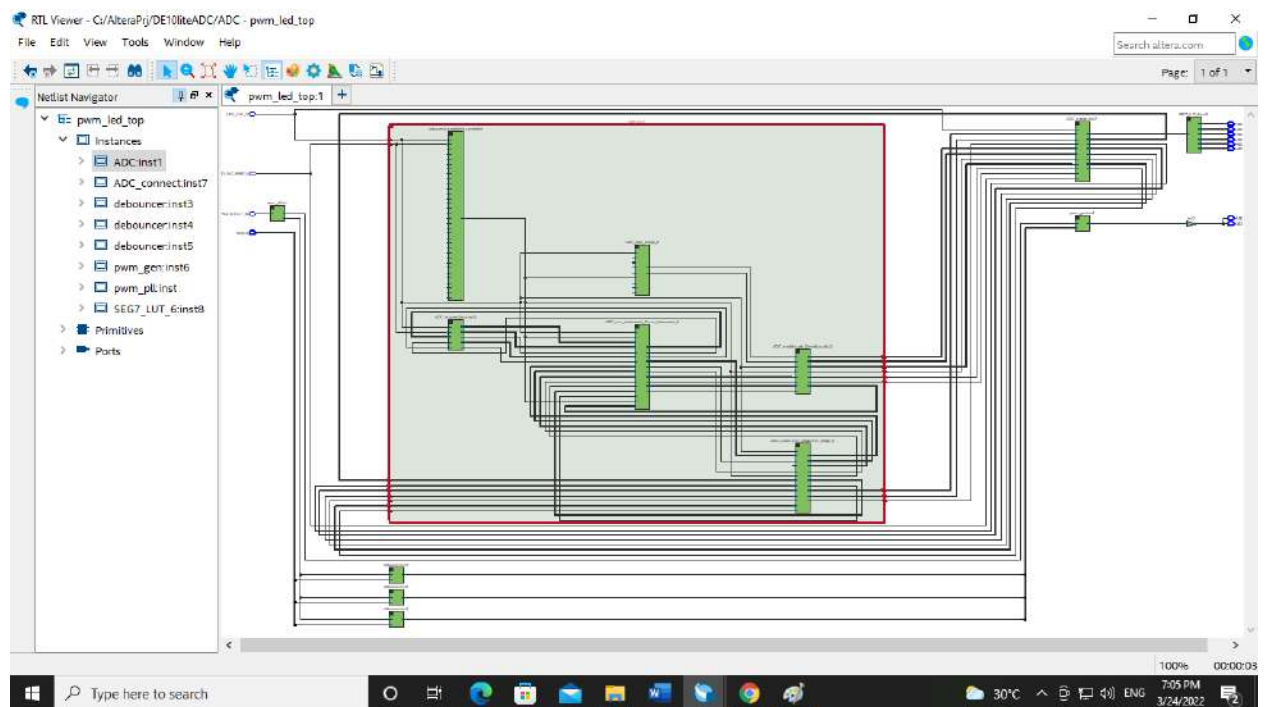
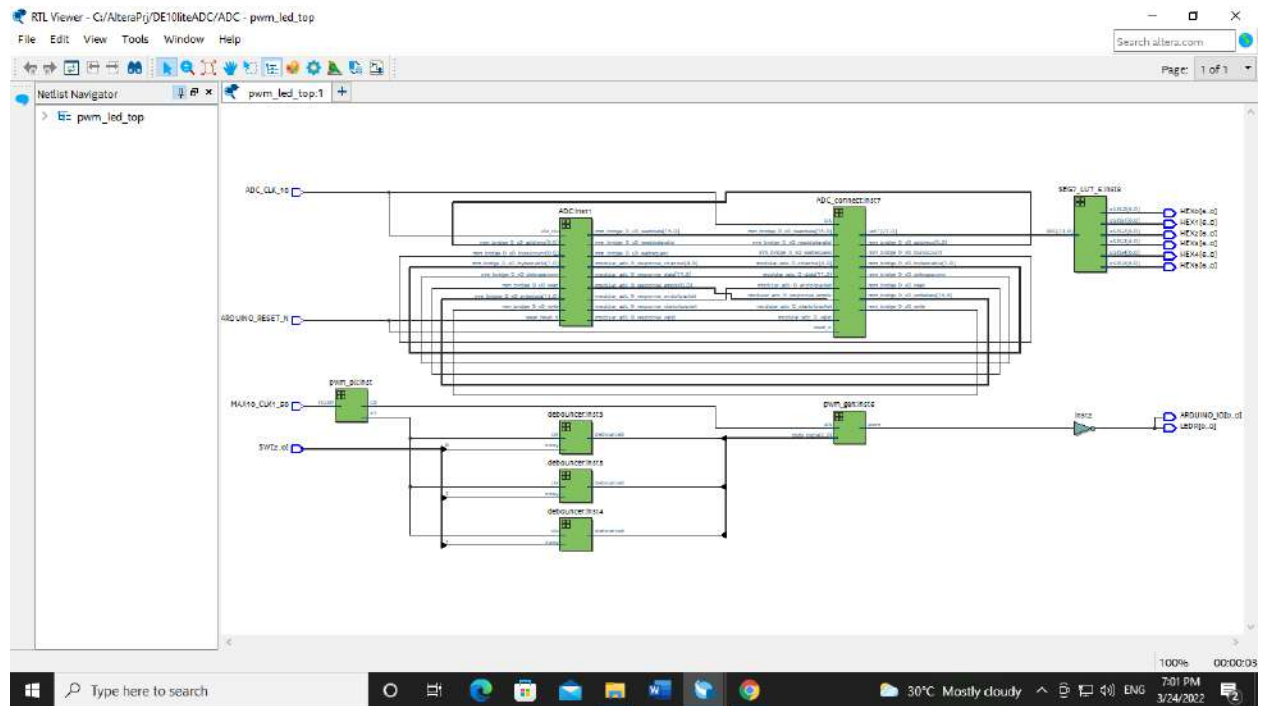
- Flow Status: Successful - Thu Mar 24 16:14:06 2022
- Quartus Prime Version: 16.1.0 Build 196 10/24/2016 SJ Lite Edition
- Revision Name: pwm\_led\_top
- Top-level Entity Name: pwm\_led\_top
- Family: MAX 10
- Device: 10M50DAF484C6GEG
- Timing Models: Preliminary
- Total logic elements: 4,744 / 49,760 (10 %)
- Total registers: 3233
- Total pins: 50 / 360 (14 %)
- Total virtual pins: 0
- Total memory bits: 270,176 / 1,677,312 (16 %)
- Embedded Multiplier 9-bit elements: 0 / 286 (0 %)
- Total PLLs: 2 / 4 (50 %)
- UFM blocks: 0 / 1 (0 %)
- ADC blocks: 1 / 2 (50 %)

The 'Messages' window shows a warning: '18236 number of processors has not been specified which may cause overloading on shared machines. set the global assignment NUM\_PARALLEL\_PROCESSORS in your quartus prime Netlist Viewers preprocess was successful. 0 errors, 1 warning'.

**Bottom Screenshot:** The 'Slow 1200mV 85C Model Fmax Summary' window is open, showing a table of Fmax values for various clocks:

Fmax	Restricted Fmax	Clock Name	Note
1 50.38 MHz	50.38 MHz	ADC_CLK_10	
2 76.46 MHz	76.46 MHz	altera_reserved_tck	
3 477.1 MHz	450.05 MHz	inst[altpll_co_ed]pll1[clk[1]	limit du_n (tmin)
4 546.75 MHz	450.05 MHz	inst[altpll_co_ed]pll1[clk[0]	limit du_n (tmin)

The 'Messages' window shows the same warning as in the top screenshot.





Results:

Fmax	50.38 MHz
%Logic Utilization	10%
Total registers	3233

Questions:

1. Does the board behave as you expected? Yes, the board behaves correctly
2. Is this a good voltmeter as is? Only partly, since the values are changing so fast, they can't be seen, and the units are not in Volt, but in some raw value (0x000 to 0xFFFF)
3. What could you change in either the board hardware or FPGA logic to make it perform better? A filter should be added, to reduce the noise in the last digit, and the value should be converted into Volt.



### Conclusions:

The System works fine, but could still be improved.

### Lessons Learned (What did you learn?):

How to build a system with Qsys. That the system built uses relatively many logic resources.

Hex Display shouldn't be driven so fast, it makes it unreadable.