**NAME\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Total Marks: [25]**

**Mark values are shown in [brackets] for each question**

**OBJECTIVES:**

Upon completion of this assignment, you should be able to:

* Write VHDL statements assigning values to individual elements of a BIT\_VECTOR or STD\_LOGIC\_VECTOR.
* Write a selected signal assignment statement in VHDL using INTEGER types.
* Write VHDL statements that use signals to combine inputs or separate outputs.

**REFERENCE READING:**

# Dueck, Robert K., *Digital Design with CPLD Applications and VHDL*:

Chapter 5: Introduction to VHDL

**EQUIPMENT REQUIRED:** None

**ASSIGNMENT:**

**1a.** Write a VHDL statement that defines an 8-bit input port, **addr**, with the most significant bit on the left. Assume port the is of type BIT\_VECTOR. [2]

**b.** Write a VHDL statement that defines an 8-bit input port, **addr**, with the most significant bit on the right. Assume port the is of type BIT\_VECTOR. [2]

**2a.** An output port is defined as x : OUT BIT\_VECTOR(5 downto 0); It is assigned a value by the statement x <= “100101”; Write the equivalent VHDL statements that will assign the port values separately for each bit. [2]

**b.** Repeat Problem 2a for the case where the output is defined as:

x : OUT BIT\_VECTOR(0 to 5); and x is assigned by the statement x <= “100101”; [2]

**3.** Write a VHDL file to encode the following truth table. Define the input, **d**, as an INTEGER and the output, **y**, as type BIT. [5]

|  |  |  |  |
| --- | --- | --- | --- |
| **d(2)** | **d(1)** | **d(0)** | **y** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**4.** A VHDL design has five input ports labeled **enable** (MSB), **read**, **write**, **selector**, and **compare** (LSB) and three outputs labeled **address\_latch** (MSB), **data\_enable**, and **strobe** (LSB).

**a.** Write a VHDL statement that concatenates all input lines into a signal called **control**. The signal is written with the most significant bit on the left. [3]

**b.** Write a series of VHDL statements that separate a signal called **status** into the output ports listed above. The ports are written with the most significant bit on the left. [3]

**5.** Write a VHDL file that uses a selected signal assignment statement to encode the following truth table. [6]

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | C | X | Y | Z |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 |