50μV V_{OS}, 0.25μV/°C, 35μA CMOS OPERATIONAL AMPLIFIERS Zerø-Drift Series

Check for Samples: OPA330, OPA2330, OPA4330

FEATURES

- **UNMATCHED PRICE PERFORMANCE**
- **LOW OFFSET VOLTAGE: 50μV (max)**
- **ZERO DRIFT: 0.25μV/°C (max)**
- **LOW NOISE: 1.1μV_{PP}, 0.1Hz to 10Hz**
- **QUIESCENT CURRENT: 35μA (max)**
- **SUPPLY VOLTAGE: 1.8V to 5.5V**
- **RAIL-TO-RAIL INPUT/OUTPUT**
- **INTERNAL EMI FILTERING**
- ***micro*SIZE PACKAGES: WCSP, SC70, QFN**

APPLICATIONS

- **BATTERY-POWERED INSTRUMENTS**
- **TEMPERATURE MEASUREMENTS**
- **TRANSDUCER APPLICATIONS**
- **ELECTRONIC SCALES**
- **MEDICAL INSTRUMENTATION**
- **HANDHELD TEST EQUIPMENT**
- **CURRENT SENSE**

DESCRIPTION

The OPA330 series of CMOS operational amplifiers offer precision performance at a very competitive price. These devices are members of the Zerø-Drift family of amplifiers which use a proprietary auto-calibration technique to simultaneously provide low offset voltage (50μV max) and near-zero drift over time and temperature at only 35μA (max) of quiescent current. The OPA330 family features rail-to-rail input and output in addition to near flat 1/f noise, making this amplifier ideal for many applications and much easier to design into a system. These devices are optimized for low-voltage operation as low as +1.8V (±0.9V) and up to +5.5V (±2.75V).

The OPA330 (single version) is available in the WCSP-5, SC70-5, SOT23-5, and SOIC-8 packages. The OPA2330 (dual version) is offered in DFN-8 (3mm × 3mm), MSOP-8, and SOIC-8 packages. The OPA4330 is offered in the standard SOIC-14 and TSSOP-14 packages, as well as in the space-saving VQFN-14 package. All versions are specified for operation from –40°C to +125°C.

PRODUCT FAMILY PACKAGE COMPARISON

DEVICE	NO OF CHANNELS	PACKAGE-LEADS						
		WCSP	SOIC	SOT23	SC70	MSOP	QFN	TSSOP
OPA330	1	5	8	5	5	–	–	–
OPA2330	2	–	8	–	–	8	8	–
OPA4330	4	–	14	–	–	–	14	14

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA330	SOT23-5	DBV	OCFQ
	SC70-5	DCK	CHL
	SOIC-8	D	O330A
	WCSP-5	YFF	OEH
OPA2330	SOIC-8	D	O2330A
	DFN-8	DRB	OCGQ
	MSOP-8	DGK	OCGQ
OPA4330	SOIC-14	D	O4330A
	TSSOP-14	PW	O4330A
OPA4330	QFN-14(2)	RGY	4330A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.
(2) Product preview device.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA330, OPA2330, OPA4330	UNIT
Supply Voltage, V_S = (V+) – (V–)		+7	V
Signal Input Terminals, Voltage(2)		(V–) –0.3 to (V+) + 0.3	V
Signal Input Terminals, Current(2)		±10	mA
Output Short-Circuit(3)		Continuous	
Operating Temperature		–40 to +150	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		+150	°C
ESD Ratings:	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	400	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

THERMAL INFORMATION

THERMAL METRIC(1)		OPA330AIYFF YFF 5 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	130	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	54	
θ_{JB}	Junction-to-board thermal resistance	51	
ψ_{JT}	Junction-to-top characterization parameter	1	
ψ_{JB}	Junction-to-board characterization parameter	50	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA330, OPA2330, OPA4330			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5V		8	50	µV
vs Temperature	**dV_{OS}/dT**			**0.02**	**0.25**	**µV/°C**
vs Power Supply	**PSRR**	**V_S = +1.8V to +5.5V**		**1**	**10**	**µV/V**
Long-Term Stability(1)				See (1)		
Channel Separation, dc				0.1		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±200	±500	pA
Input Bias Current: OPA330YFF, OPA4330				±70	±300	pA
over Temperature				**±300**		**pA**
Input Offset Current	I_{OS}			±400	±1000	pA
Input Offset Current: OPA330YFF, OPA4330				±140	±600	pA
NOISE						
Input Voltage Noise Density	e_n	f = 1kHz		55		nV/√Hz
Input Voltage Noise		f = 0.01Hz to 1Hz		0.3		μV_{PP}
Input Voltage Noise		f = 0.1Hz to 10Hz		1.1		μV_{PP}
Input Current Noise	i_n	f = 10Hz		100		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	**CMRR**	**(V–) – 0.1V < V_{CM} < (V+) + 0.1V**	**100**	**115**		**dB**
Common-Mode Rejection Ratio: OPA330YFF, OPA4330		**(V–) – 0.1V < V_{CM} < (V+) + 0.1V, V_S = 5.5V**	**100**	**115**		**dB**
INPUT CAPACITANCE						
Differential				2		pF
Common-Mode				4		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**(V–) + 100mV < V_O < (V+) – 100mV, R_L = 10kΩ**	**100**	**115**		**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	C_L = 100pF		350		kHz
Slew Rate	SR	G = +1		0.16		V/µs
OUTPUT						
Voltage Output Swing from Rail				**30**	**100**	**mV**
Short-Circuit Current	I_{SC}			±5		mA
Capacitive Load Drive	C_L		See Typical Characteristics			
Open-Loop Output Impedance		f = 350kHz, I_O = 0		2		kΩ
POWER SUPPLY						
Specified Voltage Range	V_S		1.8		5.5	V
Quiescent Current Per Amplifier	**I_Q**	**I_O = 0**		**21**	**35**	**µA**
Turn-On Time		V_S = +5V		100		µs

(1) 300-hour life test at +150°C demonstrated randomly distributed variation of approximately 1µV.

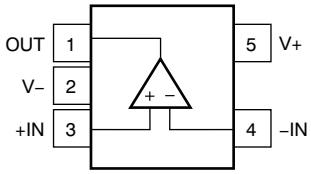
ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

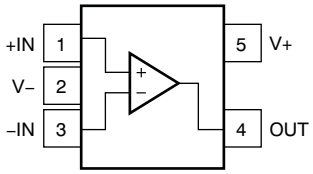
PARAMETER	TEST CONDITIONS	OPA330, OPA2330, OPA4330			UNIT
		MIN	TYP	MAX	
TEMPERATURE RANGE					
Specified Range		–40		+125	°C
Operating Range		–40		+150	°C
Storage Range		–65		+150	°C
Thermal Resistance θ_{JA}					°C/W
SOT23-5			200		°C/W
MSOP-8, SOIC-8, TSSOP-14			150		°C/W
DFN-8			50		°C/W
SC70-5			250		°C/W
WCSP-5			130		°C/W

PIN CONFIGURATIONS

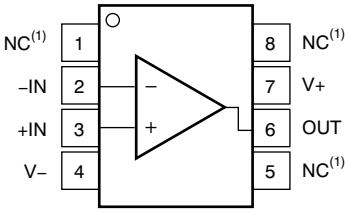
OPA330
SOT23-5
(TOP VIEW)



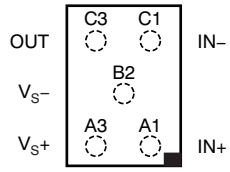
OPA330
SC70-5
(TOP VIEW)



OPA330
SOIC-8
(TOP VIEW)



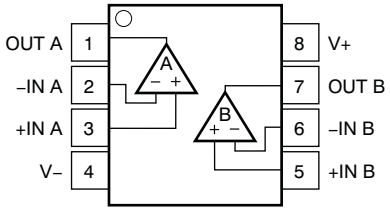
OPA330
WCSP-5
(TOP VIEW)



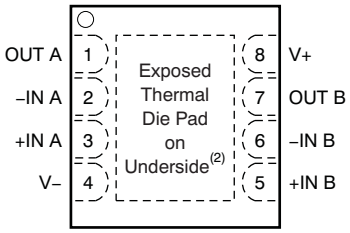
(1) NC denotes no internal connection.

PIN CONFIGURATIONS, CONTINUED

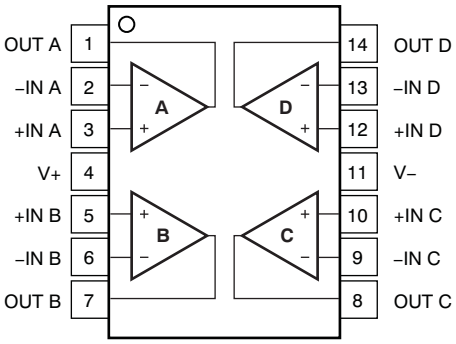
OPA2330
SOIC-8, MSOP-8
(TOP VIEW)



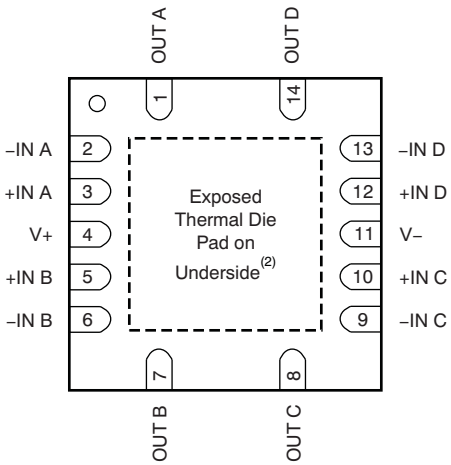
OPA2330
DFN-8
(TOP VIEW)



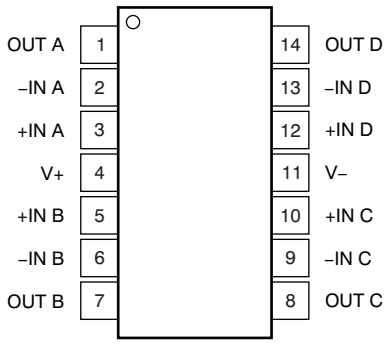
OPA4330
SOIC-14
(TOP VIEW)



OPA4330
QFN-14
(TOP VIEW)



OPA4330
TSSOP-14
(TOP VIEW)



(2) Connect thermal die pad to V–.

TYPICAL CHARACTERISTICS

At T_A = +25°C, C_L = 0pF, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

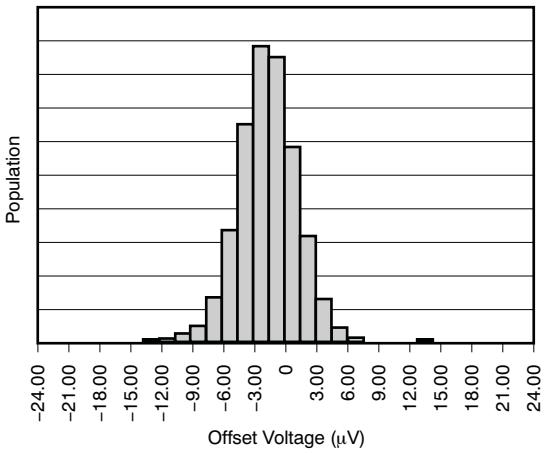


Figure 1.

OPEN-LOOP GAIN vs FREQUENCY

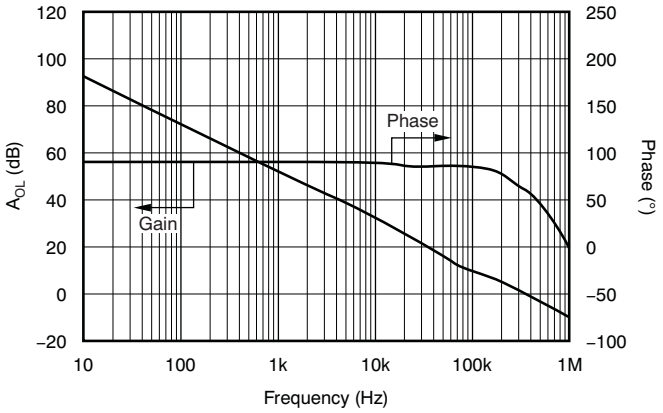


Figure 2.

COMMON-MODE REJECTION RATIO vs FREQUENCY

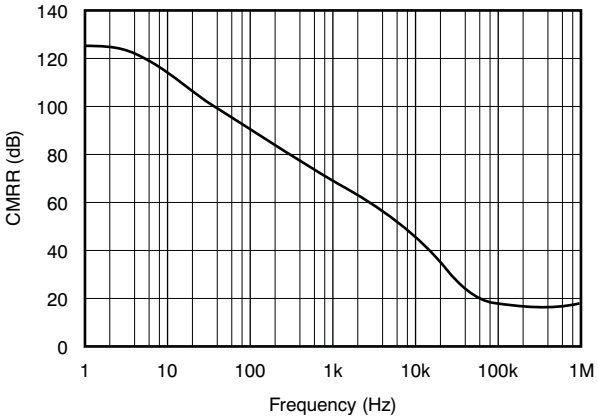


Figure 3.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

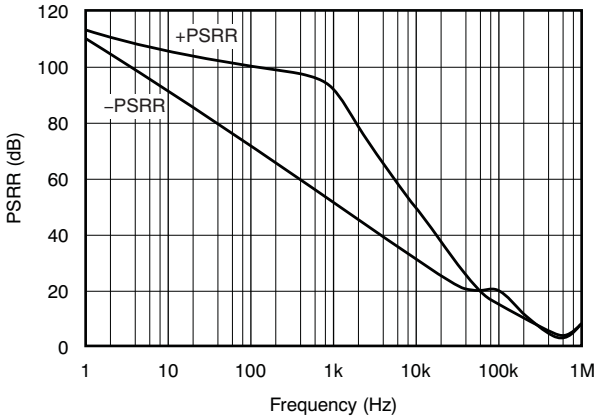


Figure 4.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

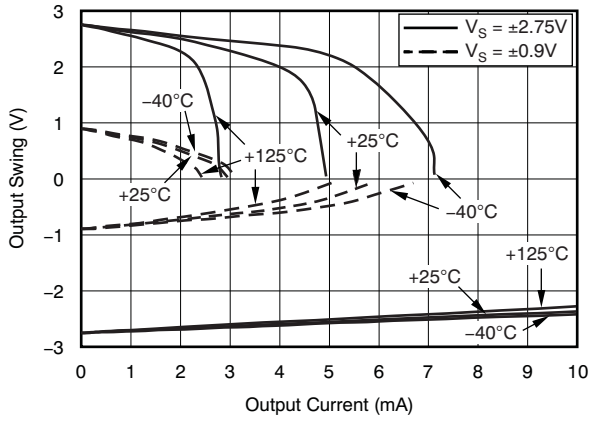


Figure 5.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

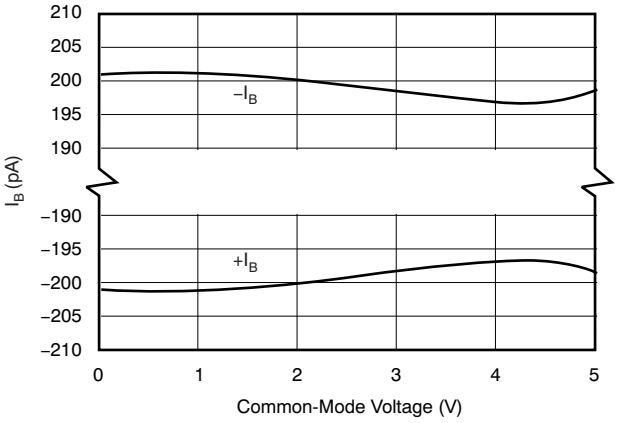


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, C_L = 0pF, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE

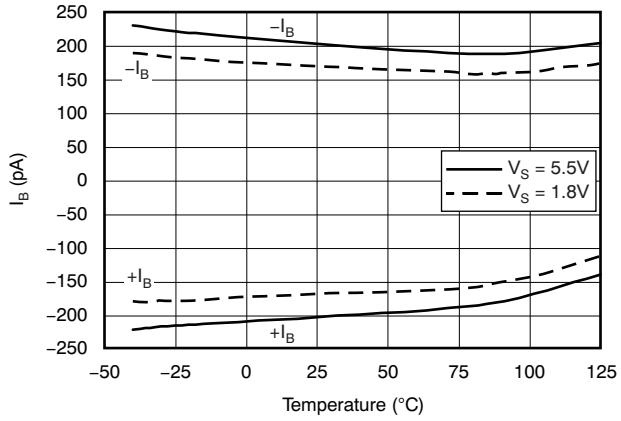


Figure 7.

QUIESCENT CURRENT vs TEMPERATURE

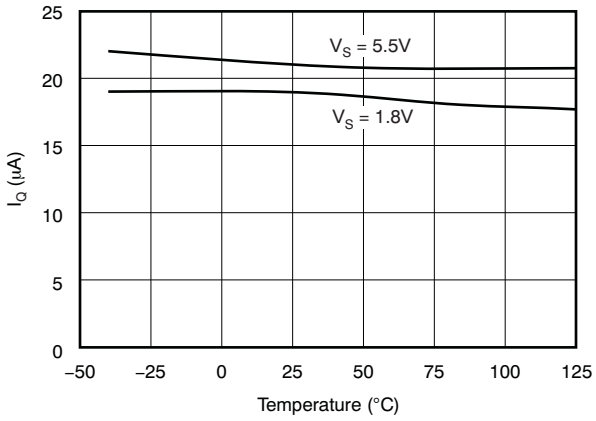


Figure 8.

LARGE-SIGNAL STEP RESPONSE

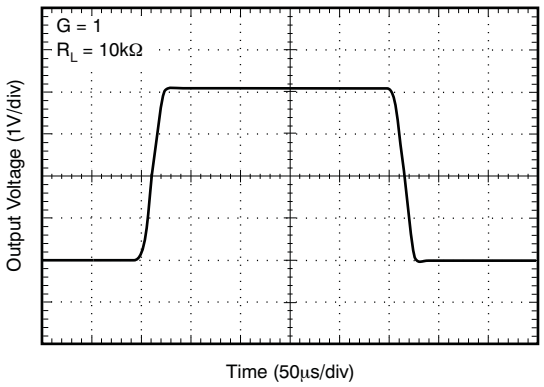


Figure 9.

SMALL-SIGNAL STEP RESPONSE

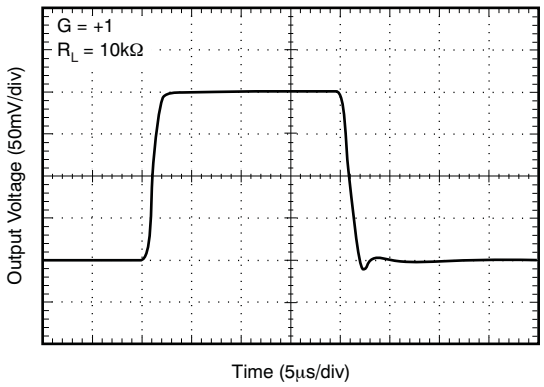


Figure 10.

POSITIVE OVER-VOLTAGE RECOVERY

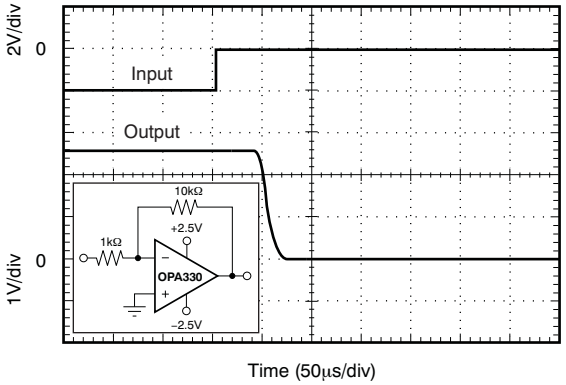


Figure 11.

NEGATIVE OVER-VOLTAGE RECOVERY

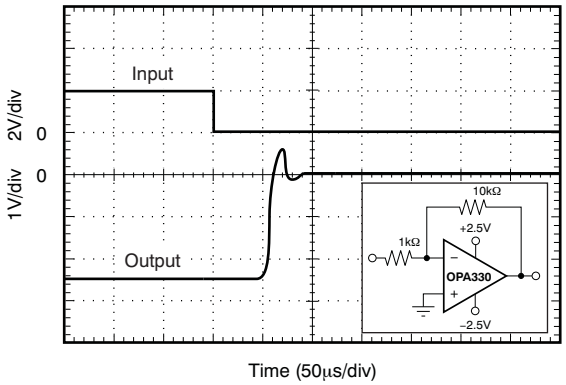


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, C_L = 0pF, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

SETTLING TIME vs CLOSED-LOOP GAIN

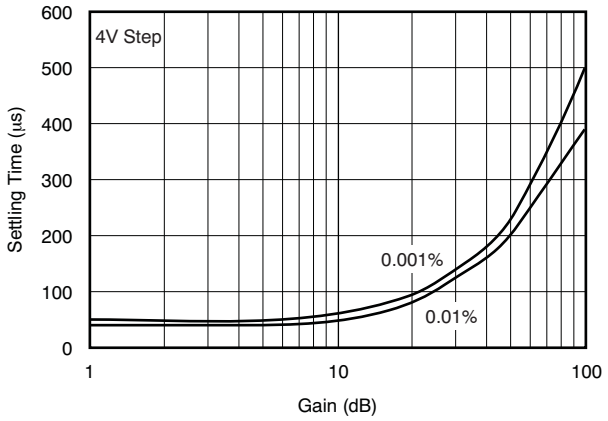


Figure 13.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

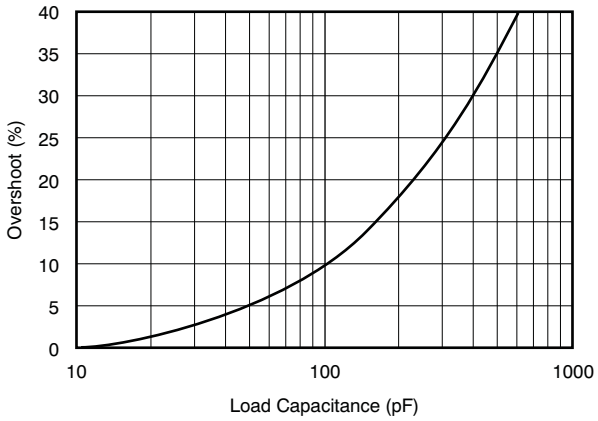


Figure 14.

0.1Hz TO 10Hz NOISE

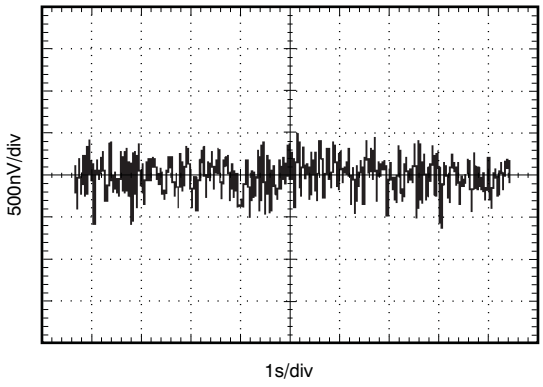


Figure 15.

CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

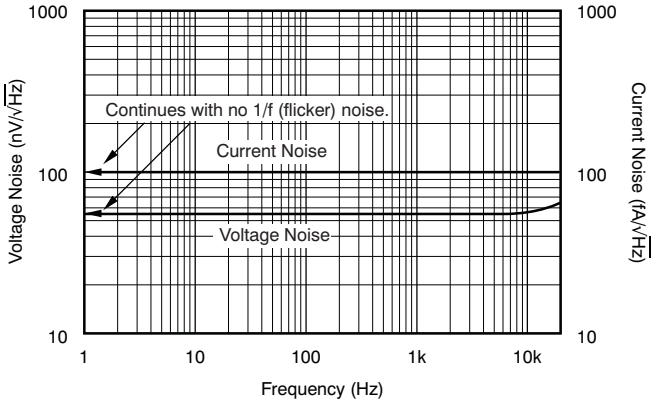


Figure 16.

INPUT BIAS CURRENT vs INPUT DIFFERENTIAL VOLTAGE

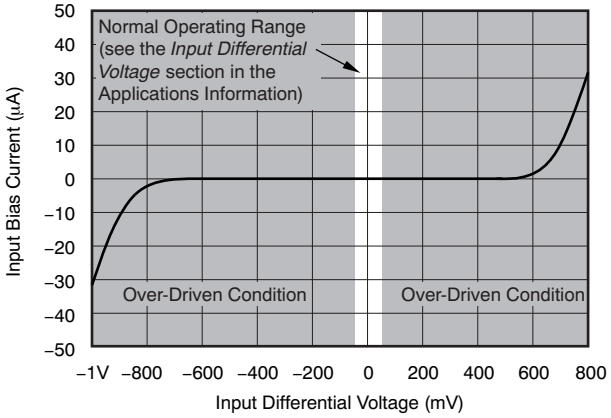


Figure 17.

APPLICATIONS INFORMATION

The OPA330, OPA2330, and OPA4330 are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. The use of proprietary Zerø-Drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPA330 family is optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100mV beyond the supplies and a rail-to-rail output that swings within 100mV of the supplies under normal test conditions. The OPA330 series are precision amplifiers for cost-sensitive applications.

OPERATING VOLTAGE

The OPA330 series op amps can be used with single or dual supplies from an operating range of V_S = +1.8V (±0.9V) up to +5.5V (±2.75V). Supply voltages greater than +7V can permanently damage the device. See the Absolute Maximum Ratings table. Key parameters that vary over the supply voltage or temperature range are shown in the Typical Characteristics section of this data sheet.

INPUT VOLTAGE

The OPA330, OPA2330, and OPA4330 input common-mode voltage range extends 0.1V beyond the supply rails. The OPA330 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is about 200pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.

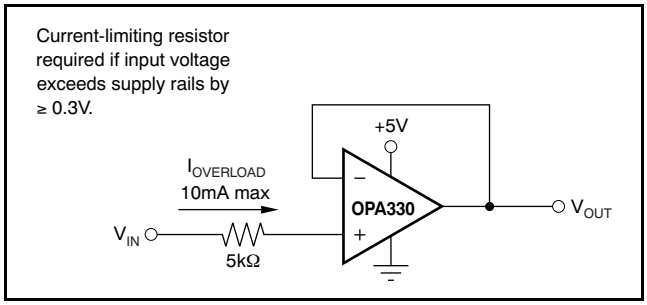


Figure 18. Input Current Protection

INPUT DIFFERENTIAL VOLTAGE

The typical input bias current of the OPA330 during normal operation is approximately 200pA. In over-driven conditions, the bias current can increase significantly (see Figure 17).The most common cause of an over-driven condition occurs when the op amp is outside of the linear range of operation. When the output of the op amp is driven to one of the supply rails the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front end input chopping switches that combine with 10kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 19. Notice that the input bias current remains within specification within the linear region.

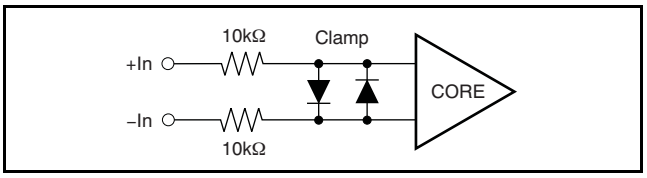


Figure 19. Equivalent Input Circuit

INTERNAL OFFSET CORRECTION

The OPA330, OPA2330, and OPA4330 op amps use an auto-calibration technique with a time-continuous 125kHz op amp in the signal path. This amplifier is zero-corrected every 8μs using a proprietary technique. Upon power-up, the amplifier requires approximately 100μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in their susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from its nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA330 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 8MHz (–3dB), with a roll-off of 20dB per decade.

ACHIEVING OUTPUT SWING TO THE OP AMP NEGATIVE RAIL

Some applications require output voltage swings from 0V to a positive full-scale voltage (such as +2.5V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA330, OPA2330, and OPA4330 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pull-down resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 20.

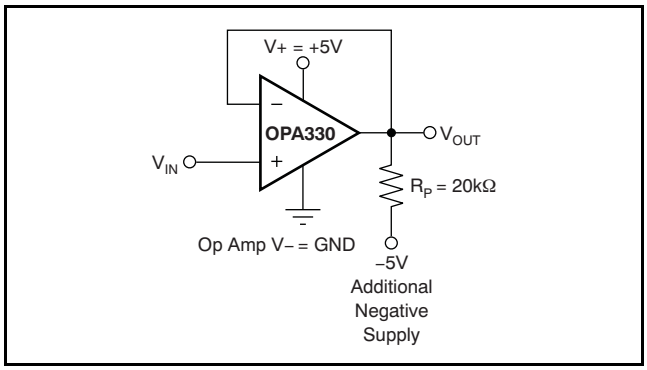


Figure 20. For V_{OUT} Range to Ground

The OPA330, OPA2330, and OPA4330 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA330, OPA2330, and OPA4330 have been characterized to perform with this technique; the recommended resistor value is approximately 20kΩ. Note that this configuration will increase the current consumption by several hundreds of microamps. Accuracy is excellent down to 0V and as low as –2mV. Limiting and nonlinearity occurs below –2mV, but excellent accuracy returns as the output is again driven above –2mV. Lowering the resistance of the pull-down resistor will allow the op amp to swing even further below the negative rail. Resistances as low as 10kΩ can be used to achieve excellent accuracy down to –10mV.

APPLICATION CIRCUITS

Figure 21 shows the basic configuration for a bridge amplifier.

A low-side current shunt monitor is shown in Figure 22.

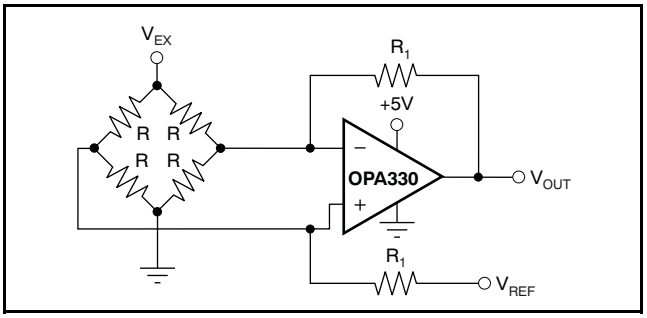
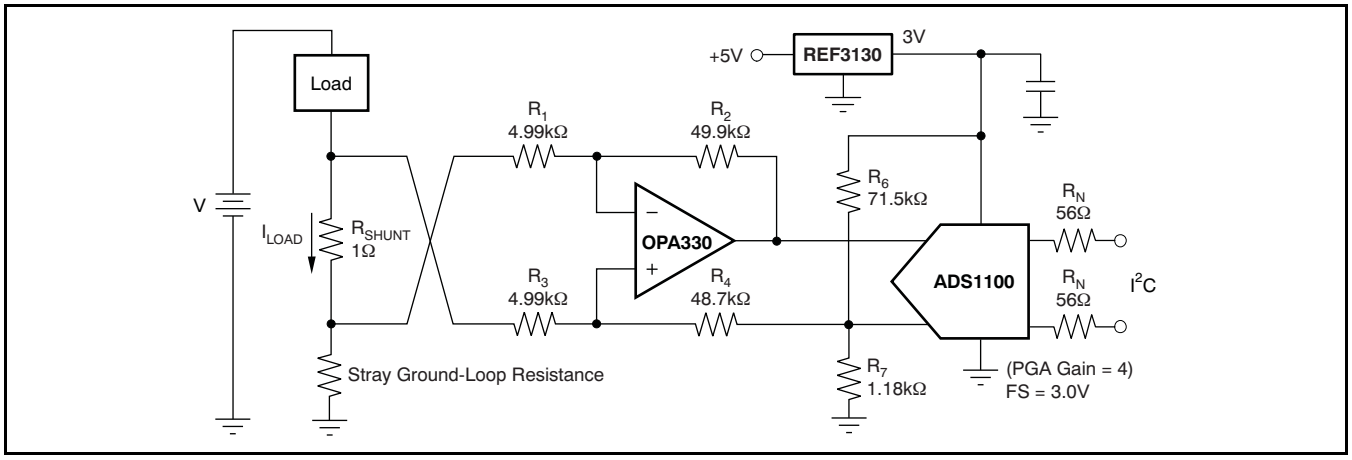


Figure 21. Single Op Amp Bridge Amplifier



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 22. Low-Side Current Monitor

R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. Because the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5V power supply is sufficiently stable, the REF3130 may be omitted.

Figure 23 shows the OPA330 in a typical thermistor circuit.

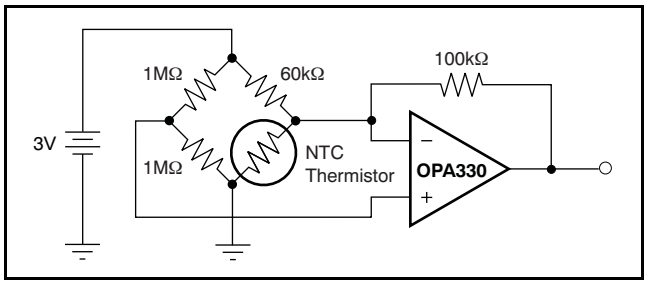


Figure 23. Thermistor Measurement

GENERAL LAYOUT GUIDELINES

Attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1μV/°C or higher, depending on materials used.

OPA330 WCSP

The OPA330 YFF package is a lead- (Pb-) free, die-level, wafer chip-scale package (WCSP). Unlike devices that are in plastic packages, these devices have no molding compound, lead frame, wire bonds, or leads. Using standard surface-mount assembly procedures, the WCSP can be mounted to a printed circuit board (PCB) without additional underfill. Figure 24 and Figure 25 detail the pinout and package marking, respectively. See the *NanoStar™ and NanoFree™ 300μm Solder Bump WCSP* Application Note (SBVA017) for more detailed information on package characteristics and PCB design.

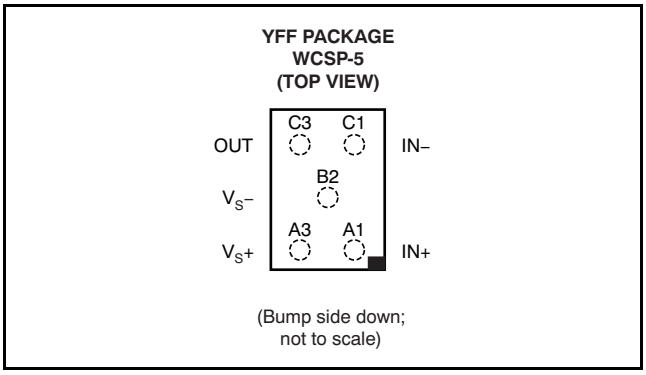


Figure 24. WCSP Pin Description

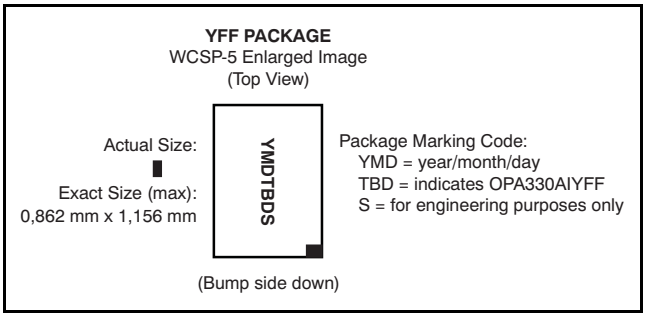


Figure 25. YFF Package Marking

PHOTOSENSITIVITY

Although the OPA330 YFF package has a protective backside coating that reduces the amount of light exposure on the die, unless fully shielded, ambient light can reach the active region of the device. Input bias current for the package is specified in the absence of light. Depending on the amount of light exposure in a given application, an increase in bias current, and possible increases in offset voltage should be expected. Fluorescent lighting may introduce noise or hum because of the time-varying light output. Best layout practices include end-product packaging that provides shielding from possible light sources during operation.

QFN AND DFN PACKAGES

The OPA4330 is offered in a QFN package. The OPA2330 is available in a DFN-8 package (also known as SON), which is a QFN package with lead contacts on only two sides of the bottom of the package. These leadless, near-chip-scale packages maximize board space and enhance thermal and electrical characteristics through an exposed pad. QFN and DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SOIC and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The QFN and DFN package can be easily mounted using standard PCB assembly techniques. See Application Note *QFN/SON PCB Attachment* (SLUA271) and Application Report *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package should be connected to V–.

QFN AND DFN LAYOUT GUIDELINES

The leadframe die pad should be soldered to a thermal pad on the PCB. A mechanical data sheet showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2009) to Revision D **Page**

- Added last *Applications* bullet 1
- Deleted footnote 1 from Product Family Package Comparison table 1
- Deleted footnote 2 and shading from all packages except QFN-14; moved WCSP-5, SOIC-14, and TSSOP-14 packages to Production Data status; and added package marking information to Package Information table 2
- Added *OPA330YFF, OPA4330* Input Bias Current parameter to Electrical Characteristics table 3
- Added Input Voltage Range, *OPA330YFF, OPA4330 Common-Mode Rejection Ratio* parameter to Electrical Characteristics table 3
- Moved TSSOP-14 thermal resistance to MSOP-8, SOIC-8 thermal resistance parameter in Electrical Characteristics table 4
- Deleted SOIC-14 and QFN-14 rows from Temperature Range section in Electrical Characteristics table 4

Changes from Revision B (September, 2009) to Revision C **Page**

- Changed maximum quiescent current value (*Features* list, document title) to 35μA 1
- Changed maximum value for Quiescent Current per Amplifier specification 3
- Added *Application Circuits* section 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA2330AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
OPA2330AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
OPA2330AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
OPA2330AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
OPA2330AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA2330AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA2330AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA2330AIDRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA2330AIDRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA2330AIDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
OPA2330AIDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
OPA2330AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA330AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
OPA330AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
OPA330AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
OPA330AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA330AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
OPA330AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA330AIDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA330AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA330AIDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA330AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
OPA330AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA330AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
OPA330AIYFFR	PREVIEW	DSBGA	YFF	5	3000	TBD	Call TI	Call TI	Samples Not Available
OPA330AIYFFT	PREVIEW	DSBGA	YFF	5	250	TBD	Call TI	Call TI	Samples Not Available
OPA4330AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA4330AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA4330AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
OPA4330AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA4330AIRGYR	PREVIEW	VQFN	RGY	14	3000	TBD	Call TI	Call TI	Samples Not Available
OPA4330AIRGYT	PREVIEW	VQFN	RGY	14	250	TBD	Call TI	Call TI	Samples Not Available

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

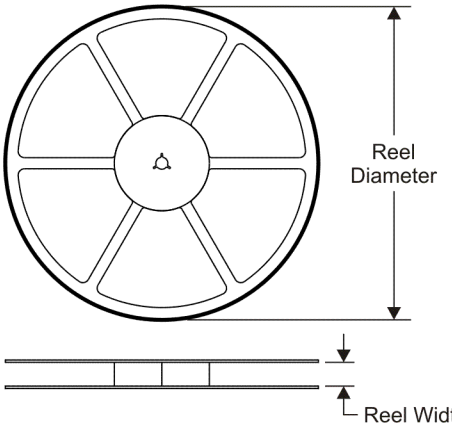
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

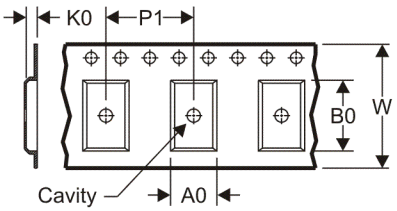
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

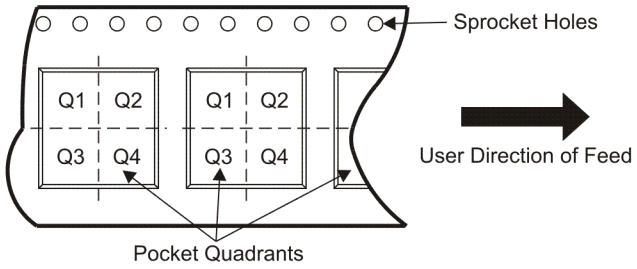


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

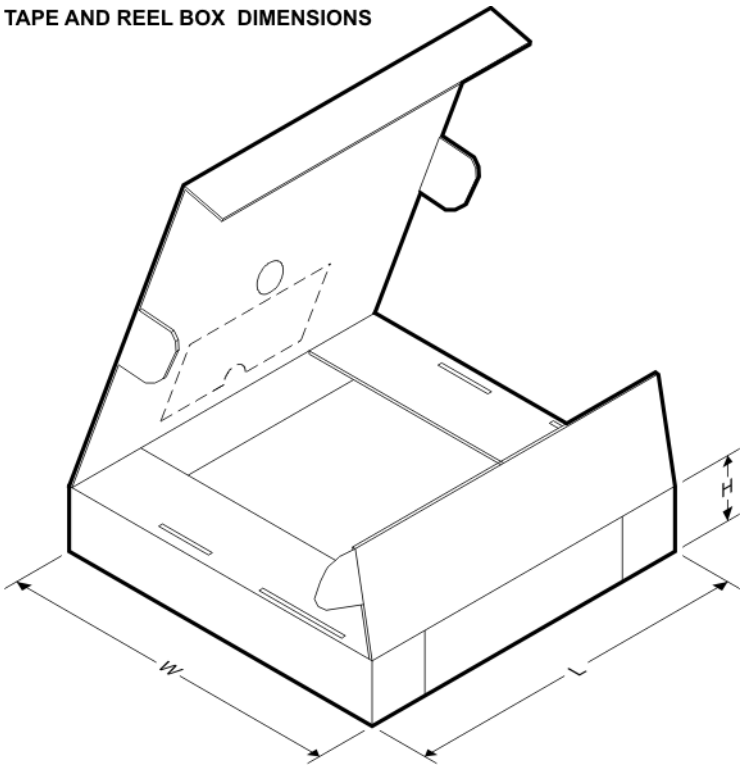
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2330AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
OPA2330AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
OPA2330AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2330AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2330AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA330AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA330AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA330AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA330AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA330AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4330AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4330AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

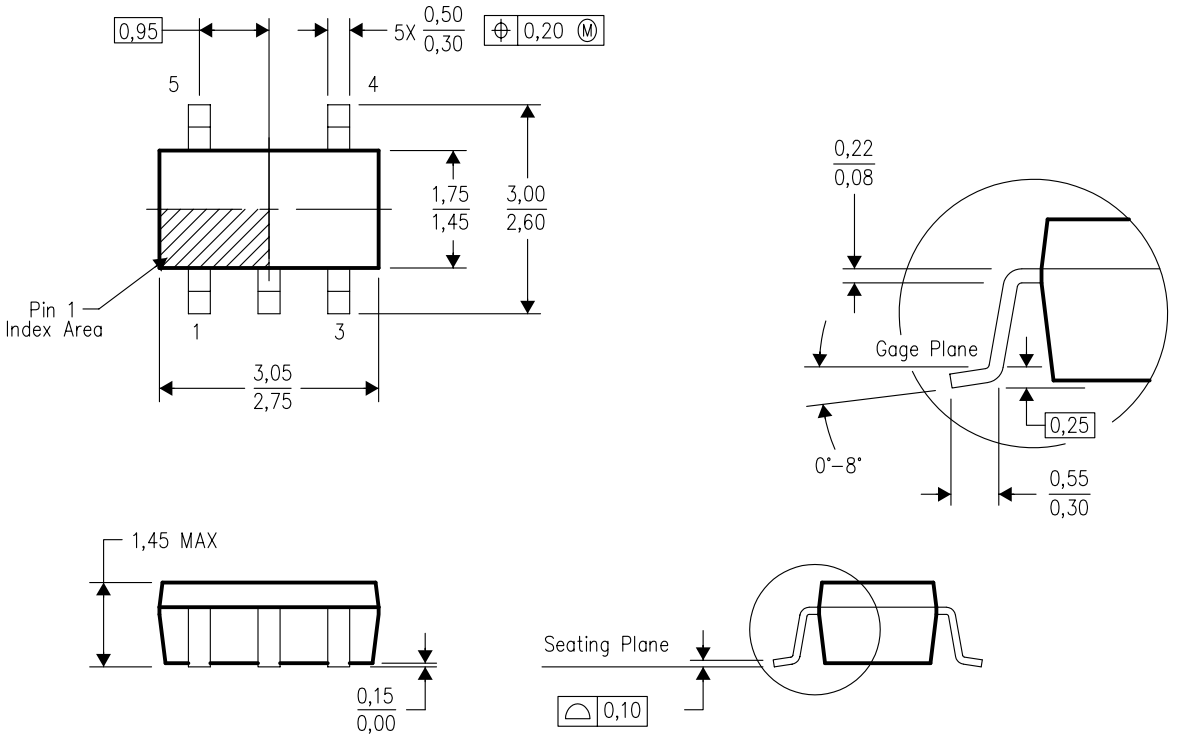
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2330AIDGKR	MSOP	DGK	8	2500	346.0	346.0	35.0
OPA2330AIDGKT	MSOP	DGK	8	250	203.0	203.0	35.0
OPA2330AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA2330AIDRBR	SON	DRB	8	3000	346.0	346.0	29.0
OPA2330AIDRBT	SON	DRB	8	250	190.5	212.7	31.8
OPA330AIDBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA330AIDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
OPA330AIDCKR	SC70	DCK	5	3000	203.0	203.0	35.0
OPA330AIDCKT	SC70	DCK	5	250	203.0	203.0	35.0
OPA330AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA4330AIDR	SOIC	D	14	2500	346.0	346.0	33.0
OPA4330AIPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

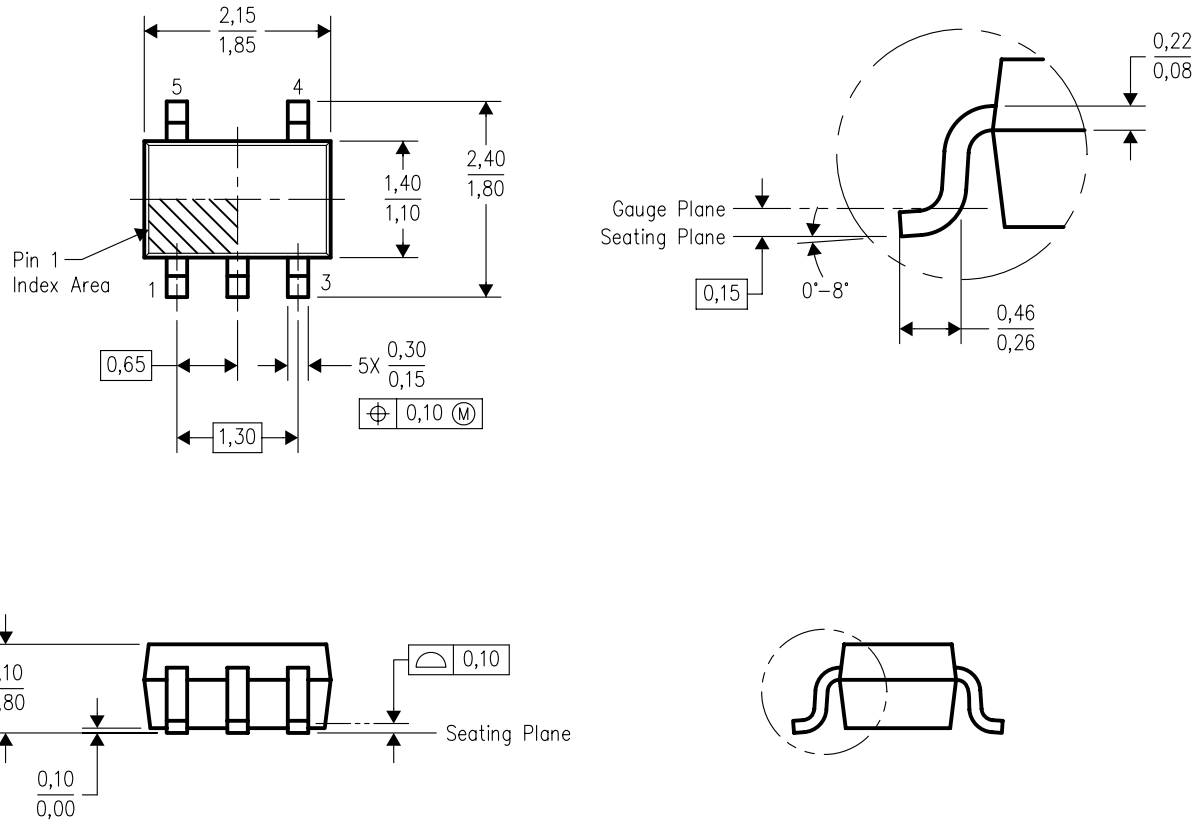
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

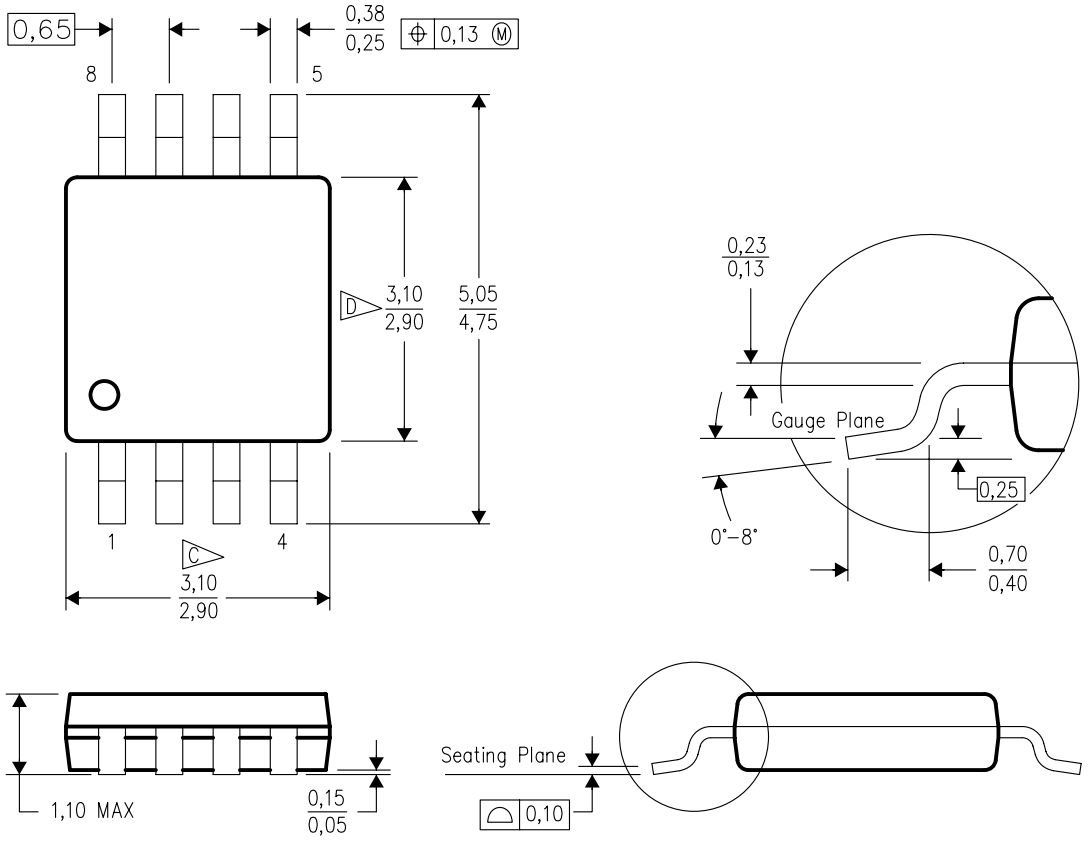
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

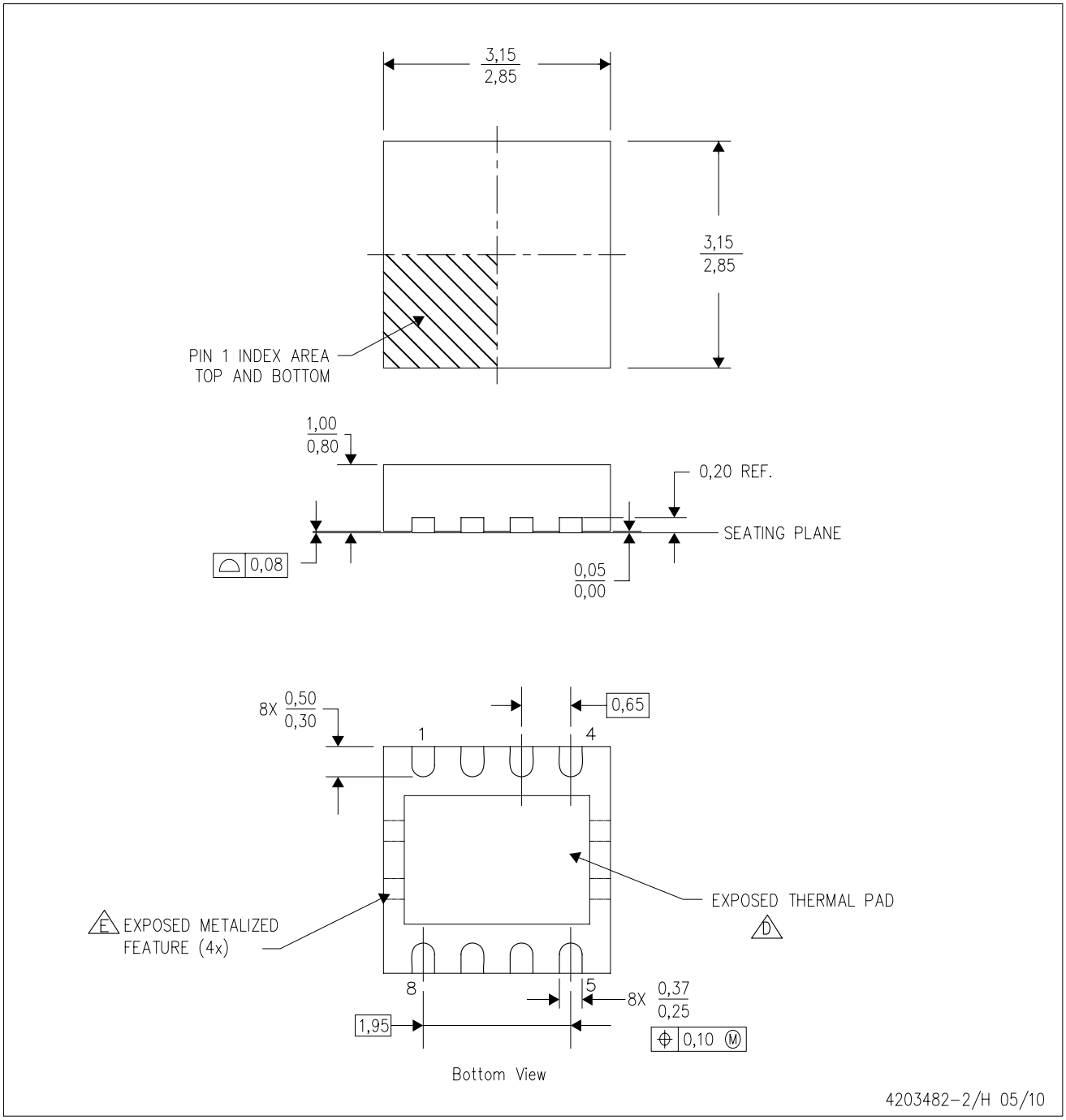
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

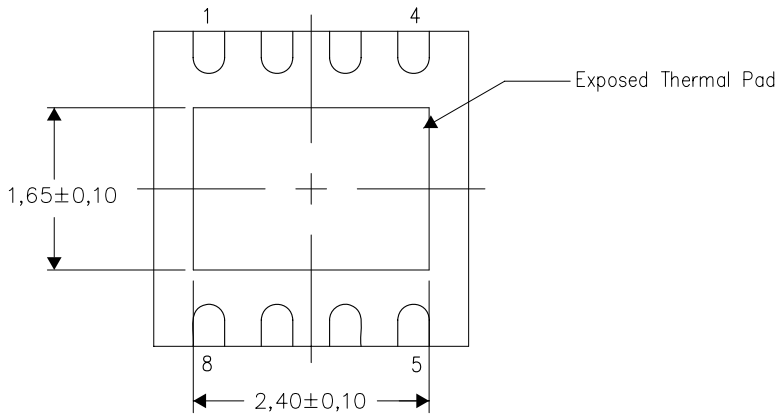
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

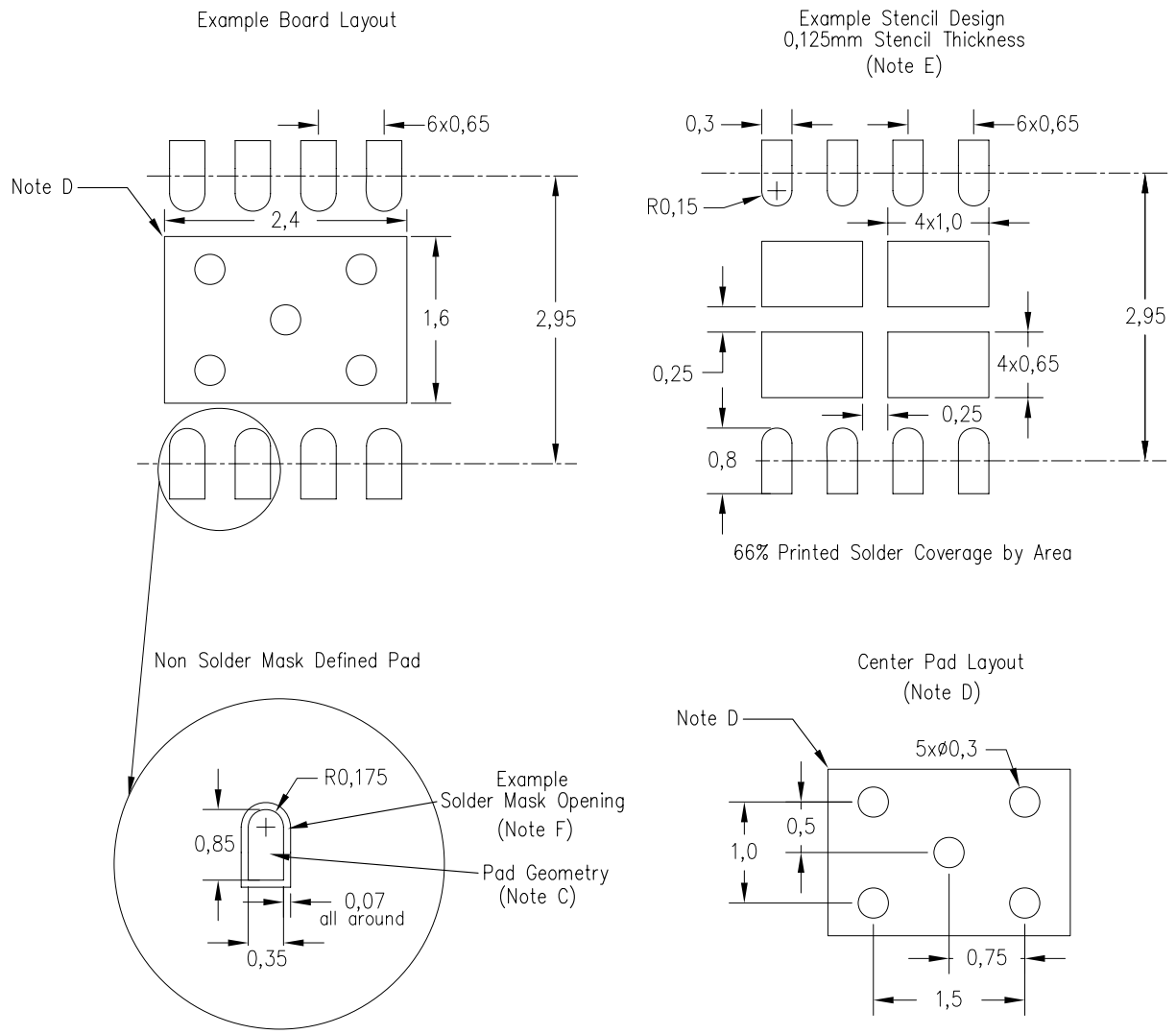


Bottom View

NOTE: All linear dimensions are in millimeters

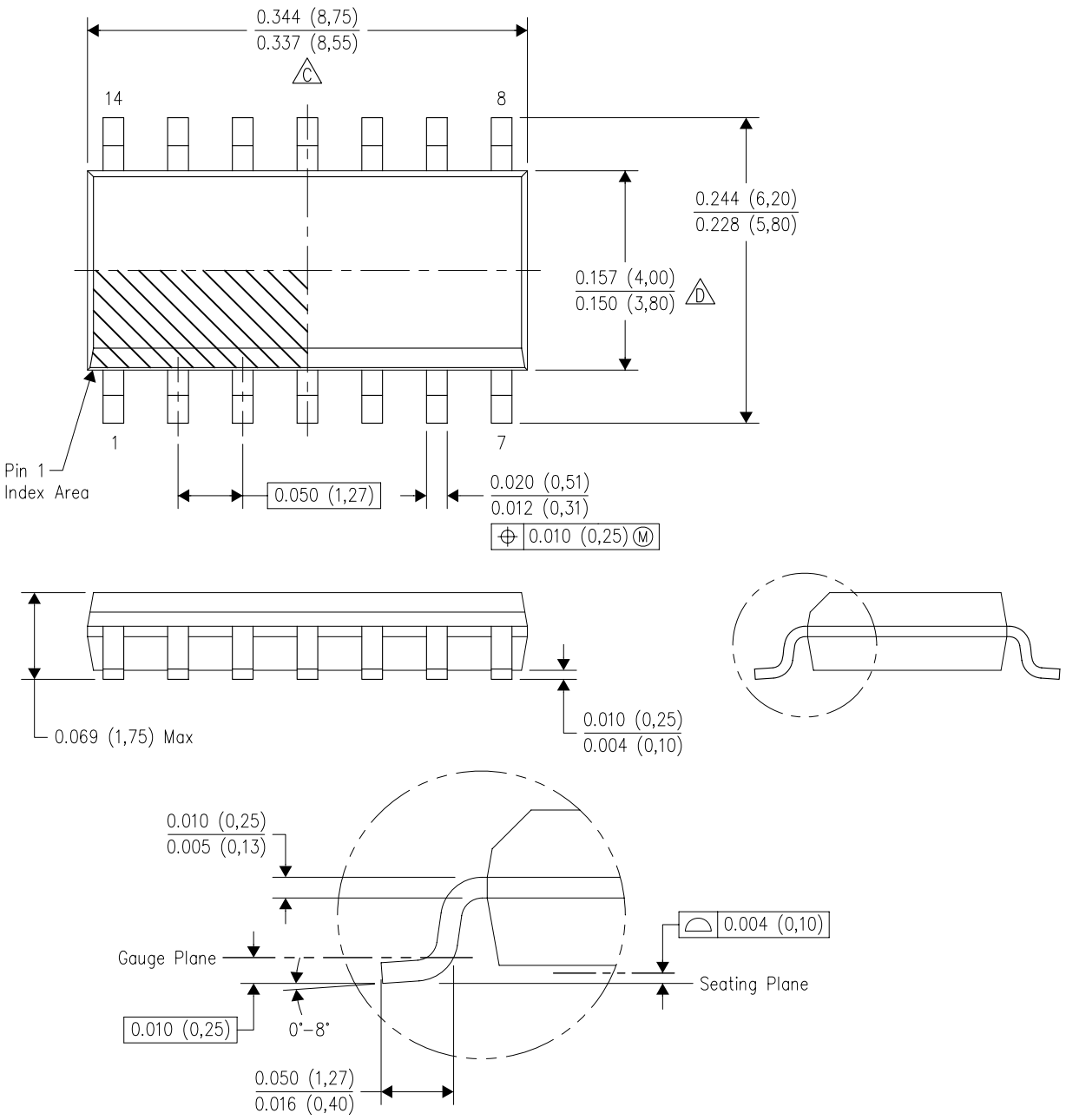
Exposed Thermal Pad Dimensions

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE



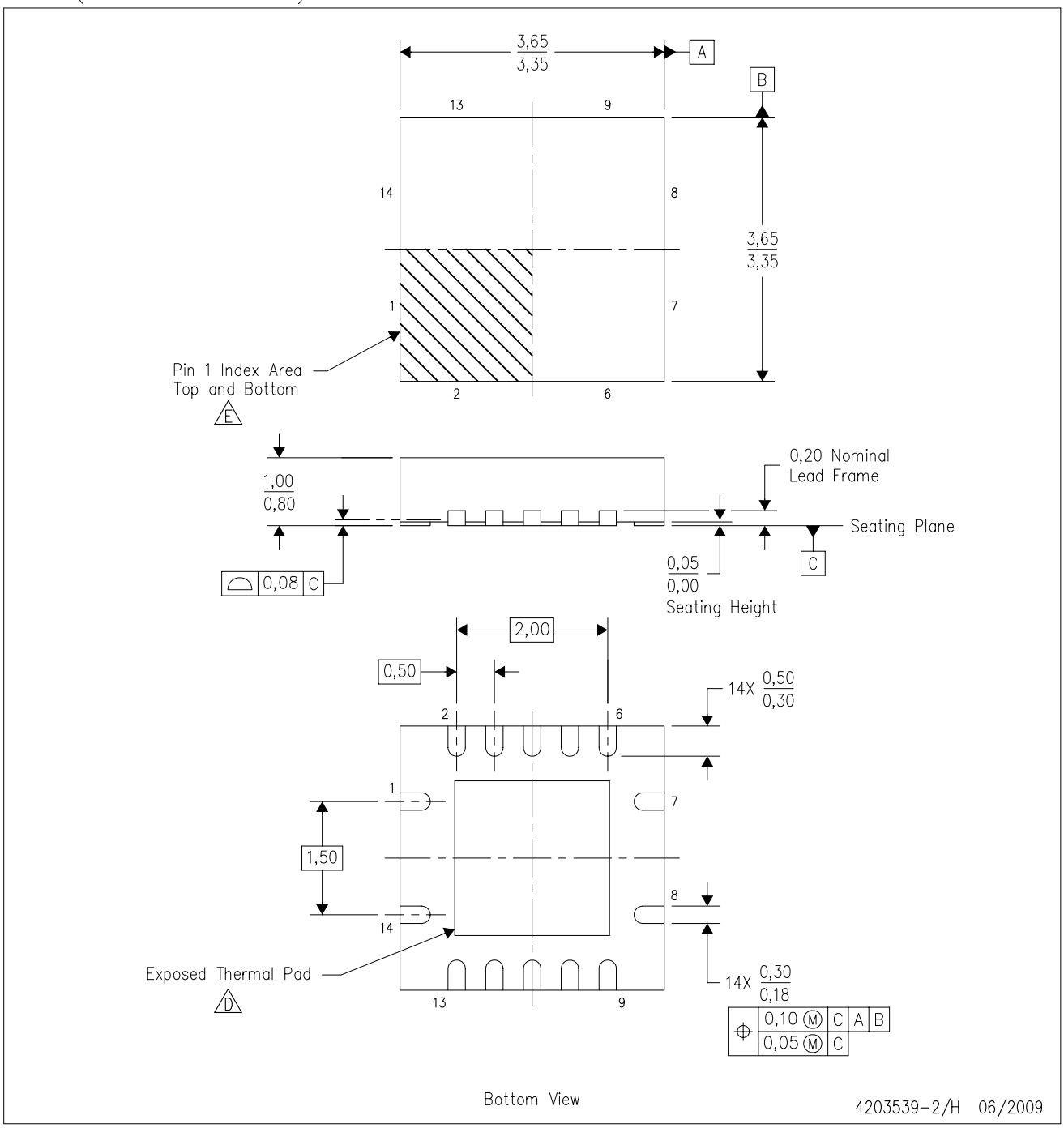
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



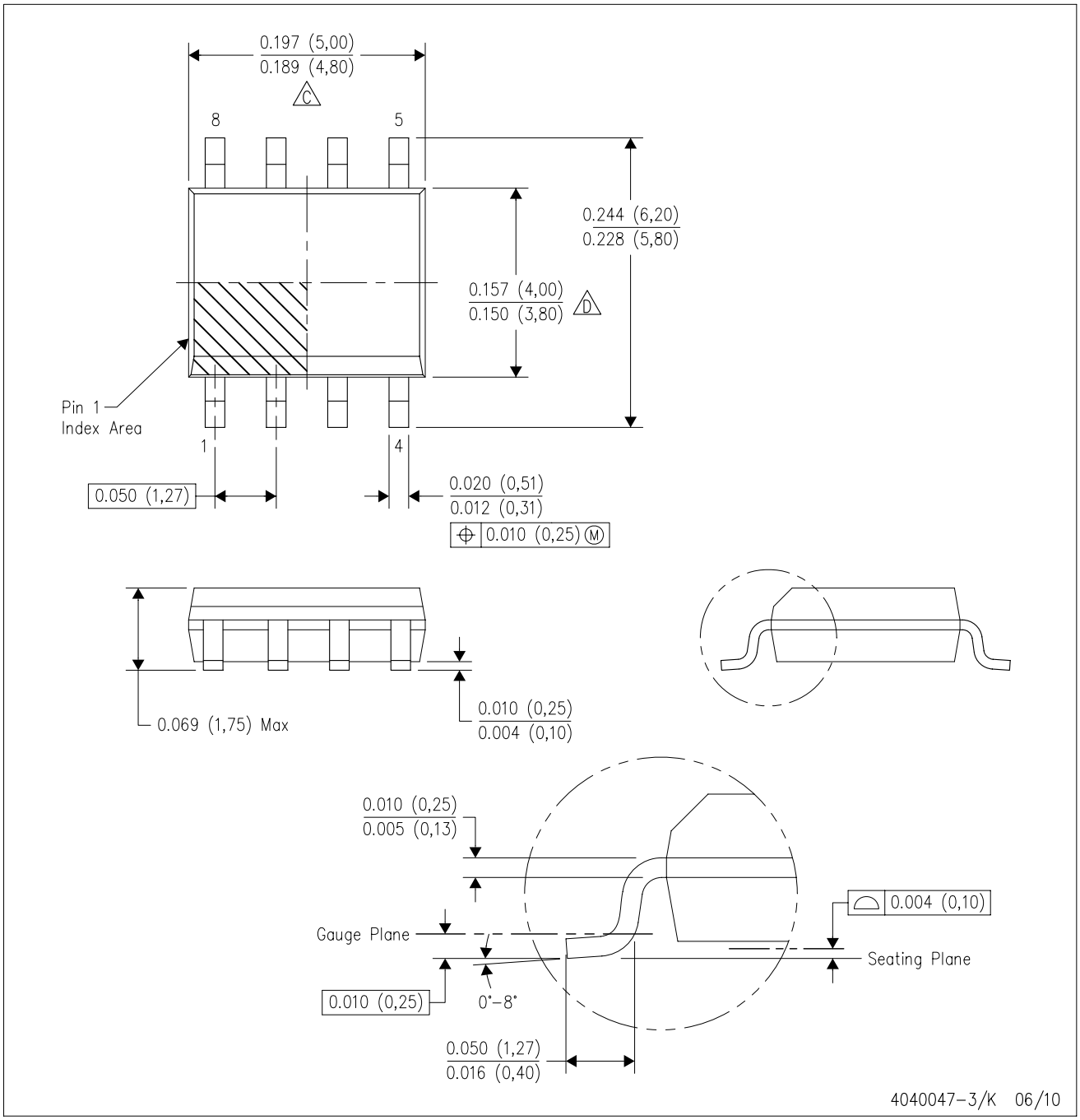
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BA.

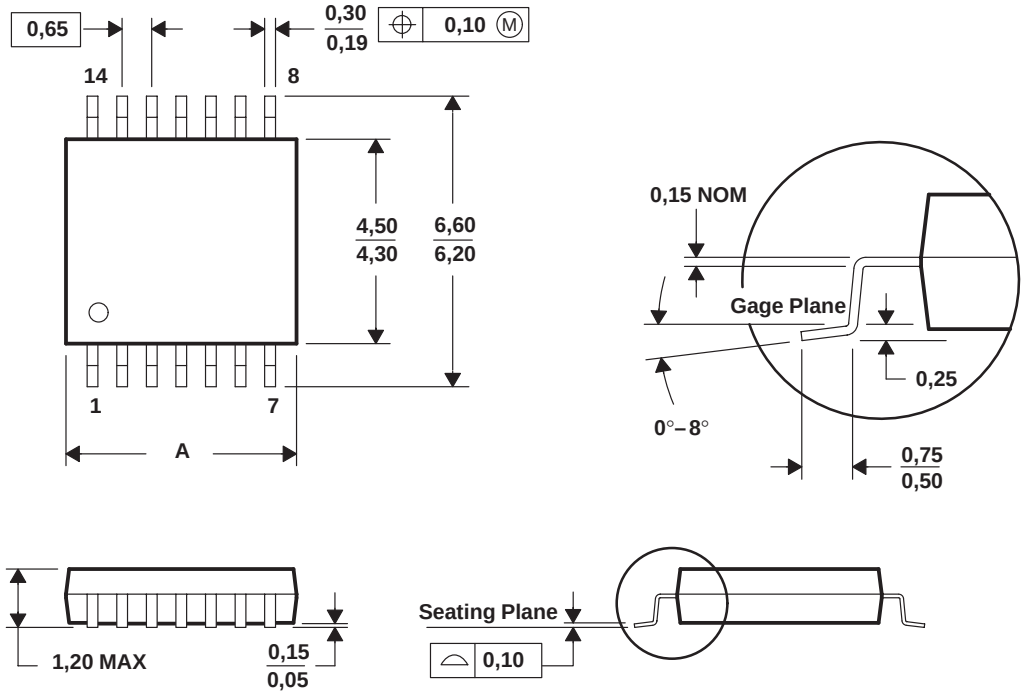
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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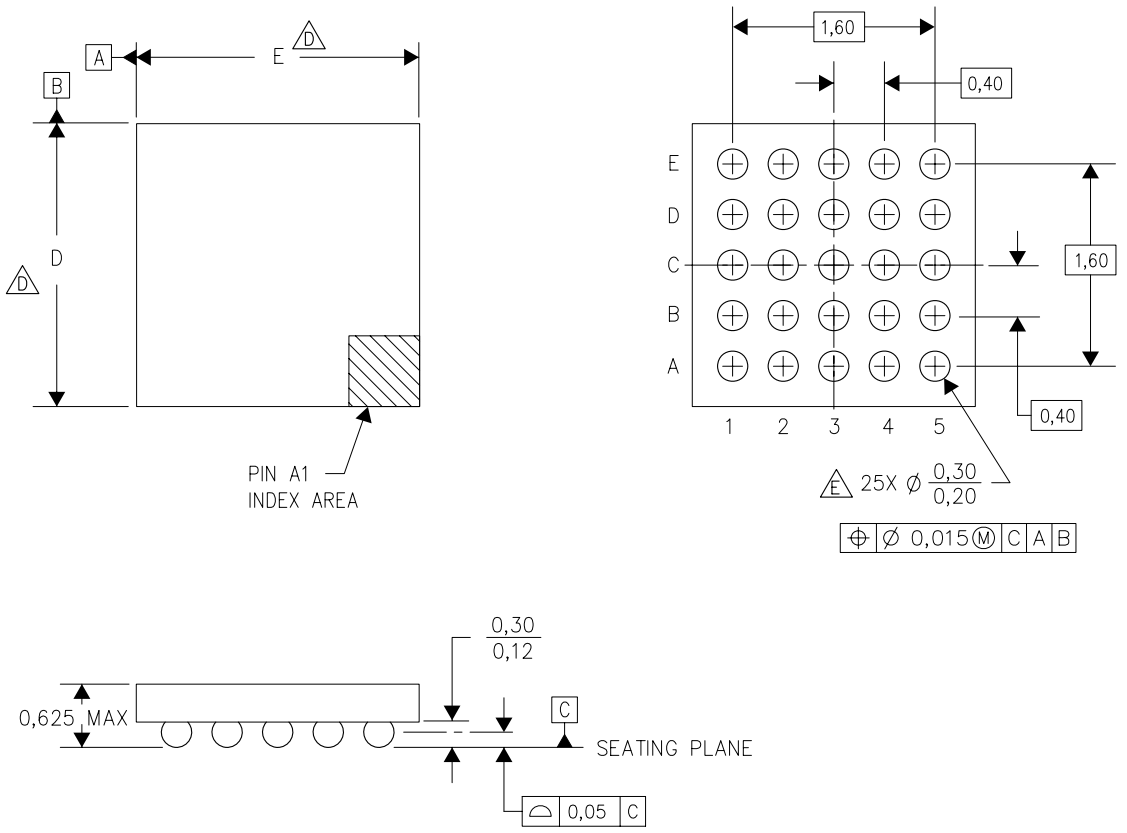
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

YFF (S–XBGA–N25) DIE–SIZE BALL GRID ARRAY



4207625–10/Y 05/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YFF package can have dimension D ranging from 1.96 to 2.65 mm and dimension E ranging from 1.96 to 2.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 5 x 5 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

NanoFree is a trademark of Texas Instruments.

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