➡ Examples:

Hardware design (VHDL, Verilog)

✓ Used by semi-conductor companies such as Intel

Critical embedded software (B/Z, Lustre/Esterel)

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(METEOR Metro Line 14 in Paris by Alstom)

✓ Rail transportation (Eurostar)

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Formal Methods of Verification

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Pros and cons of using formal methods

✓ Nothing better than a mathematical proof

➡ A code "proven safe" is safe

◉ Development is time and effort (and so money) consuming

➡ Should be motivated by the risk analysis

◉ Do not prevent from specification bugs

➡ Example of network protocols