Greta Oto Register and Control Interface

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1. Memory mapping

The Greta Oto GNSS receiver baseband occupies totally 64kB address space. All read and write operations are 32bit access without byte enable. Access to the first 32kB of address space will read/write registers and the second 32kB for RAM access. In the register space mapping, each module occupies 4kB of address space. The address mapping is shown in the following table:

Address offset	Module	Note
0x0000~0x0FFF	Global Registers	
0x1000~0x1FFF	Reserved	
0x2000~0x2FFF	Reserved	
0x3000~0x3FFF	Reserved	
0x4000~0x4FFF	Acquire Engine	
0x5000~0x5FFF	TE FIFO	
0x6000~0x6FFF	Tracking Engine	
0x7000~0x7FFF	Accessory	for PPS etc.
0x8000~0x8FFF	TE State Buffer	4kB for 32 channels, expandable
0xC000~0xCFFF	AE Configure Buffer	
Others	Reserved	

Data field in registers access mode can be one of the following: RO (read only), R/W (read write), R/W1C (read and write 1 to clear, typically used in interrupt registers), WTRIG (write 1 to trigger action, typically used for reset or trigger events).

2. Global registers

The name, offset and field definition for global registers are listed in following tables:

BB_ENABLE - 0x00

Bit	Mode	Name	Default	Description
31:9	-	-	23'h0	Reserved
8	R/W	TRACKING_ENGINE_ENABLE	1'b0	Enable flag of tracking engine system 0: Tracking engine is disabled, will also disable TE FIFO. 1: Tracking engine is enabled, will also enable TE FIFO.
7:0	-	-	8'h0	Reserved

BB_RESET - 0x04

Bit	Mode	Name	Default	Description
31:9	-	-	23'h0	Reserved
8	WTRIG	TE_FIFO_RESET	1'b0	Reset TE FIFO Write: 0: No effect

Bit	Mode	Name	Default	Description
				1: Reset TE FIFO
7:2	-	-	6'h0	Reserved
1	WTRIG	TRACKING_ENGINE _RESET	1'b0	Write: 0: No effect. 1: Reset tracking engine
0	WTRIG	ACQUIRE_ENGINE_ RESET	1'b0	Write: 0: No effect. 1: Reset acquire engine

FIFO_CLEAR - 0x08

Bit	Mode	Name	Default	Description
31:9	-	-	23'h0	Reserved
9	WTRIG	PPS_LATCH	1'b0	Latch PPS counter Write: 0: No effect 1: Latch PPS clock and pulse counter
8	WTRIG	TE_FIFO_CLEAR	1'b0	Clear bit for TE FIFO Write: 0: No effect 1: Clear TE FIFO
7:1	-	-	7'h0	Reserved
0	WTRIG	TE_FIFO_LATCH	1'b0	Latch TE FIFO write address Write: 0: No effect 1: Latch TE FIFO write address

TRACKING_START - 0x0c

Bit	Mode	Name	Default	Description
31:1	-	-	31'h0	Reserved
0	R/W	TRACKING_START	1'b0	Start/resume tracking engine Read: 0: tracking engine is waiting CPU 1: tracking engine is working Write: 0: No effect 1: Start/resume tracking engine

MEASUREMENT_NUMBER - 0x10

Bit	Mode	Name	Default	Description
31:10	-	-	22'h0	Reserved
9:0	R/W	MEAS_NUMBER	10'h0	Number of blocks of data to process between measurement interrupts. For 1ms block data and 1Hz measurement, this register set to 1000.

MEASUREMENT_COUNT - 0x14

Bit	Mode	Name	Default	Description
31:10	-	-	22'h0	Reserved
9:0	R/W	MEAS_COUNT	10'h0	Counter for measurement number to generate interrupt.

INTERRUPT_FLAG - 0x18

Bit	Mode	Name	Default	Description
31:12	-	-	20'h0	Reserved
11	R/W1C	AE_INT_FLAG	1'b0	AE interrupt flag
10	R/W1C	REQ_INT_FLAG	1'b0	Request interrupt flag
9	R/W1C	MEAS_INT_FLAG	1'b0	Measurement interrupt flag
8	R/W1C	DATA_READY_INT_FLAG	1'b0	Interrupt flag indicate whether tracking engine has coherent data ready
7:0	-	-	8'h0	Reserved

REQUEST_COUNT - 0x1c

Bit	Mode	Name	Default	Description
31:1	-	-	31'h0	Reserved
9:0	R/W	REQ_COUNT	10'h0	Request interrupt counter. Will be decreased 1 if this is not zero at the same cycle MEASUREMENT_COUNT change. If it decreased to zero, the interrupt flag will be set. If host write at the same cycle when hardware decrease this value, host write takes effect.

INT_MASK - 0x20

Bit	Mode	Name	Default	Description
31:12	-	-	20'h0	Reserved
11	R/W1C	AE_INT_MASK	1'b0	AE interrupt mask
10	R/W1C	REQ_INT_MASK	1'b0	Request interrupt mask
9	R/W1C	MEAS_INT_MASK	1'b0	Measurement interrupt mask
8	R/W1C	DATA_READY_INT_MASK	1'b0	Interrupt mask indicate whether tracking engine has coherent data ready
7:0	-	-	8'h0	Reserved

BB_VERSION - 0x40

Bit	Mode	Name	Default	Description
31:24	RO	MAJOR_VERSION	8'h1	Major version
23:16	RO	MINOR_VERSION	8'h0	Minor version
15:0	RO	RELEASE_VERSION	16'h?	Release version

3. Acquisition engine

The name, offset and field definition for AE registers are listed in following tables:

Revision 1.0

AE_CONTROL– 0x04

Bit	Mode	Name	Default	Description
31:9	-	-	23'h0	Reserved
8	WTRIG	START_ACQ	1'b0	Start acquisition
7:6	-	-	2'b0	Reserved
5:0	R/W	CHANNEL_NUMBER	6'h0	Number of channels to do acquisition, valid range 1~32

AE_BUFFER_CONTROL – 0x08

Bit	Mode	Name	Default	Description
31:10	-	-	22'h0	Reserved
9	WTRIG	RESET_RATE_ADAPTOR	1'b0	Reset registers in rate adaptor
8	WTRIG	START_FILL_BUFFER	1'b0	Start fill AE buffer.
7	-	-	1'b0	Reserved
6:0	R/W	BUFFER_THRESHOLD	7'h0	Length of AE buffer threshold indicator in unit of 1kB. When AE buffer filled to this threshold, REACH_THRESHOLD indicator will be set.

AE_STATUS – 0x0c

Bit	Mode	Name	Default	Description
31:20	-	-	12'h0	Reserved
19	R	AE_FINISH	1'b0	Clear when start acquisition and set when acquisition finished.
18	R	AE_BUFFER_FULL	1'b0	Clear when start to fill AE buffer and set when AE buffer is full.
17	R	AE_BUFFER_REACH_TH	1'b0	Clear when start to fill AE buffer and set when AE buffer filled to threshold.
16	R	AE_BUFFER_FILLING	1'b0	Clear when start to fill AE buffer and set when AE buffer is filling.
15:9	-	-	7'h0	Reserved
8:4	R	AE_CURRENT_CHANNEL	5'h0	Current channel AE is doing.
3:0	R	AE_CURRENT_STATE	4'h0	Current value of AE FSM.

AE_CARRIER_FREQ – 0x10

Bit	Mode	Name	Default	Description
31:0	R/W	CARRIER_FREQ	32'h0	Carrier frequency of code rate adaptor. Calculated by $f_{IF}/fs*2^{32}$.

AE_CODE_RATIO – 0x14

Bit	Mode	Name	Default	Description
31:24	-	-	8'h0	Reserved

Bit	Mode	Name	Default	Description
23:0	R/W	CODE_RATE_RATIO	24'h0	Code rate decimation ratio. Calculated by fc/fs*2^{24}. In which fs is source sample rate, fc is twice of code rate for GPS/BDS and 16x code rate for GLONASS.

AE_THRESHOLD – 0x18

Bit	Mode	Name	Default	Description
31:8	-	-	24'h0	Reserved
7:0	R/W	QUANT_THRESHOLD	8'd37	Threshold for quantization

4. TE FIFO

The name, offset and field definition for TE FIFO registers are listed in following tables:

TE_FIFO_CONFIG – 0x00

Bit	Mode	Name	Default	Description
31:9	-	-	23'h0	Reserved
8	R/W	TRIG_SOURCE	1'b0	Source FIFO to trigger. If multiple sources are selected, trigger will be effect whichever source send trigger signal. If this field set to 0 or only self is selected as source, trigger will NEVER happen.
7:3	-	-	5'h0	Reserved
2	WTRIG	FIFO_CLEAR	1'h0	Write: 0: No effect. 1: Force clear FIFO.
1	R/W	FIFO_TRIG	1'h0	Read: 0: FIFO is not waiting trigger from source 1: FIFO is waiting trigger from source Write: 0: No effect 1: Force FIFO goes into disable state and start waiting trigger from source
0	R/W	DUMMY_WRITE	1'h0	0: disable FIFO dummy write 1: enable FIFO dummy write

TE_FIFO_STATUS – 0x04

Bit	Mode	Name	Default	Description
31:3	-	-	29'h0	Reserved
2	RO	FIFO_ENABLED	1'h0	Read/ Write:

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Bit	Mode	Name	Default	Description
				0: FIFO is enabled and running 1: FIFO is not running
1	RO	GUARD_ALARM_FLAG	1'h0	Read/ Write: 0: FIFO overflow guard alarm flag negative 1: FIFO overflow guard alarm flag positive
0	R/W1C	OVERFLOW_FLAG	1'h0	Read: 0: FIFO overflow flag negative 1: FIFO overflow flag positive Write: 0: No effect 1: Clear FIFO overflow flag

TE_FIFO_GUARD – 0x10

Bit	Mode	Name	Default	Description
31:16	-	-	16'h0	Reserved
15:0	R/W	FIFO_GUARD_TH	16'h0	The threshold of alarming FIFO is going to overflow. In the unit of sample. Write will align to multiple of 256 (force 8LSB to be 0).

TE_FIFO_READ_ADDR – 0x14

Bit	Mode	Name	Default	Description
31:14	-	-	16'h0	Reserved
13:0	RO	READ_ADDR	16'h0	Current FIFO read address. Address in unit of sample.

TE_FIFO_WRITE_ADDR – 0x18

Bit	Mode	Name	Default	Description
31:20	RO	WRITE_ADDR_ROUND	12'h0	Current round number of FIFO write address.
19:6	RO	WRITE_ADDR	14'h0	Current FIFO write address. Address in unit of sample.
5:0	-	-	6'h0	Reserved

TE_FIFO_BLOCK_SIZE – 0x28

Bit	Mode	Name	Default	Description
31:16	-	-	16'h0	Reserved
15:0	R/W	CLUSTER_NUM	16'h0	Number of clusters to read from FIFO.

TE_FIFO_BLOCK_ADJUST – 0x2c

Bit	Mode	Name	Default	Description

Bit	Mode	Name	Default	Description
31:8	-	-	24'h0	Reserved
7:0	R/W	FIFO_BLOCK_ADJUST	8'h0	FIFO block size adjust control register, adjustment in unit of cluster, this value is signed integer.

TE_FIFO_LWADDR_CPU – 0x40

Bit	Mode	Name	Default	Description
31:20	RO	LATCHED_WRITE_ADDR_ROUND	12'h0	CPU latched current round number of FIFO write address.
19:6	RO	LATCHED_WRITE_ADDR	14'h0	CPU latched FIFO write address.
5:0	RO	LATCHED_WRITE_ADDR_SUB	6'h0	CPU latched system clock count between two samples.

TE_FIFO_LWADDR_EM – 0x44

Bit	Mode	Name	Default	Description
31:20	RO	LATCHED_WRITE_ADDR_ROUND	12'h0	Event mark latched current round number of FIFO write address.
19:6	RO	LATCHED_WRITE_ADDR	14'h0	Event mark latched FIFO write address.
5:0	RO	LATCHED_WRITE_ADDR_SUB	6'h0	Event mark latched system clock count between two samples.

TE_FIFO_LWADDR_PPS – 0x48

Bit	Mode	Name	Default	Description
31:20	RO	LATCHED_WRITE_ADDR_ROUND	12'h0	PPS latched current round number of FIFO write address.
19:6	RO	LATCHED_WRITE_ADDR	14'h0	PPS latched FIFO write address.
5:0	RO	LATCHED_WRITE_ADDR_SUB	6'h0	PPS latched system clock count between two samples.

TE_FIFO_LWADDR_AE – 0x4c

Bit	Mode	Name	Default	Description
31:20	RO	LATCHED_WRITE_ADDR_ROUND	12'h0	AE latched current round number of FIFO write address.
19:6	RO	LATCHED_WRITE_ADDR	14'h0	AE latched FIFO write address.
5:0	RO	LATCHED_WRITE_ADDR_SUB	6'h0	AE latched system clock count between two samples.

5. Tracking Engine

The name, offset and field definition for TE registers are listed in following tables:

Revision 1.0

TE_CHANNEL_ENABLE – 0x00

Bit	Mode	Name	Default	Description
31:0	R/W	TE_CHANNEL_ENABLE	32'h0	Read/ Write: Enable flag of each logic channel, bit0 corresponds to channel0, etc. 0: Corresponding channel is disabled 1: Corresponding channel is enabled

TE_COH_DATA_READY – 0x04

Bit	Mode	Name	Default	Description
31:0	R/W	TE_COH_DATA_READY	32'h0	Read/ Write: Coherent data ready flag of each logic channel, bit0 corresponds to channel0, etc. Any correlator reach coherent number will set this flag. 0: Corresponding channel has not reached coherent number yet 1: Corresponding channel has coherent data ready to read

TE _OVERWRITE_PROTECT_CHANNEL – 0x08

Bit	Mode	Name	Default	Description
31:0	R/W	TE_CHANNEL_OVERWRITE_PROTECT	32'h0	Read/ Write: Coherent data overwrite protect flag of each logic channel, bit0 corresponds to channel0, etc. Any correlator has overwrite protect will set this flag. 0: Corresponding channel has not overwrite protect 1: Corresponding channel has overwrite protect

TE_OVERWRITE_PROTECT_ADDR – 0x10

Bit	Mode	Name	Default	Description
31:12	-	-	20'h0	Reserved
11:0	RO	OVERWRITE_PROTECT_ADDR	12'h0	Coherent address that protected by overwrote

TE_OVERWRITE_PROTECT_VALUE – 0x14

Bit	Mode	Name	Default	Description
31:16	RO	OVERWRITE_PROTECT_VALUE_I	16'h0	Overwrite protect value I

Bit	Mode	Name	Default	Description
15:0	RO	OVERWRITE_PROTECT_VALUE_Q	16'h0	Overwrite protect value Q

TE_POLYNOMIAL – 0x20

Bit	Mode	Name	Default	Description
31	R/W	SERIAL_PARALLEL	1'b0	Serialize/parallel select 0: 2 parallel Gold code generation 1: 1 serialize feedback shift registers
30:28	-	-	3'h0	Reserved
27:14	RW	G2_POLYNOMIAL	14'h0	Polynomial of G2 in preset code generator setting0
13:0	R/W	G1_POLYNOMIAL	14'h0	Polynomial of G1 in preset code generator setting0

TE_CODE_LENGTH – 0x24

Bit	Mode	Name	Default	Description
31:14	R/W	GLOBAL_LENGTH	18'h0	Global code length For serialize, all 32bit is used as global length.
13:0	R/W	G1_LENGTH	14'h0	Code length of G1 generator

TE_POLYNOMIAL2 – 0x28

Bit	Mode	Name	Default	Description
31	R/W	SERIAL_PARALLEL	1'b0	Serialize/parallel select 0: 2 parallel Gold code generation 1: 1 serialize feedback shift registers
30:28	-	-	3'h0	Reserved
27:14	RW	G2_POLYNOMIAL	14'h0	Polynomial of G2 in preset code generator setting0
13:0	R/W	G1_POLYNOMIAL	14'h0	Polynomial of G1 in preset code generator setting0.

TE_CODE_LENGTH2 – 0x2c

Bit	Mode	Name	Default	Description
31:14	R/W	GLOBAL_LENGTH	18'h0	Global code length. For serialize, all 32bit is used as global length
13:0	R/W	G1_LENGTH	14'h0	Code length of G1 generator

TE_NOISE_CONFIG – 0x30

Bit	Mode	Name	Default	Description
31:2	-	-	30'h0	Reserved
1:0	R/W	NOISE_SMOOTH	2'b00	Smooth factor of noise floor

Bit	Mode	Name	Default	Description
				00 – 1/256
				01 – 1/1024
				10 – 1/4096
				11 – 1/16384

TE_NOISE_FLOOR – 0x34

Bit	Mode	Name	Default	Description
31:16	-	-	16'h0	Reserved
15:0	R/W	NOISE_FLOOR	16'd784	Noise floor

6. PPS

The name, offset and field definition for PPS registers are listed in following tables:

PPS_CTRL – 0x00

Bit	Mode	Name	Default	Description
31:2	-	-	30'h0	Reserved
1	R/W	INT_ENABLE	1'b0	Enable PPS pulse interrupt
0	R/W	PPS_ENABLE	1'b0	Enable PPS function

PPS_EM_CTRL – 0x04

Bit	Mode	Name	Default	Description
31:2	-	-	30'h0	Reserved
1	R/W	EM_POLAR	1'b0	event mark trigger edge, 0 for rising edge, 1 for falling edge
0	R/W	EM_ENABLE	1'b0	Enable event mark latch

PPS_PULSE_INTERVAL – 0x08

Bit	Mode	Name	Default	Description
31:30	-	-	2'b00	Reserved
29:0	R/W	PULSE_INTERVAL	30'h0	Number of PPS clock cycles between PPS counter events

PPS_PULSE_ADJUST – 0x0c

Bit	Mode	Name	Default	Description
31:30	-	-	2'b00	Reserved
29:0	W	PULSE_ADJUST	30'h0	Adjust to PPS_PULSE_FREQ. This value is a signed value. When written, the corresponding value will be used to adjust to PPS event interval once and then be cleared.

PPS_PULSE_CTRL1 – 0x10

Bit	Mode	Name	Default	Description
31:18	-	-	14'h0	Reserved
17	R/W	PULSE_POLAR	1'b0	Pulse polarity, 0 for rising edge as pulse epoch, 1 for falling edge as pulse epoch
16	R/W	PULSE_ENABLE	1'b0	Pulse output enable
15:0	R/W	PULSE_DELAY	16'h0	Pulse delay to PPS counter event

PPS_PULSE_WIDTH1 – 0x14

Bit	Mode	Name	Default	Description
31:30	-	-	2'b00	Reserved
29:0	R/W	PULSE_ WIDTH	16'h0	Pulse width in number of PPS clock

PPS_PULSE_CTRL2 – 0x18

Bit	Mode	Name	Default	Description
31:18	-	-	14'h0	Reserved
17	R/W	PULSE_POLAR	1'b0	Pulse polarity, 0 for rising edge as pulse epoch, 1 for falling edge as pulse epoch
16	R/W	PULSE_ENABLE	1'b0	Pulse output enable
15:0	R/W	PULSE_DELAY	16'h0	Pulse delay to PPS counter event

PPS_PULSE_WIDTH2 – 0x1c

Bit	Mode	Name	Default	Description
31:30	-	-	2'b00	Reserved
29:0	R/W	PULSE_WIDTH	16'h0	Pulse width in number of PPS clock

PPS_PULSE_CTRL3 – 0x20

Bit	Mode	Name	Default	Description
31:18	-	-	14'h0	Reserved
17	R/W	PULSE_POLAR	1'b0	Pulse polarity, 0 for rising edge as pulse epoch, 1 for falling edge as pulse epoch
16	R/W	PULSE_ENABLE	1'b0	Pulse output enable
15:0	R/W	PULSE_DELAY	16'h0	Pulse delay to PPS counter event

PPS_PULSE_WIDTH3 – 0x24

Bit	Mode	Name	Default	Description
31:30	-	-	2'b00	Reserved
29:0	R/W	PULSE_ WIDTH	16'h0	Pulse width in number of PPS clock

PPS_CLK_COUNT_LATCH_CPU – 0x30

Bit	Mode	Name	Default	Description

Bit	Mode	Name	Default	Description
31	-	-	1'b0	Reserved
30:0	R	CLK_COUNT	31'h0	Clock counter latched at CPU trigger epoch

PPS_PULSE_COUNT_LATCH_CPU – 0x34

Bit	Mode	Name	Default	Description
31:8	-	-	24'h0	Reserved
7:0	R	PULSE_COUNT	8'h0	Pulse counter latched at CPU trigger epoch

PPS_CLK_COUNT_LATCH_EM – 0x38

Bit	Mode	Name	Default	Description
31	-	-	1'b0	Reserved
30:0	R	CLK_COUNT	31'h0	Clock counter latched at event mark trigger epoch

PPS_PULSE_COUNT_LATCH_EM – 0x3c

Bit	Mode	Name	Default	Description
31:8	-	-	24'h0	Reserved
7:0	R	PULSE_COUNT	8'h0	Pulse counter latched at event mark trigger epoch