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A Practical Guide to Configuring the Spartan-3A Family

Goals

- **Explain advantages and disadvantages of each configuration mechanism available for Spartan-3A**
- **Show how to use an industry standard flash for Spartan-3A configuration**
- **Describe the multi-boot feature and how to use it**
- **Introduce Spartan-3AN features**

Agenda

- **Introduction to configuration**
- **Features Spartan-3A shares with other Xilinx FPGAs**
- **Features Spartan-3A shares with Spartan-3E and Virtex-5**
- **Unique features exclusive to Spartan-3A**
- **Spartan-3AN**

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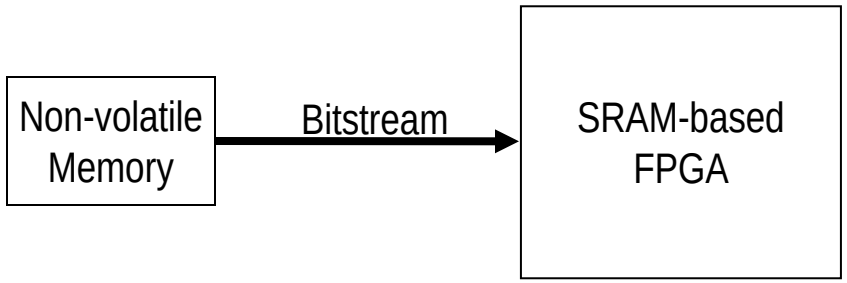
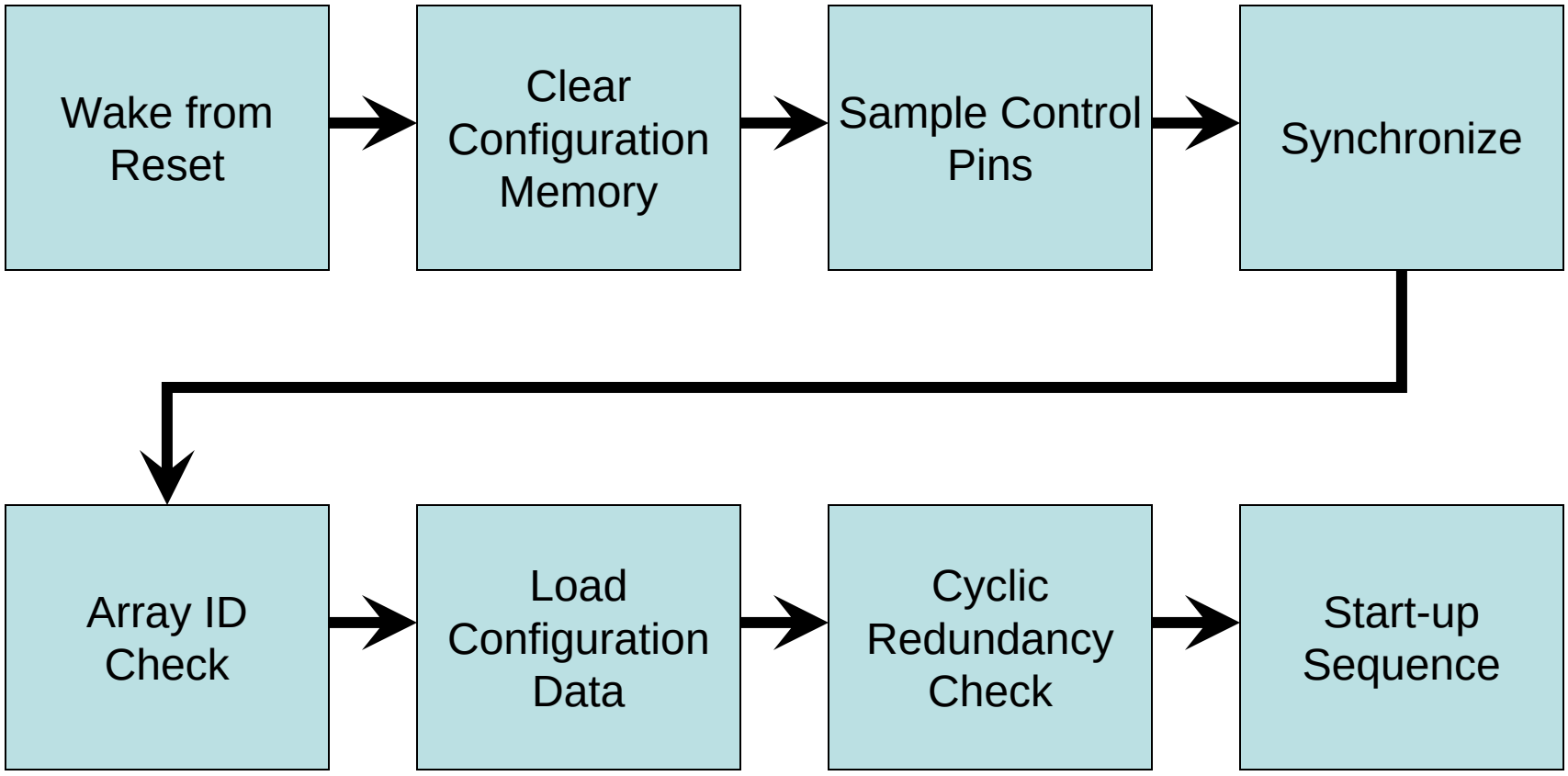
What Is Configuration?

- **When the FPGA is powered on, it has no identity**
- **"Configuration" is the process of loading the FPGA SRAM with an identity**
- **This identity is called a bitstream**



- **This can be done two ways**
  - –PC connection to the FPGA – Good for debug
  - –Non-volatile, on-board memory – Required for an embedded system

Configuration's Sequence of Events



Configuration Modes

- **MODE = Method by which the bitstream gets into the FPGA**
- **Set via three FPGA pins**
- **Mode determines**
  - Data port
  - Protocol
  - Clock source
    - Master = FPGA source
    - Slave = external source
- **Mode trade-offs**
  - configuration speed
  - cost
  - FPGA I/Os consumed
  - Ease of use

Spartan-3A Configuration Modes
Boundary Scan
Slave Serial
Master Serial
Slave Parallel
Master Byte Peripheral Interface (BPI)
Master Serial Peripheral Interface (SPI)

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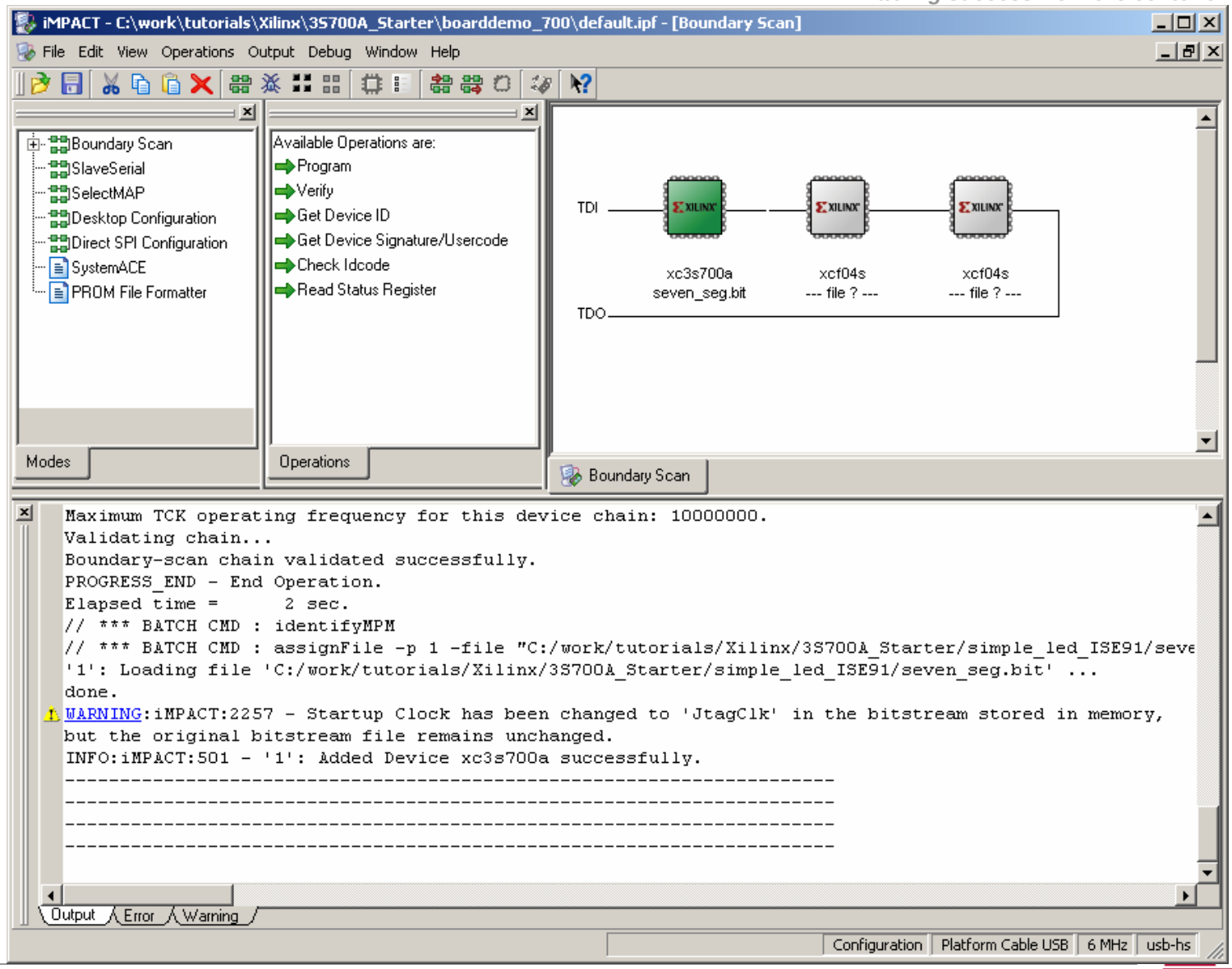
Xilinx Configuration Software

- **iMPACT, now at Version 9.1**
- **Both GUI and command-line versions**
- **Multiple functions**
  - Prepare programming files
  - Boundary-scan configuration of FPGAs
  - Programming Platform Flash PROMs
  - Programming SPI and parallel flash connected to FPGAs

Programming Software – iMPACT



Boundary Scan Mode Configuration

- **Option 1: Cable connected to FPGA's JTAG port**
  - Uses PC and Xilinx iMPACT software
  - Best environment for debugging
  - USB or parallel cables

- **Option 2: SystemACE CompactFlash (CF)**
  - Store bitstream on CompactFlash card
  - Xilinx SystemACE controller chip
    - Reads bitstream from CompactFlash
    - Transfers bitstream via boundary scan
  - Multiple bitstreams possible

Spartan-3A Configuration Modes
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Programming Cable Solutions

- **Parallel Cable IV - PC4**
  - Supports I/O down to 1.8V

- **Platform USB Cable**
  - Fast
  - USB 2.0 compliant
  - Supports I/O down to 1.5V

Avnet System ACE™ Module (SAM)

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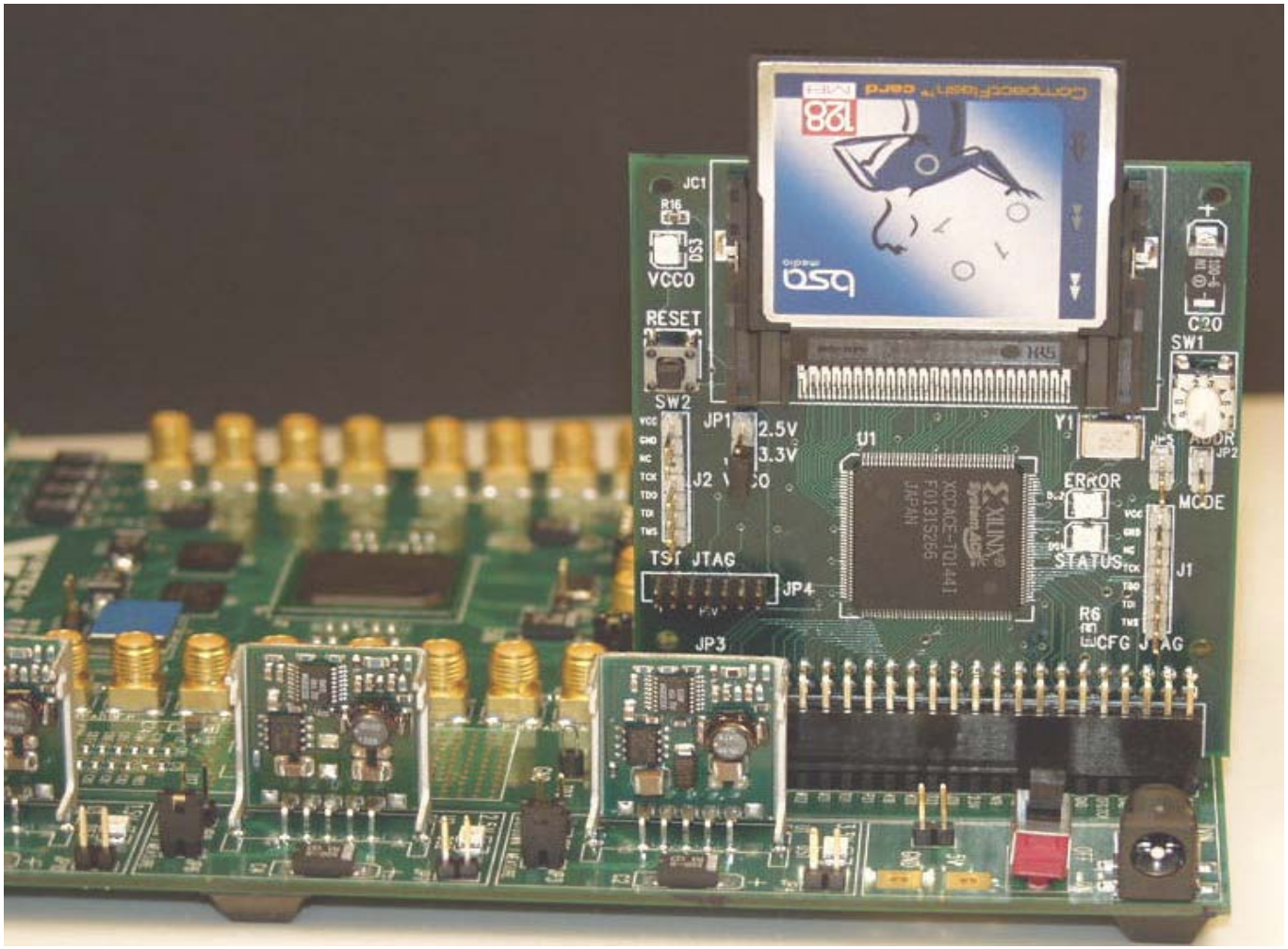

Serial Mode Configuration

- **Serial data interface**
- **Xilinx Platform Flash compatible**
- **Clock source**
  - Generated by FPGA in Master Serial Mode
  - External source in Slave Serial Mode

Spartan-3A Configuration Modes
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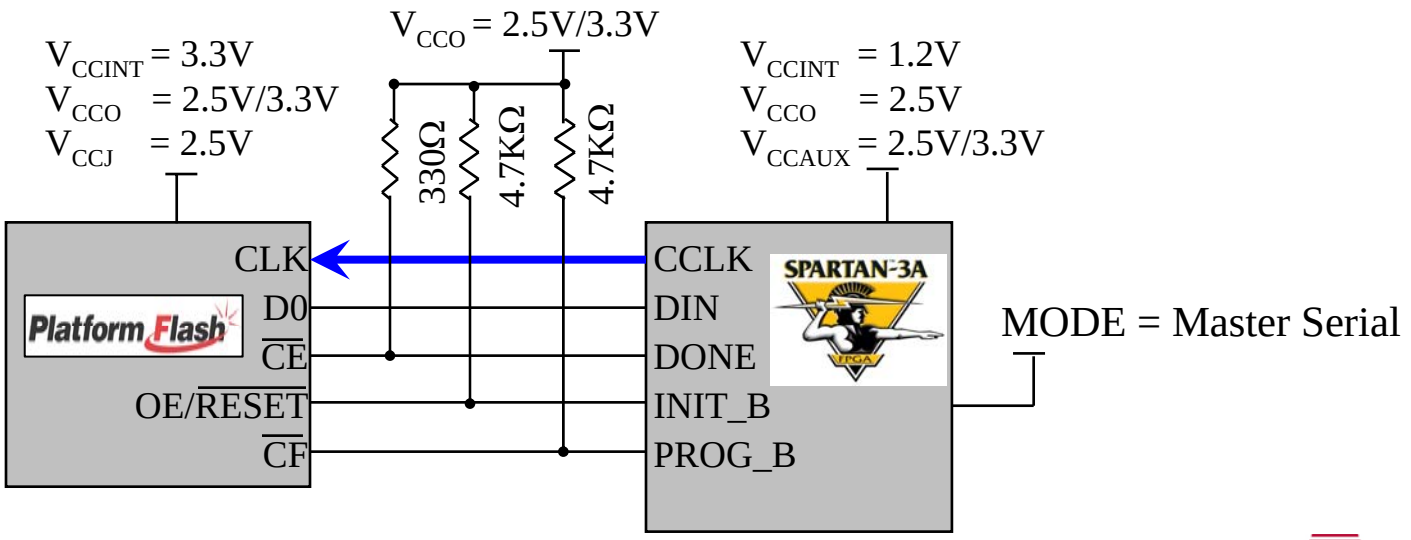

Slave Parallel Mode Configuration

- **Byte-wide interface**
- **Xilinx Platform Flash compatible**
- **External clock source**
  - Platform Flash
  - Processor
  - Oscillator

Spartan-3A Configuration Modes
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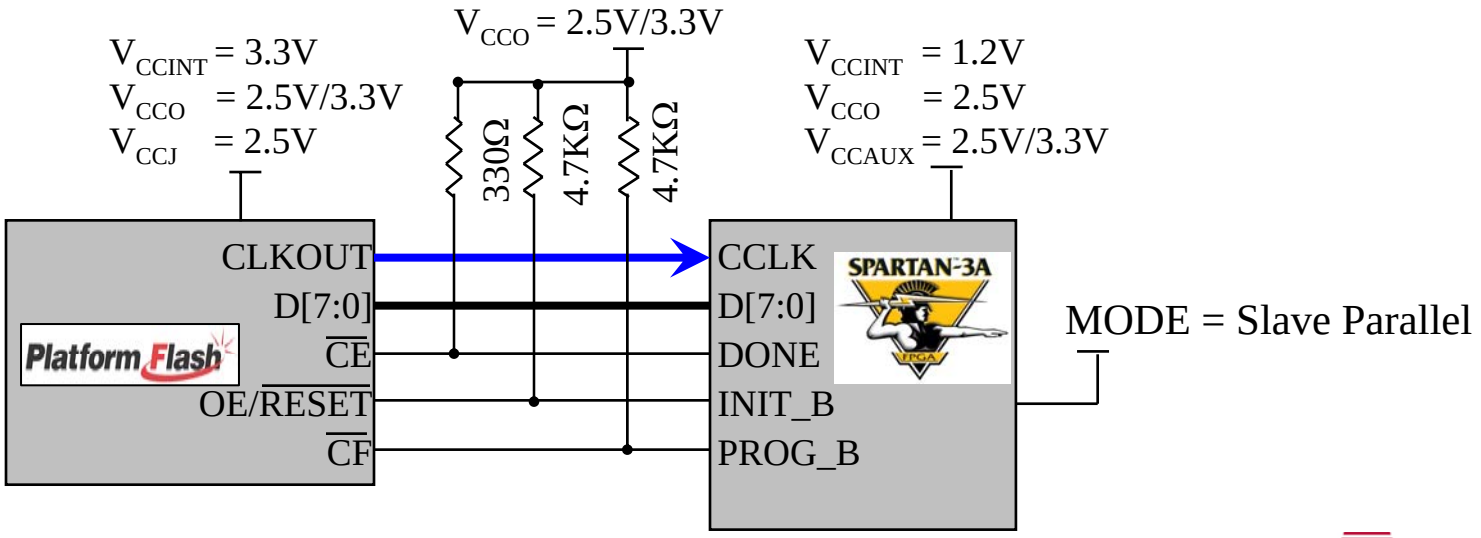

Platform Flash PROMs

- **Xilinx solution for configuration**
- **Easy to use and high speed**
- **Full Xilinx in-system programming support**

Advantages

- **Simplest hardware solution**
- **Easiest lab programming**
- **Parallel version has fastest configuration time**
- **Serial version has lowest possible I/O count**
- **Long production lifetime**

Disadvantages

- **More expensive per Mbit**
- **More difficult to access extra space post-configuration**
- **Maximum device density limited to 32 Mbit**

MicroProcessor Configuration

- **A microProcessor can configure the FPGA**
- **Use the serial or parallel configuration port**
- **Use external configuration clock with Slave mode**
- **Monitors FPGA configuration signals**
- **Bitstream can be embedded in software**

Agenda

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Master BPI Mode Configuration

- **Industry-standard parallel NOR flash**
  - Highest pin utilization
  - Ideal for embedded applications with flash already on-board
  - Memory easily accessible post-configuration
  - Board-tested with Intel StrataFlash

Spartan-3A Configuration Modes
Boundary Scan
Slave Serial
Master Serial
Slave Parallel
Master Byte Peripheral Interface (BPI)
Master Serial Peripheral Interface (SPI)

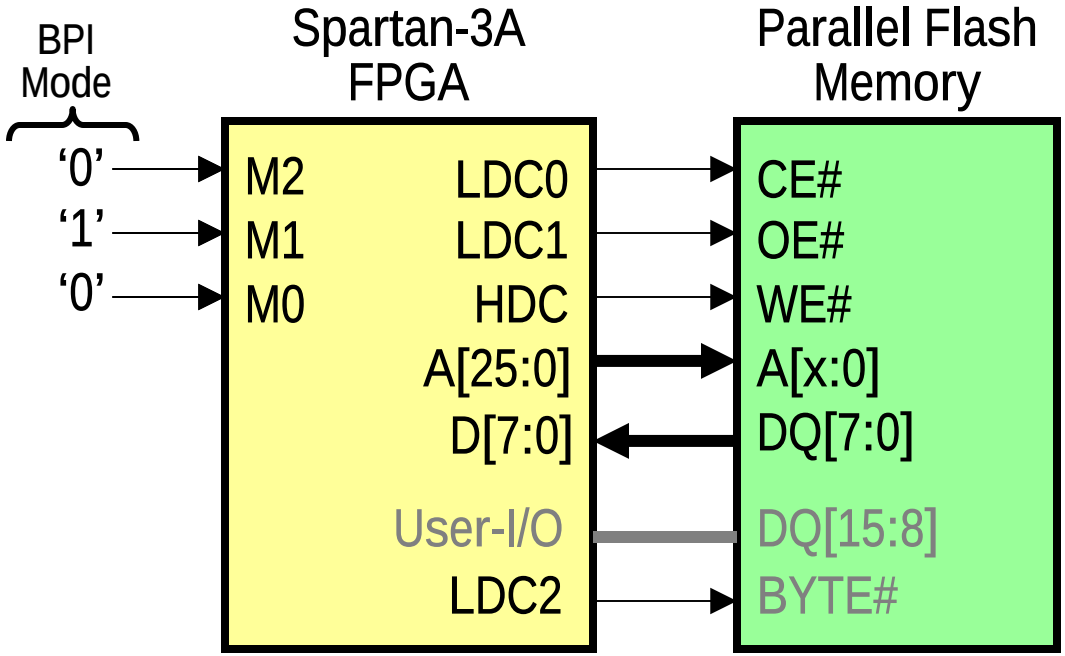
Advantages

- **Less expensive per Mbit**
- **High density – up to 512 Mb**
- **Random accessible, byte addressable**
- **Readable/writeable by FPGA user application**

Disadvantages

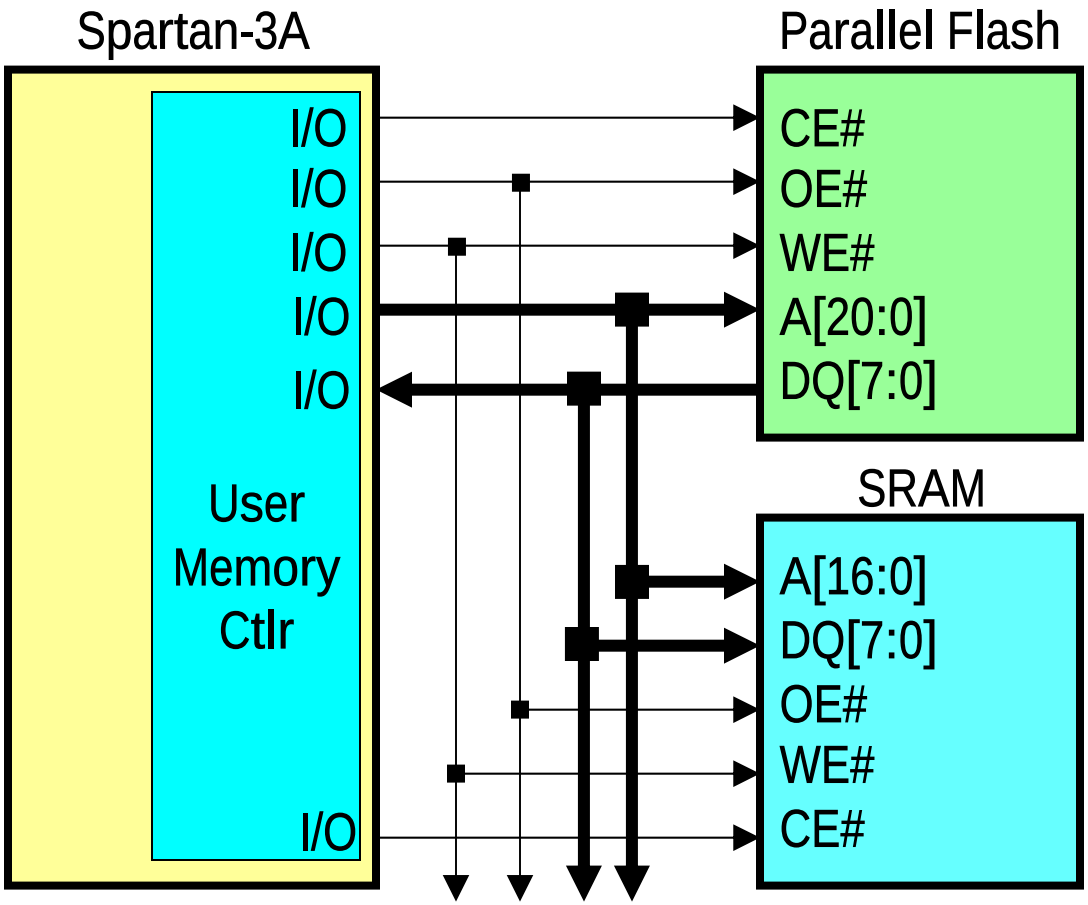
- **Shorter production lifetime**
- **No JTAG interface**
- **Slower data transfer**
- **More involved lab programming**
- **Requires a large number of FPGA I/Os**

BPI Interface



- **MODE = 0:1:0 enables BPI controller inside FPGA**
- **LDC = Low During Configuration**
- **HDC = High During Configuration**
- **LDC/HDC control enables during configuration**
- **Not supported in XC3S50A**
- **Spartan-3A does not have BPI-down mode**

BPI Flash Post-Configuration with SRAM



- **Shared address, data, and control pins uses dual-purpose configuration pins**
- **2-bank memory controller controls flash and SRAM**

Master SPI Mode Configuration

- **Industry-standard SPI flash**
  - Least expensive of any solution
  - 5 more I/Os than serial Platform Flash
  - Memory easily accessible post-configuration
  - Board-tested with Intel S33

Spartan-3A Configuration Modes
Boundary Scan
Slave Serial
Master Serial
Slave Parallel
Master Byte Peripheral Interface (BPI)
Master Serial Peripheral Interface (SPI)

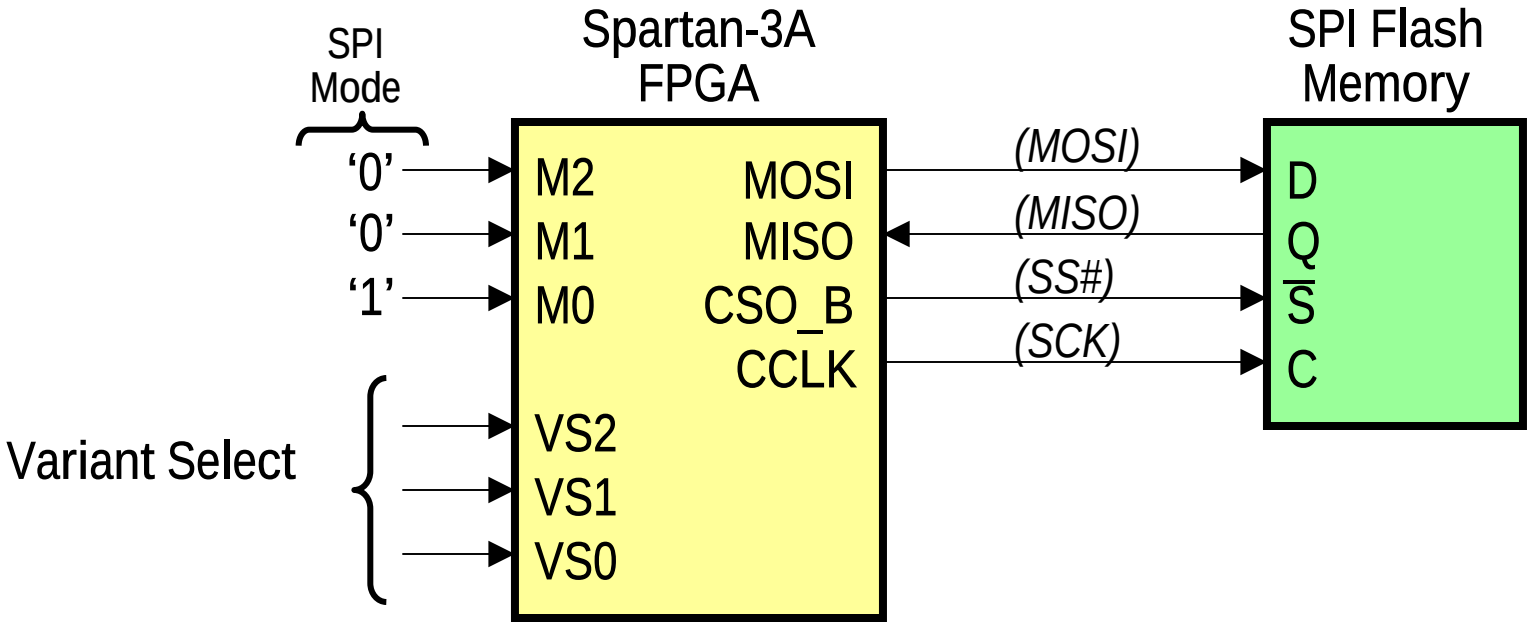
Advantages

- **Least expensive per Mbit**
- **High density – up to 128 Mb**
- **Random accessible, byte addressable**
- **Readable/writeable by FPGA user application**

Disadvantages

- **Shorter production lifetime**
- **No JTAG interface**
- **Slower data transfer**
- **More involved lab programming**
- **A few more I/Os**

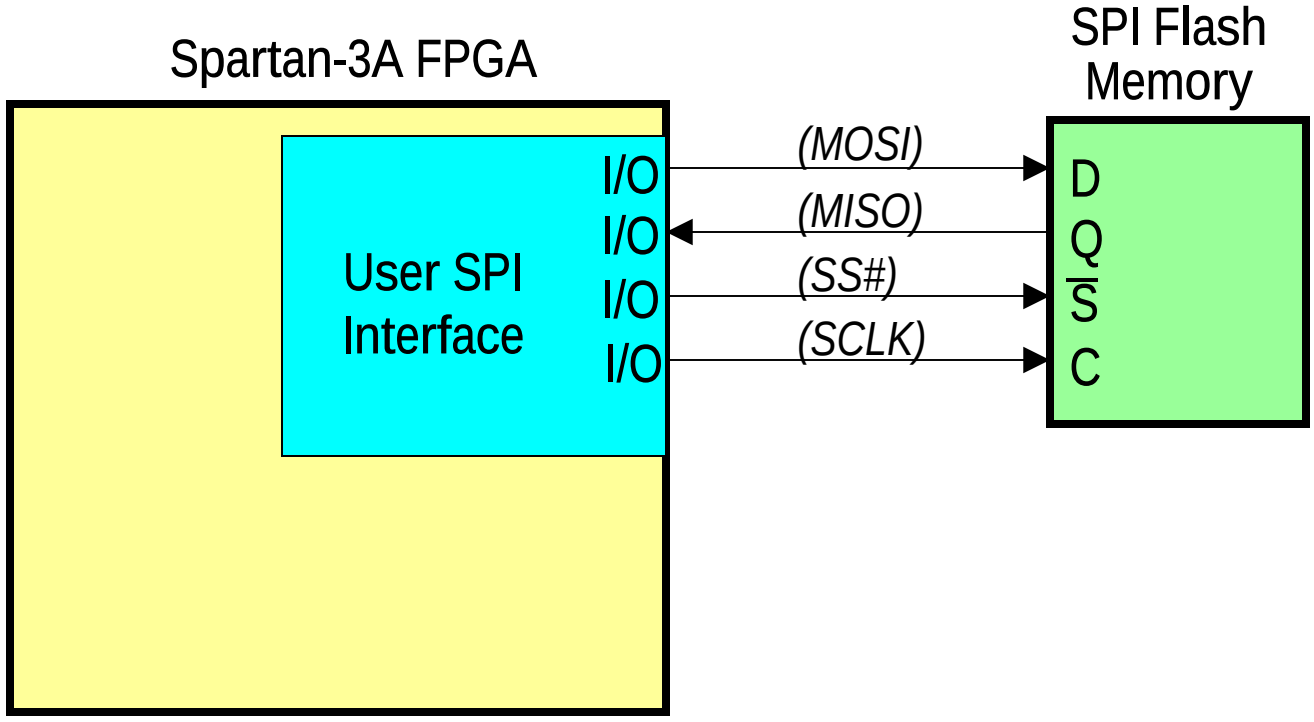
Master SPI Flash Interface



- **MODE = 0:0:1 enables SPI controller inside FPGA**
- **Variant Select pins determine the SPI read command used**
  - Refer to *Spartan-3 Generation Configuration User Guide*
    - Intel S33 VS = 111
    - ST Micro M25P VS = 111
    - Atmel AT45DBxxB VS = 110
    - etc.

SPI Flash Post-Configuration

- **SPI config pins become user I/Os after config**
- **Build SPI interface in FPGA**



Comparison Summary

	Platform Flash	SPI	BPI
Pins	7 (x1) or 14 (x8)	12	45
Mode	Serial or Parallel*	Serial Only	Parallel Only
Storage Density	1 – 32 Mbit	512K – 128 Mbit	512K – 512 Mbi
Sourcing	Xilinx only	Multiple	Multiple
Guaranteed Supply	Yes	No	No
Storage Cost	Low	Lowest	Low
User data read/write	Yes**	Yes	Yes
JTAG Interface	Yes	No	No
Power Reliability	Excellent	Fair	Fair
Xilinx Support	Excellent	Limited	Very Limited
ISE 8.2i Support	Excellent	Very Limited	None
ISE 9.1i Support	Excellent	Limited	Very Limited

*** Only with XCF08P, XCF16P, and XCF32P**

**** Read-Only using XAPP694/XAPP482 via configuration data port, Read/Write using XAPP544 via JTAG**

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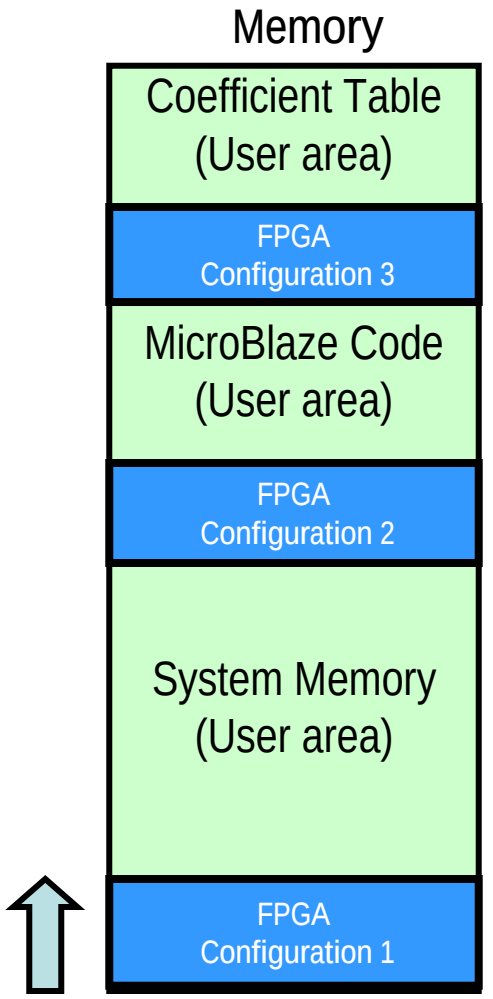
MultiBoot

- **MultiBoot allows the FPGA application to load one of multiple FPGA bitstreams**
- **The FPGA controls reconfiguration from a different bitstream stored in external memory**

- **How is it done?**
  - The FPGA configures the first time based on Mode pins
  - The FPGA application designates a new bitstream for configuration
  - The FPGA initiates a reconfiguration by asserting MultiBoot
  - The FPGA is reconfigured with new bitstream



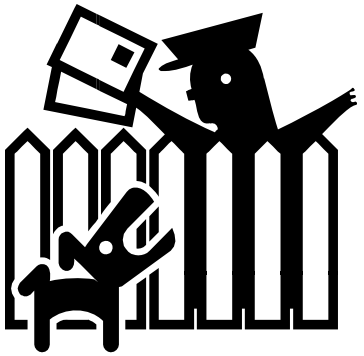
MultiBoot Comparison

	Spartan-3E	Spartan-3A
Complexity	Easy	Complex
MultiBoot from BPI	Up or Down	Up only
MultiBoot from SPI	No	✓
MultiBoot from Platform Flash	✓	✓
MultiBoot between memories	No	✓
MultiBoot Trigger	MBT on STARTUP	Via ICAP
MultiBoot Images	2 (Top or Bottom)	Depends on PROM size
Specify start address?	No (Top or Bottom only)	✓
ICAP required	N/A	✓
Watchdog	No	✓

Slide courtesy Xilinx GPD

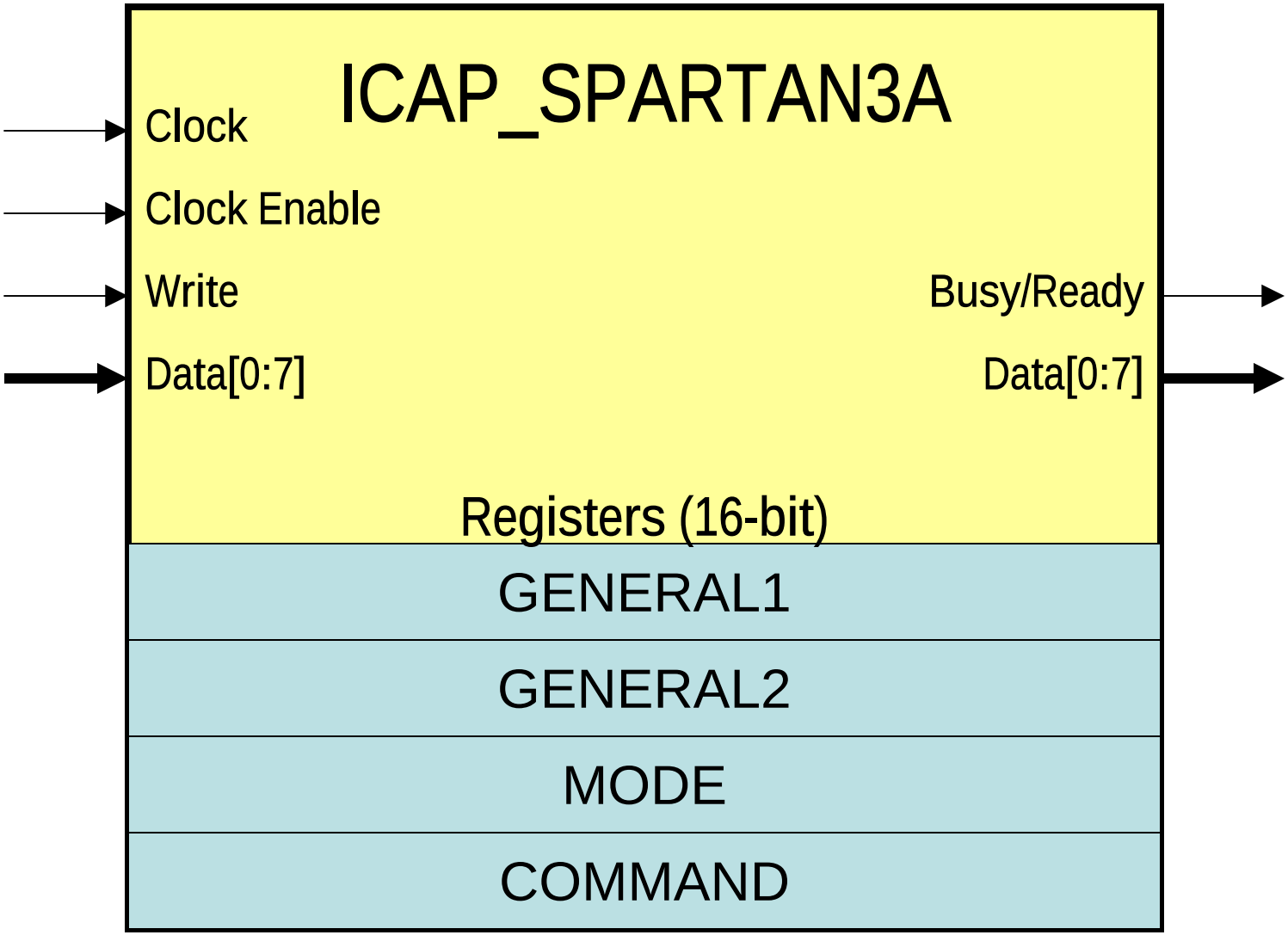
Watchdog Timer

- **16-bit counter clocked by CCLK (default)**
  - ~66 ms
- **Power-Up BPI/SPI Retry**
  - If no SYNC word is detected, resends address/read command
- **MultiBoot Fail-Safe Retry**
  - If no SYNC word is detected, starts over from the “fail-safe” bitstream by resending read command (if SPI) & address 0
- **Master Mode Frame Error Retry**
  - If configuration CRC error, reboot and start over
    from the first address / read command
- **Three Strikes and You’re Out**
  - After three failures of any of the above scenarios,
    stop configuring, pull INIT_B pin Low



Slide courtesy Xilinx GPD

Internal Configuration Access Port (ICAP)



GENERAL1 Register

SPI & BPI: Lower 16 address bits for next configuration address

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Two ways to set it

1. **Write to ICAP in application**
2. **Bitgen option *next_config_address***

GENERAL2 Register

SPI: Flash write command and upper 8 address bits for next configuration address

C7	C6	C5	C4	C3	C2	C1	C0	A23	A22	A21	A20	A19	A18	A17	A16

BPI: Upper 10 address bits for next configuration address

-	-	-	-	-	-	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16

Two ways to set it

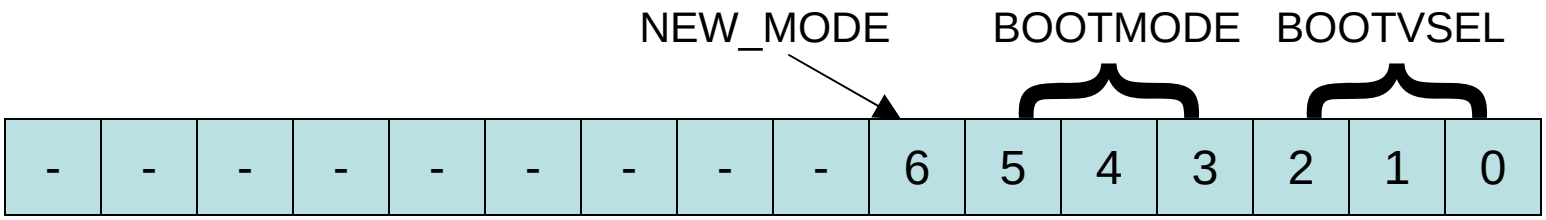
1. **Write to ICAP in application**
2. **Bitgen option *next_config_address***

MODE Register

NEW_MODE: 0=use Mode pins; 1=use BOOTMODE and BOOTVSEL

BOOTMODE: Internal Mode setting

BOOTVSEL: Internal Variant Select setting



One way to set it

1. **Write to ICAP in application**

- **However, by default, NEW_MODE = 0**
- **If MultiBoot destination is in the same memory, no need to set this register**

COMMAND Register

Only one command defined: REBOOT = b01110

-	-	-	-	-	-	-	-	-	-	-	4	3	2	1	0

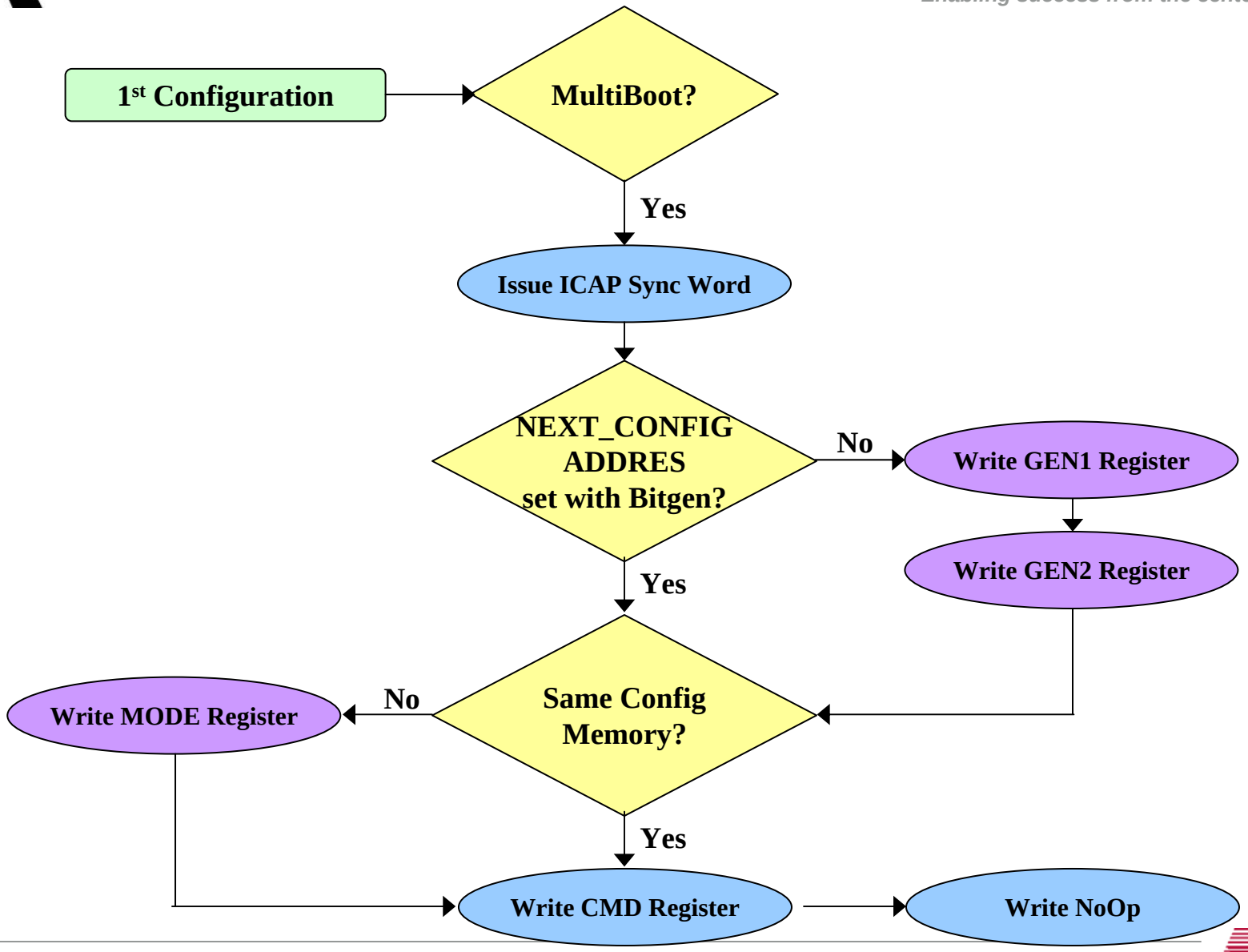
One way to set it

1. **Write to ICAP in application**
   - REBOOT command is the MultiBoot trigger

Steps to Get MultiBoot Working

- **Create at least two designs and test them**
- **Instantiate ICAP_SPARTAN3A in the MultiBoot-capable design**
- **Add a state machine to write to ICAP during MultiBoot**
- **Decide the location for the next bitstream**
  - Set the next location address in state machine or Bitgen
- **Enable ICAP in Bitgen for that design**
- **Create & store the MultiBoot image, matching the next location address**

MultiBoot State Machine Flow Chart

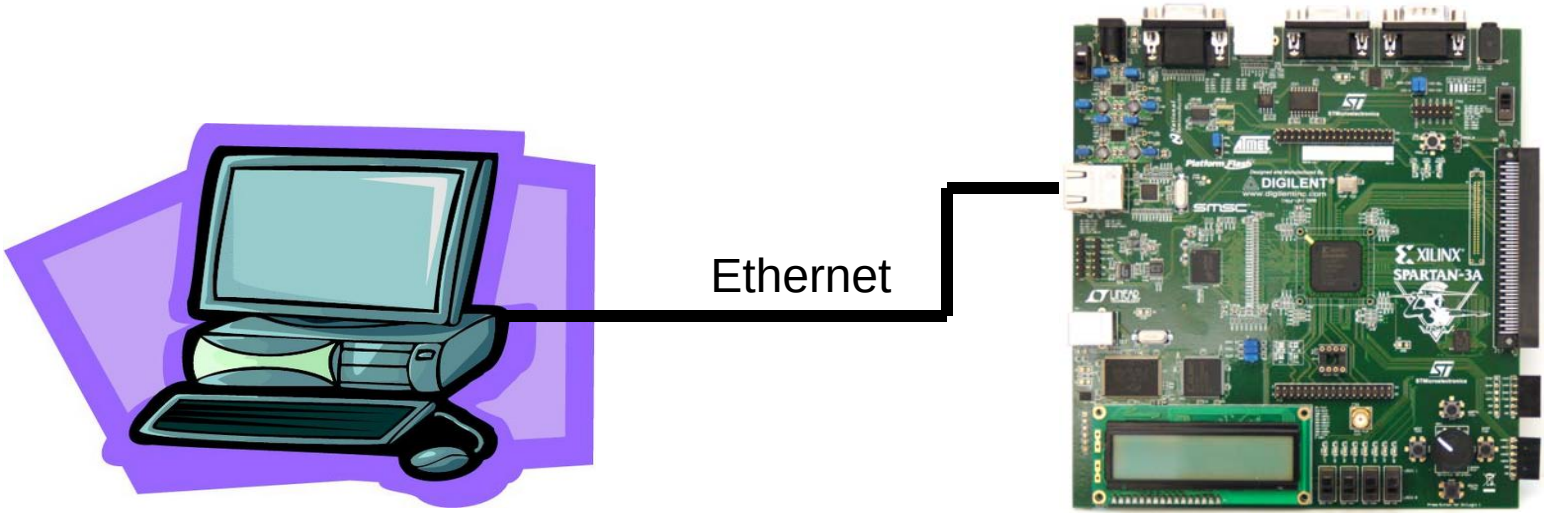


Writing ICAP Registers

- **Typically 32-bits per transaction**
  - 8-bit instruction
  - 8-bit destination address
  - 16-bit data
- **8-bit ICAP port**
- **Therefore, each register write requires four cycles**
  - Write instruction
  - Write destination
  - Write upper 8 data bits
  - Write lower 8 data bits

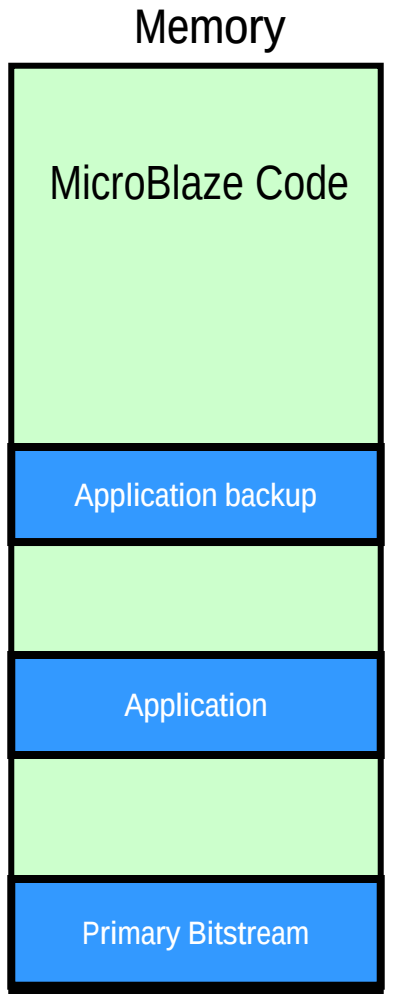
Remote Configuration Update Example

- **Update application bitstream over Ethernet**
- **Destination is multi-boot location in flash**
- **If update fails**
  - System reverts to primary, maintenance bitstream
  - Try update again

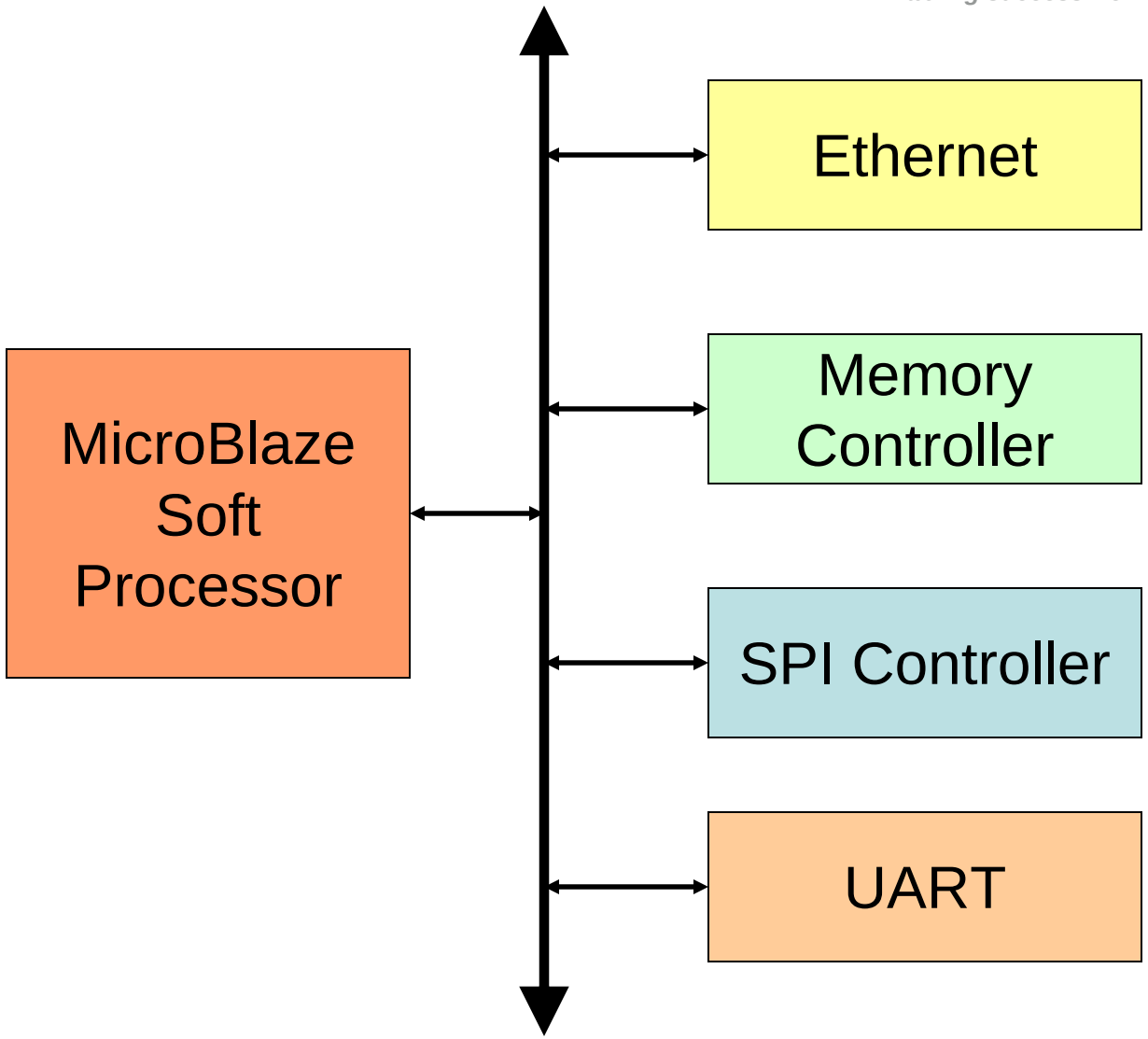


Primary Bitstream User Interface

- **Press 1 to boot application**
  - Multiboot to location #2
- **Press 2 to update application**
  - Save current application to location #3
  - Receive new bitstream over ethernet, stored in RAM
  - Transfer new bitstream from RAM to location #2
- **Press 3 to boot previous application**
  - Multiboot to location #3
- **Press 4 to restore previous application**
  - Move bitstream at location #3 back to location #2



Primary System Hardware



Demonstration

- **Bitstreams**
  - Primary bitstream as described
  - Application bitstream #1 flashes LED #1
  - Application bitstream #2 flashes LED #2

- **Process**
  - Multi-boot system to Application #1
  - Re-boot to primary
  - Update to Application #2
  - Multi-boot again

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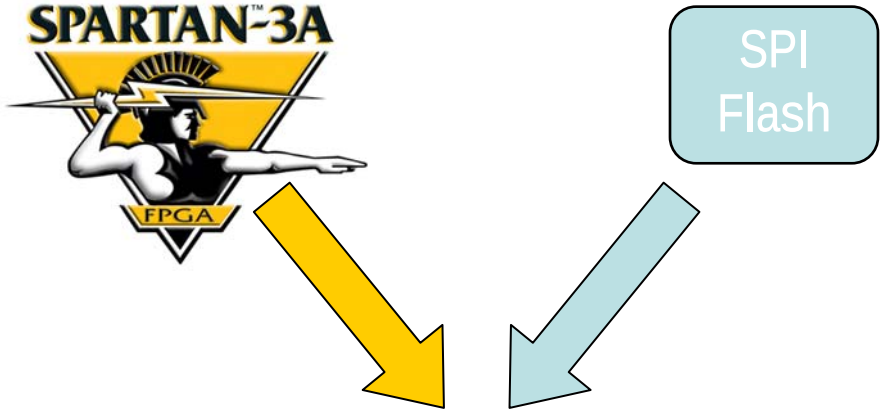
Spartan-3AN

"N" = Non-volatile



SPARTAN-3AN

- Less board space
- Integrated configuration
- Extra flash space for user design

Spartan-3AN Platform

- **Fourth member of Spartan-3 Generation FPGAs**
  - Four devices from 200K gates to 1.4M gates
  - I/O ranging from 195 to 502
- **Key New Features**
  - Up to 11Mbits of integrated User Flash
  - Customizable security
- **All devices in full production by end of Q3, 2007**
- **Full tool support in ISE Foundation and WebPACK™**
- **Pin compatible with Spartan-3A**

Spartan-3AN Configuration

- **Internal**
  - Configuration interface hidden from the user increasing device security
  - Fixed configuration interface
  - Multi-boot capability
    - Internally support up to 2 configuration files
- **External**
  - Same as Spartan-3A, including Multi-boot

Spartan-3AN Programming Support

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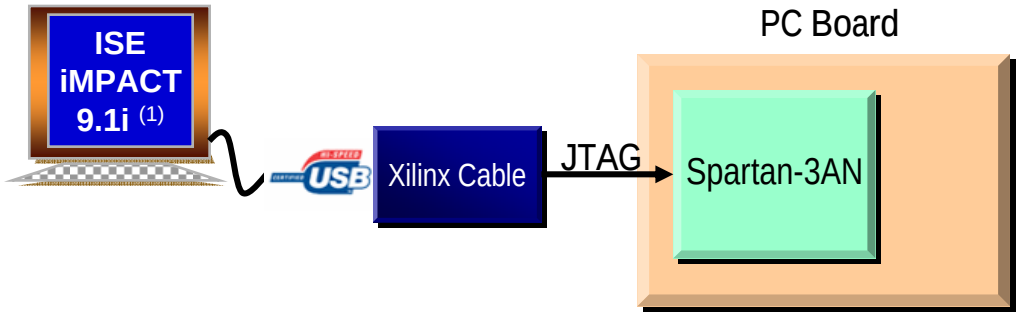

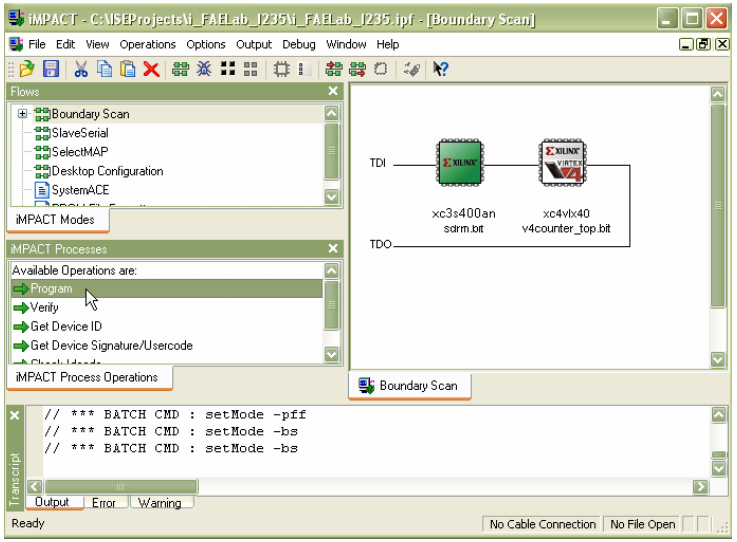

- **Prototype**
  - Xilinx iMPACT & cables allow quick and easy prototyping and debugging
    - Software: ISE iMPACT 9.1i
    - Cables: Platform USB Cable, Parallel Cable IV, MultiPRO
- **Production**
  - BP Microsystems programmer support Spartan-3AN
    - Single and gang programming

Spartan-3AN Platform

Device	XC3S50AN	XC3S200AN	XC3S400AN	XC3S700AN	XC3S1400AN
System Gates	50K	200K	400K	700K	1,400K
Logic Cells	1,584	4,032	8,064	13,248	25,344
Mults/BRAMs	3	16	20	20	32
Flash Size Bits	1M	4M	4M	8M	16M
User Flash Bits*	642K	3.1M	2.4M	5.9M	12.5M
DCMs	2	4	4	8	8
Max Differential I/O	50	90	142	165	227
Max Single Ended I/O	108	195	311	372	502
TQ144	108				
FT256		195			
FG400			311		
FG484				372	
FG676					502

*** User Flash can be used for additional configuration storage, data storage, and/or microcode storage**

Note: Spartan-3AN Platform devices are pin compatible with Spartan-3A Platform

Conclusion

- **Spartan-3A supports all the previously supported configuration techniques**
- **Spartan-3A enhances support for industry standard flash**
  - Multi-boot expanded to support >2 images
  - ICAP allows full control over the multi-boot sequence
  - Watchdog
- **Spartan-3AN is Spartan-3A Non-volatile**
  - All the Spartan-3A features
  - Plus integrated SPI flash

What's Next?

- **Contact your FAE**
- **Get Xilinx tools**
  - ISE WebPACK can be downloaded free
  - EDK is often bundled with Avnet development boards during Avnet Speedway promotions
- **Get a development board**
- **Create your own multi-boot design**
  - Or attend an Avnet Speedway workshop in your area

Thank You!
Any Questions?