

## STP16CPC26

### Low voltage 16-bit constant current LED sink driver

#### **Features**

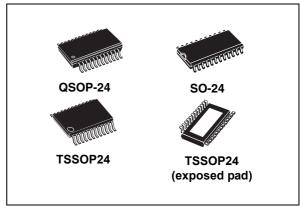
- 16 constant current output channels
- Adjustable output current through external resistor
- Output current: 5 mA to 90 mA
- ±1% typical current accuracy bit to bit
- Max clock frequency: 30 MHz
- 20 V current generators rated voltage
- 5 V power supply
- Thermal shutdown for overtemperature protection

### **Applications**

- Video display panel LED driver
- Special lighting

## **Description**

The STP16CPC26 is a monolithic, low voltage, 16-bit constant current LED sink driver. The device contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. In the output stage sixteen regulated current generators provide 5 mA to 90 mA constant current to drive LEDs. The current is



externally adjusted through a resistor. LED brightness can be adjusted from 0% to 100% via  $\overline{\text{OE}}$  pin.

The STP16CPC26 guarantees a 20 V driving capability, allowing users to connect more LEDs in series to each current source.

The high 30 MHz clock frequency makes the device suitable for high data rate transmission.

The thermal shutdown (170°C with about 15°C hysteresis) assures protection from overtemperature events.

The STP16CPC26 is housed in four different packages: QSOP-2, SO-24, TSSOP-24 and HTSSOP-24 (with exposed pad).

Table 1. Device summary

Order codes	Package	Packaging
STP16CPC26MTR	SO-24	1000 parts per reel
STP16CPC26TTR	TSSOP24	2500 parts per reel
STP16CPC26XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPC26PTR	QSOP-24	2500 parts per reel

Contents STP16CPC26

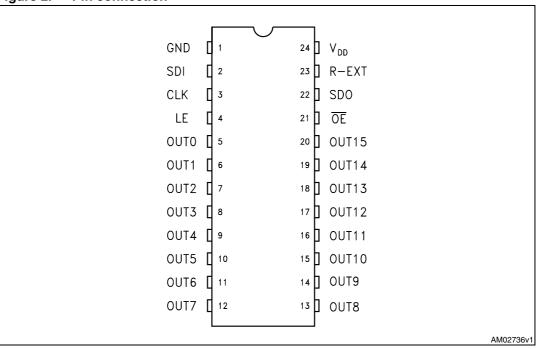
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STP16CPC26 Pin description

## 1 Pin description

Figure 2. Pin connection



Note:

Exposed-pad should be electrically connected to a metal land electrically isolated or connected to ground

Table 2. Pin description

Pin N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	ŌĒ	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	$V_{DD}$	Supply voltage terminal

Electrical ratings STP16CPC26

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the "absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage	0 to 7	V
V <sub>O</sub>	Output voltage	-0.5 to 20	٧
Io	Output current	90	mA
VI	Input voltage	-0.4 to V <sub>DD</sub> +0.4	V
I <sub>GND</sub>	GND terminal current	1600	mA
ESD	Electrostatic discharge protection HBM human body model	±2	kV
f <sub>CLK</sub>	Clock frequency	50	MHz

#### 2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit	
T <sub>A</sub>	Operating free-air temperature range	-40 to +125		
T <sub>OPR</sub>	Operating temperature range	-40 to +150	°C	
T <sub>STG</sub>	Storage temperature range	-55 to +150		
		SO-24	60	
	Thermal resistance junction-case	TSSOP24	85	°C/W
R <sub>thJA</sub>	(1)	TSSOP24 <sup>(2)</sup>	37.5	C/VV
		QSOP24	72	

<sup>1.</sup> According with JEDEC standard 51-7B

<sup>2.</sup> The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

## 3 Electrical characteristics

 $V_{DD}$  = 5 V,  $T_A$  = 25°C, unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{DD}$	Supply voltage		4.5	5	5.5	٧
V <sub>IH</sub>	Input voltage high level		0.8*Vdd	-	Vdd	V
V <sub>IL</sub>	Input voltage low level		GND	-	0.2*Vdd	٧
V <sub>OL</sub>	Serial data output voltage	I <sub>OH</sub> =- 1mA,	-	-	0.4	V
V <sub>OH</sub>	(SDO) <sup>(1)</sup>	I <sub>OL</sub> =+ 1mA	V <sub>DD</sub> -0.4	-	-	<b>'</b>
I <sub>OH</sub>	Output leakage current	V <sub>O</sub> =20V, Outn = OFF	-	-	0.5	μΑ
I <sub>OL1</sub>	Output current (2)	$V_{DS}$ =0.3V, $R_{EXT}$ =900 $\Omega$	20.7	22	23.3	mA
I <sub>OL2</sub>	Output current (2)	$V_{DS}$ =0.6V, $R_{EXT}$ =360 $\Omega$	51.7	55	58.3	IIIA
Δl <sub>OL2</sub>	Current accuracy channel-to-	$V_{DS}$ =0.3V, $R_{EXT}$ =900 $\Omega$ , $I_{OL}$ = 22mA	-	±1	±3	%
Δl <sub>OL3</sub>	channel (2) (3)	$V_{DS}$ =0.6V, $R_{EXT}$ =360 $\Omega$ , $I_{OL}$ = 55mA	-	±1	±3	70
R <sub>IN</sub> (up)	Pull-up resistor for OE pin		250	500	800	kΩ
R <sub>IN</sub> (down)	Pull-down resistor for LE pin		250	500	800	K\$2
I <sub>DD(OFF1)</sub>		R <sub>EXT</sub> = OPEN, OUT 0 to 15 = OFF	-	3	6.8	
I <sub>DD(OFF2)</sub>	Supply current (OFF)	$R_{EXT} = 900\Omega$ , OUT 0 to 15 = OFF	-	7	9.6	
I <sub>DD(OFF3)</sub>		$R_{EXT} = 360\Omega$ , OUT 0 to 15 = OFF	-	11	13.2	mA
I <sub>DD(ON1)</sub>	Supply current (ON)	$R_{EXT} = 900\Omega$ , OUT 0 to 15 = ON	-	7	10.8	
I <sub>DD(ON2)</sub>	Зарріў сапені (ОМ)	$R_{EXT} = 360\Omega$ , OUT 0 to 15 = ON	-	11	15.3	
%/dV <sub>DS</sub>	Output current vs. output voltage regulation <sup>(4)</sup>	$V_{DS}$ from 1.0V to 3.0V $I_{O}$ =22mA $I_{O}$ =55mA	-	±0.1	-	%/V
%/dV <sub>DD</sub>	Output current vs. supply voltage regulation <sup>(4)</sup>	I <sub>O</sub> =22mA; V <sub>DS</sub> =0.3V I <sub>O</sub> =55mA; V <sub>DS</sub> =0.6V	-	±1	-	%/V
Tsd	Thermal shutdown <sup>(4)</sup>		170	-	-	
Tsd-hy	Thermal shutdown hysteresis (4)		-	15	20	°C

<sup>1.</sup> Specification within -40 to +125  $^{\circ}$ C T<sub>J</sub> temperature range are assured by design, characterization and statistical correlation.

<sup>2.</sup> Test performed with all outputs turned on, but only one output loaded at a time.

<sup>3.</sup>  $\Delta_{\text{IOL+}} = ((I_{\text{OLmax}} - I_{\text{OLmean}}) / I_{\text{OLmean}})^* 100, \ \Delta_{\text{IOL-}} = ((I_{\text{OLmin}} - I_{\text{OLmean}}) / I_{\text{OLmean}})^* 100, \ \text{where } I_{\text{OLmean}} = (I_{\text{OLout1}} + I_{\text{OLout2}} + \ldots + I_{\text{OLout16}}) / 16$ 

<sup>4.</sup> Not tested, guaranteed by design

Electrical characteristics STP16CPC26

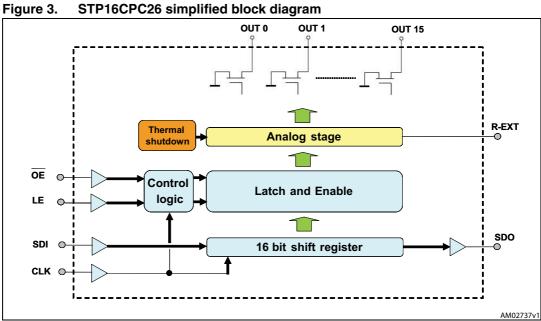
 $V_{DD}$  = 5 V, Tj = 25°C, unless otherwise specified

Table 6. Switching characteristics

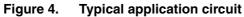
Symbol	ı	Parameter	Test conditions	Min.	Тур.	Max.	Unit
f <sub>clk</sub>	Clock frequen	су	Cascade operation	-	-	30	MHz
t <sub>PLH1</sub>	CLK - OUTn				100		ns
t <sub>PLH2</sub>	LE - OUTn	Propagation			100		ns
t <sub>PLH3</sub>	OE – OUTn	delay time ("L" to "H")			80		ns
t <sub>PLH</sub>	CLK - SDO				20		ns
t <sub>PHL1</sub>	CLK - OUTn				28		ns
t <sub>PHL2</sub>	LE - OUTn	Propagation delay time			28		ns
t <sub>PHL3</sub>	OE – OUTn	("H" to "L")	$V_{DS} = 0.8V$ $V_{IH} = V_{DD}$		25		ns
t <sub>PHL</sub>	CLK - SDO		V <sub>IL</sub> = QND		20		ns
t <sub>w(CLK)</sub>	CLK		$R_{\text{ext}} = 300 \ \Omega$	20	-	-	ns
t <sub>w(L)</sub>	LE	Pulse width	$V_{LED} = 4.0V$	20	-	-	ns
tw(OE)	ŌĒ		$R_L = 51\Omega$ $C_L = 10pF$	150	-	-	ns
t <sub>su(L)</sub>	Setup time for LE			5	-	-	ns
t <sub>h(L)</sub>	Hold time for LE			5	-	-	ns
t <sub>su(D)</sub>	Setup time for	SDI		5	-	-	ns
t <sub>h(D)</sub>	Hold time for	SDI		5	-	-	ns
t <sub>r</sub> <sup>(1)</sup>	Maximum CLI	K rise time		-	-	5000	ns
t <sub>f</sub> (1)	Maximum CLI	K fall time		-	-	5000	ns
t <sub>or1</sub>	Output rise tin	ne of V <sub>out</sub>	V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = GND		75		ns
t <sub>of1</sub>	Output fall tim	e of V <sub>out</sub>	$V_{DS} = 0.8V$ , $R_L = 51\Omega$ $C_L = 10$ pF, $I_{out} = 5$ mA		67		ns
t <sub>or2</sub>	Output rise tin	ne of V <sub>out</sub>	V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = GND		75		ns
t <sub>of2</sub>	Output fall time of V <sub>out</sub>		$V_{DS} = 0.8V$ , $R_L = 51\Omega$ $C_L = 10$ pF, $I_{out} = 20$ mA		50		ns
t <sub>or3</sub>	Output rise time of Vout		V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = GND		72		ns
t <sub>of3</sub>	Output fall tim	e of V <sub>out</sub>	$V_{DS} = 0.8V$ , $R_L = 51\Omega$ $C_L = 10$ pF, $I_{out} = 60$ mA		50		ns
I <sub>out-ov</sub>	Output curren	t turn-on overshoot	$V_{DS} = 0.6 \text{ to } 3V$ $R_L = 51, C_L = 10pF; I_{out} = 5 \text{ to } 60mA$	-	-	0	%

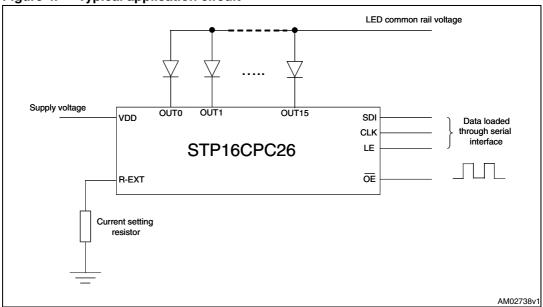
If devices are connected in cascade and tr or tf is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

#### Simplified Internal Block diagram 4



# 5 Typical application circuit





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## 6 Equivalent circuits for inputs and outputs

Input terminals LE and  $\overline{\text{OE}}$  have pull-down and pull-up connection respectively. CLK and SDI must be connected to external circuit to fix the logic level.

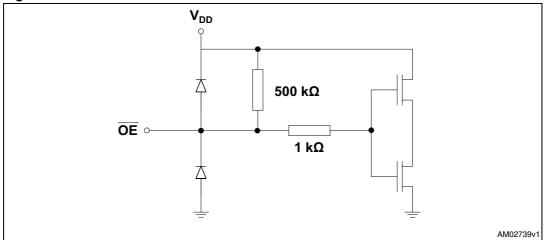


Figure 6. LE terminal

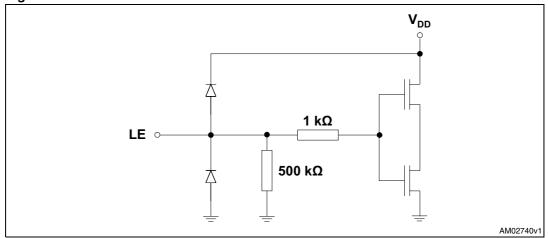


Figure 7. CLK, SDI terminal

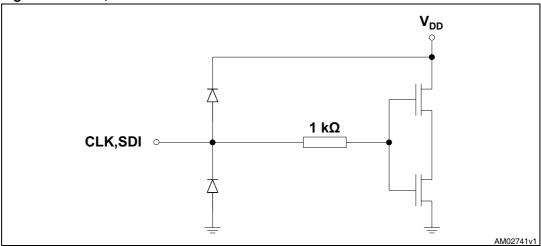
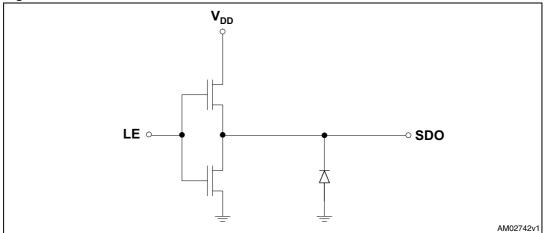


Figure 8. SDO terminal



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STP16CPC26 Typical test circuits

## 7 Typical test circuits

*Figure 9* and *Figure 10* show respectively the typical test circuit used measuring electrical (e.g. input voltage high/low level, output leakage current, supply current, etc.) and switching characteristics (propagation delays, set-up and hold time, rise and fall time of V<sub>OUT</sub>, etc.).

The resistor  $R_L$  and capacitor  $C_L$  in parallel connected to each output in *Figure 9* simulate a LED behavior.

Figure 9. Typical test circuit for electrical characteristics

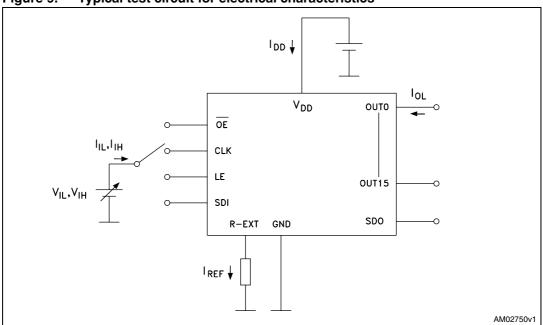
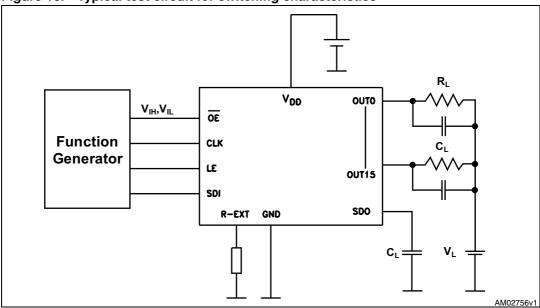


Figure 10. Typical test circuit for switching characteristics



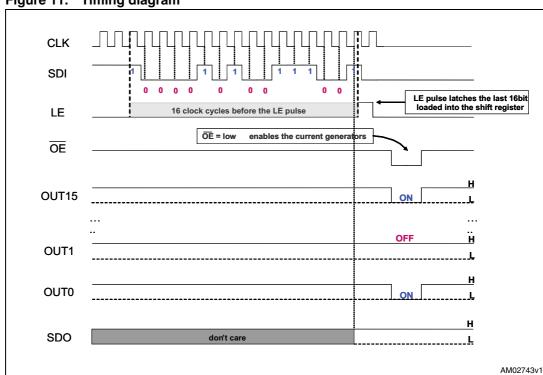
Timing diagrams STP16CPC26

## 8 Timing diagrams

The timing diagram shown in *Figure 11* and the truth table in *Table 7* explain how to send data to the device. This can be summarized in the following points:

- LE and OE are level sensitive and not synchronized with the CLK signal
- When LE is at low level, the latch circuit holds previous data
- If LE is high level, data present in the shift register are latched
- When  $\overline{\text{OE}}$  is at low level, the status of the outputs OUT0 to OUT15 depends on the data in the latch circuits
- With  $\overline{OE}$  at high level, all outputs are switched off independently on the data stored in the latch circuits
- Every rising edge of the CLK signal, a new data on SDI pin is sampled. This data is loaded into the shift register, whereas a bit is shifted out from SDO.



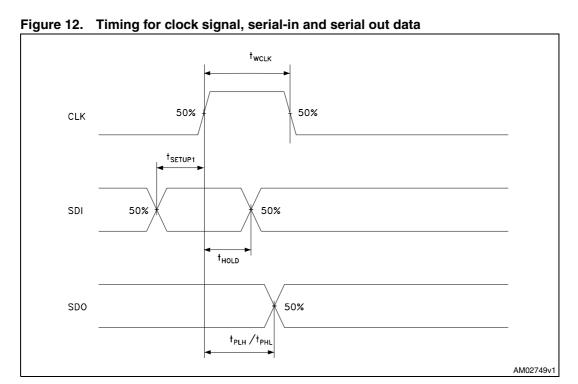


STP16CPC26 Timing diagrams

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CLOCK	LE	ŌĒ	SDI	OUT15OUT0 <sup>(1)</sup>	SDO
?	Н	L	D <sub>n</sub>	D <sub>n</sub> D <sub>n-15</sub>	D <sub>n-16</sub>
?	L	L	D <sub>n+1</sub>	n+1 NO CHANGE	
?	Н	L	D <sub>n+2</sub>	D <sub>n+2</sub> D <sub>n-13</sub>	D <sub>n-14</sub>
?	Х	L	D <sub>n+3</sub>	D <sub>n+2</sub> D <sub>n-13</sub>	D <sub>n-14</sub>
?	Х	Н	D <sub>n+3</sub>	OFF	D <sub>n-14</sub>

Table 7. Truth table

<sup>1.</sup> OUTn = ON when Dn = H, OUTn = OFF when Dn = L



The correct sampling of the data depends on the stability of the data at SDI on the rising edge of the clock signal and it is assured by a proper data setup and hold time ( $t_{SETUP1}$  And  $t_{HOLD}$ ), as shown in *Figure 12*. The same figure shows the propagation delay from CLK to SDO ( $t_{PLH}/t_{PHL}$ ).

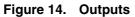
Figure 13 describes the setup times for LE and  $\overline{\text{OE}}$  signals ( $t_{\text{SETUP2}}$  and  $t_{\text{SETUP3}}$  respectively), the minimum duration of these signals ( $t_{\text{WLAT}}$  and  $t_{\text{WENA}}$  respectively) and the propagation delay from CLK to  $\text{OUT}_n$ , LE to  $\text{OUT}_n$  and  $\overline{\text{OE}}$  to  $\text{OUT}_n$  ( $t_{\text{PLH1}}/t_{\text{PHL1}}$ ,  $t_{\text{PLH2}}/t_{\text{PHL2}}$  and  $t_{\text{PLH3}}/t_{\text{PHL3}}$  respectively).

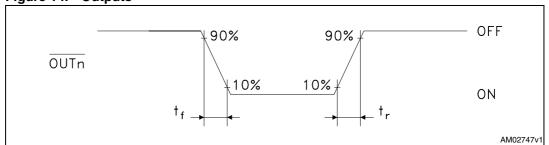
Finally *Figure 14* defines the turn-on and turn-off time  $(t_r \text{ and } t_f)$  of the current generators.

**Timing diagrams** STP16CPC26

50% CLK SDI †SETUP2 50% 50% LE t<sub>WLAT</sub> †<sub>WENA</sub> OE 50% 50% †<sub>SETUP3</sub> OUTn 50%  $t_{\rm PHL1}/t_{\rm PLH1}$  $t_{PHL2}/t_{PLH2}$  $t_{\rm PHL3}/t_{\rm PLH3}$ 

Figure 13. Timing for clock signal serial-in data, latch enable, output enable and outputs





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## 9 Current generators characteristics

### 9.1 Current setting

The current of all outputs is programmed through an external resistor connected to R-EXT pin, as shown in *Figure 15*.

The curve in *Figure 16* describes the relation between the current and the resistor connected to R-EXT pin, whereas the *Table 8* shows how to set some typical current values.

Figure 15. Resistor for current programming

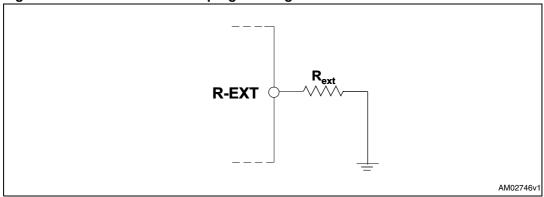


Figure 16. Output current vs R-EXT resistor

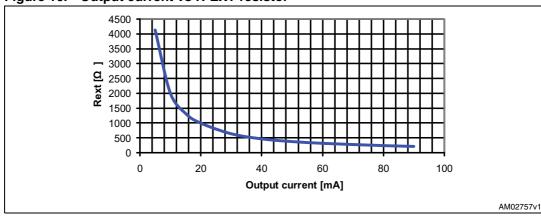


Table 8. Recommended values of Rext for some output current value

Output current [mA]	R <sub>ext</sub> [Ω]	Closer standard value (E24 series) [ $\Omega$ ]
5	4129	4300
10	2005	200
20	999	1000
40	471	470
60	322	330
90	217	220

### 9.2 Current accuracy

A typical current accuracy of  $\pm 1\%$  ( $\pm 3\%$  maximum) between channels is guaranteed at 22 mA and 55 mA output current (refer to *Table 5*) and  $\pm 6\%$  (maximum) current accuracy between ICs.

### 9.3 Generators voltage drop

In order to correctly regulate the current, a minimum dropout voltage must be assured across the current generators.

Figure 17 and Table 9 provides just an indicative idea about the dropout voltage to assure over the current range. However it is recommended to use value of  $V_{DROP}$  slightly higher than those indicated in Figure 17 and Table 9.

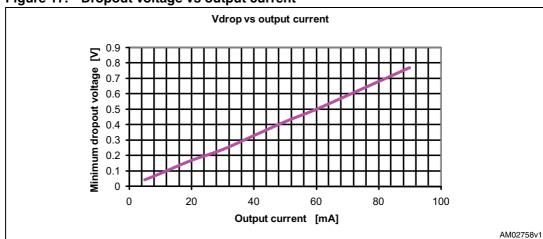


Figure 17. Dropout voltage vs output current

Table 9. Dropout voltage vs output current

Output current [mA]	V <sub>DROP</sub> @ 3.3V [mV]	V <sub>DROP</sub> @ 5V [mV]
5	44	44
10	85	85
20	170	170
40	350	330
60	530	500
90	820	770

#### 9.4 Turn-on and turn-off characteristics

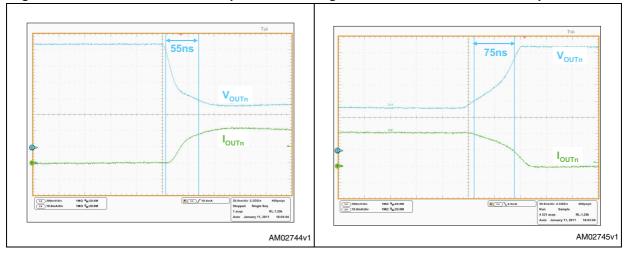
Figure 18 and 19 shows the turn-on and turn-off time of an output of STP16CPC26 with a programmed current of 20 mA per channel and a drop across the current generators of 0.8 V.

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In this example the turn-on and turn-off time (measured between the 10% and 90% of the voltage of the OUTn pin) are respectively around 55 ns and 75 ns.

Figure 18. Turn-on time of the outputs

Figure 19. Turn-off time of the outputs



Thermal shutdown STP16CPC26

### 10 Thermal shutdown

The STP16CPC26 is featured with a thermal shutdown. This protection is triggered if the junction temperature reaches 170°C. When the thermal shutdown is activated, all outputs are turned off independently on the data latched.

Once the temperature decreases (thermal shutdown hysteresis is typically 15°C), the outputs are enabled again and the device keeps on working.

# 11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 10. QSOP-24 mechanical data

Dim.		mm.			inch	
	Min	Тур	Max	Min	Тур	Max
Α	1.54	1.62	1.73	0.061	0.064	0.068
A1	0.1	0.15	0.25	0.004	0.006	0.010
A2		1.47			0.058	
b	0.31	0.2		0.012	0.008	
С	0.254	0.17		0.010	0.007	
D	8.56	8.66	8.76	0.337	0.341	0.345
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.91	4.01	0.150	0.154	0.158
е		0.635			0.025	
L	0.4	0.635	0.89	0.016	0.025	0.035
h	0.25	0.33	0.41	0.010	0.013	0.016
<	8°	0°				

DIMENSIONS IN mm BOTTOM VIEW GAUGE PLANE D/2-// 0.1 C C 0,25 <u>A 1</u> b (24x) SEATING PLANE ○ 0.1 C COPLANAR LEADS 13 E1 12 С TOP VIEW PIN 1 IDENTIFICATION

Figure 20. QSOP-24 package dimensions

Table 11. TSSOP24 mechanical data

Dim.	mm.		inch			
Dilli.	Min	Тур	Max	Min	Тур	Max
Α			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
С	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
Е	4.3		4.5	0.169		0.177
е		0.65 BSC			0.0256 BSC	
Н	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

Figure 21. TSSOP24 package dimensions

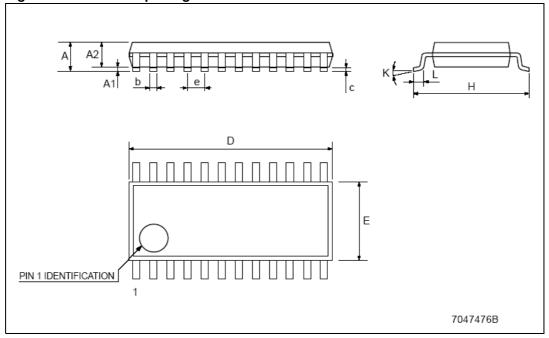


Table 12. Tape and reel TSSOP24

Dim.	mm.			inch		
	Min	Тур	Max	Min	Тур	Max
Α		-	330		-	12.992
С	12.8	-	13.2	0.504	-	0.519
D	20.2	-		0.795	-	
N	60	-		2.362	-	
Т		-	22.4		-	0.882
Ao	6.8	-	7	0.268	-	0.276
Во	8.2	-	8.4	0.323	-	0.331
Ko	1.7	-	1.9	0.067	-	0.075
Po	3.9	-	4.1	0.153	-	0.161
Р	11.9	-	12.1	0.468	-	0.476

Figure 22. Reel dimensions

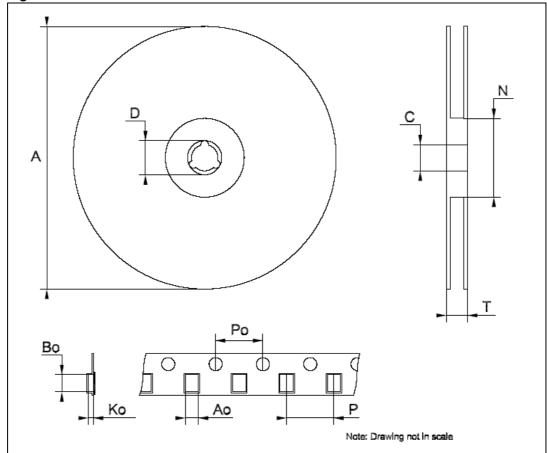


Table 13. SO-24 mechanical data

Dim.	mm.			inch		
	Min	Тур	Max	Min	Тур	Max
Α			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
С		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
Е	10.00		10.65	0.393		0.419
е		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 23. SO-24 package dimensions

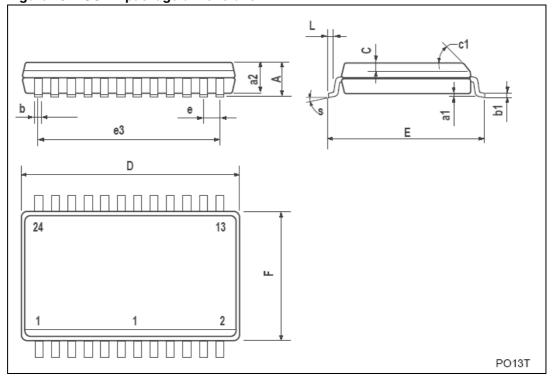


Table 14. Tape and reel SO-24

Dim.	mm.			inch		
	Min	Тур	Max	Min	Тур	Max
Α		-	330		-	12.992
С	12.8	-	13.2	0.504	-	0.519
D	20.2	-		0.795	-	
N	60	-		2.362	-	
Т		-	30.4		-	1.197
Ao	10.8	-	11.0	0.425	-	0.433
Во	15.7	-	15.9	0.618	-	0.626
Ko	2.9	-	3.1	0.114	-	0.122
Po	3.9	-	4.1	0.153	-	0.161
Р	11.9	-	12.1	0.468	-	0.476

Figure 24. Reel dimensions

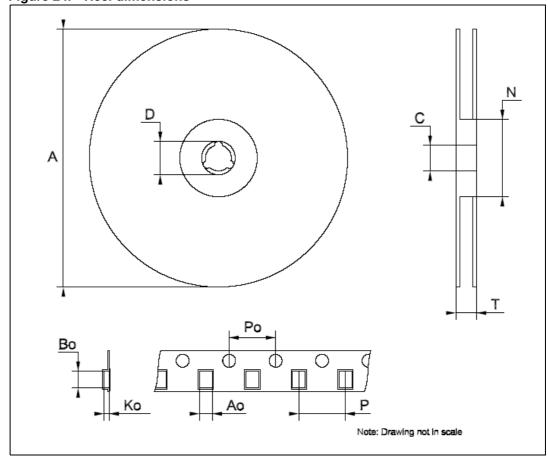
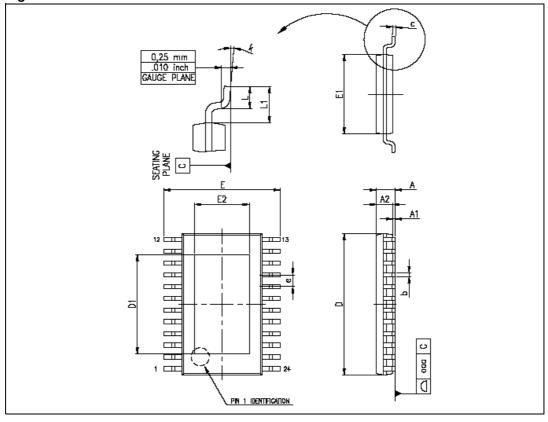


Table 15. TSSOP24 exposed-pad

Dim	mm			inch		
Dim.	Min	Тур	Max	Min	Тур	Max
Α			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
С	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1	4.7	5.0	5.3	0.185	0.197	0.209
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.2	3.5	0.114	0.126	0.138
е		0.65			0.0256	
К	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 25. TSSOP24 dimensions



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Revision history STP16CPC26

# 12 Revision history

Table 16. Document revision history

Date	Revision	Changes
04-Mar-2011	1	First release
05-Apr-2011	2	Updated Table 5

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