VQ100: 100-lead Very Thin Quad Flat Package

The XC3S50A and XC3S200 are available in the 100-lead very thin quad flat package, VQ100.

Table 63 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 does not support Suspend mode (SUSPEND and AWAKE are not connected), the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode, or daisy chain configuration (DOUT is not connected).

Table 63 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A, highlighted in light blue. See "Footprint Migration Differences," page 72 for additional information.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 63: **Spartan-3A VQ100 Pinout**

Bank	Pin Name	Pin	Type
0	IO_0/GCLK11	P90	CLK
0	IO_L01N_0	P78	IO
0	IO_L01P_0/VREF_0	P77	VREF
0	IO_L02N_0/GCLK5	P84	CLK
0	IO_L02P_0/GCLK4	P83	CLK
0	IO_L03N_0/GCLK7	P86	CLK
0	IO_L03P_0/GCLK6	P85	CLK
0	IO_L04N_0/GCLK9	P89	CLK
0	IO_L04P_0/GCLK8	P88	CLK
0	IO_L05N_0	P94	IO
0	IO_L05P_0	P93	IO
0	IO_L06N_0/PUDC_B	P99	DUAL
0	IO_L06P_0/VREF_0	P98	VREF
0	IP_0	P97	IP
0	IP_0/VREF_0	P82	VREF
0	VCCO_0	P79	VCCO
0	VCCO_0	P96	VCCO
1	IO_L01N_1	P57	IO
1	IO_L01P_1	P56	IO
1	IO_L02N_1/RHCLK1	P60	CLK
1	IO_L02P_1/RHCLK0	P59	CLK
1	IO_L03N_1/TRDY1/RHCLK3	P62	CLK
1	IO_L03P_1/RHCLK2	P61	CLK
1	IO_L04N_1/RHCLK7	P65	CLK
1	IO_L04P_1/IRDY1/RHCLK6	P64	CLK
1	IO_L05N_1	P71	IO
1	IO_L05P_1	P70	IO
1	IO_L06N_1	P73	IO
1	IO_L06P_1	P72	IO
1	IP_1/VREF_1	P68	VREF
1	VCCO_1	P67	VCCO
2	IO_2/MOSI/CSI_B	P46	DUAL
2	IO_L01N_2/M0	P25	DUAL
2	IO_L01P_2/M1	P23	DUAL
2	IO_L02N_2/CSO_B	P27	DUAL
2	IO_L02P_2/M2	P24	DUAL
2	IO_L03N_2/VS1 (3S50A) IO_L04P_2/VS1 (3S200A)	P30	DUAL
2	IO_L03P_2/RDWR_B	P28	DUAL
2	IO_L04N_2/VS0	P31	DUAL
2	IO_L04P_2/VS2 (3S50A) IO_L03N_2/VS2 (3S200A)	P29	DUAL
2	IO_L05N_2/D7 (3S50A) IO_L06P_2/D7 (3S200A)	P34	DUAL
2	IO_L05P_2	P32	IO
2	IO_L06N_2/D6	P35	DUAL
2	IO_L06P_2 (3S50A) IO_L05N_2 (3S200A)	P33	IO
2	IO_L07N_2/D4	P37	DUAL
2	IO_L07P_2/D5	P36	DUAL
2	IO_L08N_2/GCLK15	P41	CLK
2	IO_L08P_2/GCLK14	P40	CLK
2	IO_L09N_2/GCLK1	P44	CLK
2	IO_L09P_2/GCLK0	P43	CLK
2	IO_L10N_2/D3	P49	DUAL
2	IO_L10P_2/INIT_B	P48	DUAL
2	IO_L11N_2/D0/DIN/MISO (3S50A) IO_L12P_2/D0/DIN/MISO (3S200A)	P51	DUAL
2	IO_L11P_2/D2	P50	DUAL
2	IO_L12N_2/CCLK	P53	DUAL

Table 63: **Spartan-3A VQ100 Pinout*(Continued)***

2	IO_L12P_2/D1 (3S50A) IO_L11N_2/D1 (3S200A)	P52	DUAL
2	IP_2/VREF_2	P39	VREF
2	VCCO_2	P26	VCCO
2	VCCO_2	P45	VCCO
3	IO_L01N_3	P4	IO
3	IO_L01P_3	P3	IO
3	IO_L02N_3	P6	IO
3	IO_L02P_3	P5	IO
3	IO_L03N_3/LHCLK1	P10	CLK
3	IO_L03P_3/LHCLK0	P9	CLK
3	IO_L04N_3/IRDY2/LHCLK3	P13	CLK
3	IO_L04P_3/LHCLK2	P12	CLK
3	IO_L05N_3/LHCLK7	P16	CLK
3	IO_L05P_3/TRDY2/LHCLK6	P15	CLK
3	IO_L06N_3	P20	IO
3	IO_L06P_3	P19	IO
3	IP_3	P21	IP
3	IP_3/VREF_3	P7	VREF
3	VCCO_3	P11	VCCO
GND	GND	P14	GND
GND	GND	P18	GND
GND	GND	P42	GND
GND	GND	P47	GND
GND	GND	P58	GND
GND	GND	P63	GND
GND	GND	P69	GND
GND	GND	P74	GND
GND	GND	P8	GND
GND	GND	P80	GND
GND	GND	P87	GND
GND	GND	P91	GND
GND	GND	P95	GND
VCCAUX	DONE	P54	CONFIG
VCCAUX	PROG_B	P100	CONFIG
VCCAUX	TCK	P76	JTAG
VCCAUX	TDI	P2	JTAG
VCCAUX	TDO	P75	JTAG
VCCAUX	TMS	P1	JTAG
VCCAUX	VCCAUX	P22	VCCAUX
VCCAUX	VCCAUX	P55	VCCAUX
VCCAUX	VCCAUX	P92	VCCAUX

Table 63: **Spartan-3A VQ100 Pinout*(Continued)***

VCCINT	VCCINT	P17	VCCINT
VCCINT	VCCINT	P38	VCCINT
VCCINT	VCCINT	P66	VCCINT
VCCINT	VCCINT	P81	VCCINT

User I/Os by Bank

Table 64 indicates how the 68 available user-I/O pins are distributed between the four I/O banks on the VQ100 package.

Table 64: **User I/Os Per Bank for the XC3S50A and XC3S200A in the VQ100 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	15	3	1	1	3	7
Right	1	13	6	0	0	1	6
Bottom	2	26	2	0	19	1	4
Left	3	14	6	1	0	1	6
TOTAL		**68**	**17**	**2**	**20**	**6**	**23**

Footprint Migration Differences

The XC3S50A and XC3S200 have common VQ100 pinouts except for some differences in alignment of differential I/O pairs.

Differential I/O Alignment Differences

Some differential I/O pairs in the VQ100 on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A FPGAs, as shown in Table 65. All the mismatched pairs are in I/O Bank 2. These differences are indicated with the black diamond character (◆) in the footprint diagrams Figure 17 and Figure 18.

Table 65: **Differential I/O Differences in VQ100**

VQ100 Pin	Bank	XC3S50A	XC3S200A
P29	2	IIO_L04P_2/VS2	IO_L03N_2/VS2
P30		IO_L03N_2/VS1	IO_L04P_2/VS1
P33		IO_L06P_2	IO_L05N_2
P34		IO_L05N_2/D7	IO_L06P_2/D7
P51		IO_L11N_2/D0/DIN/MISO	IO_L12P_2/D0/DIN/MISO
P52		IO_L12P_2/D1	IO_L11N_2/D1

VQ100 Footprint (XC3S50A)

Note pin 1 indicator in top-left corner and logo orientation.

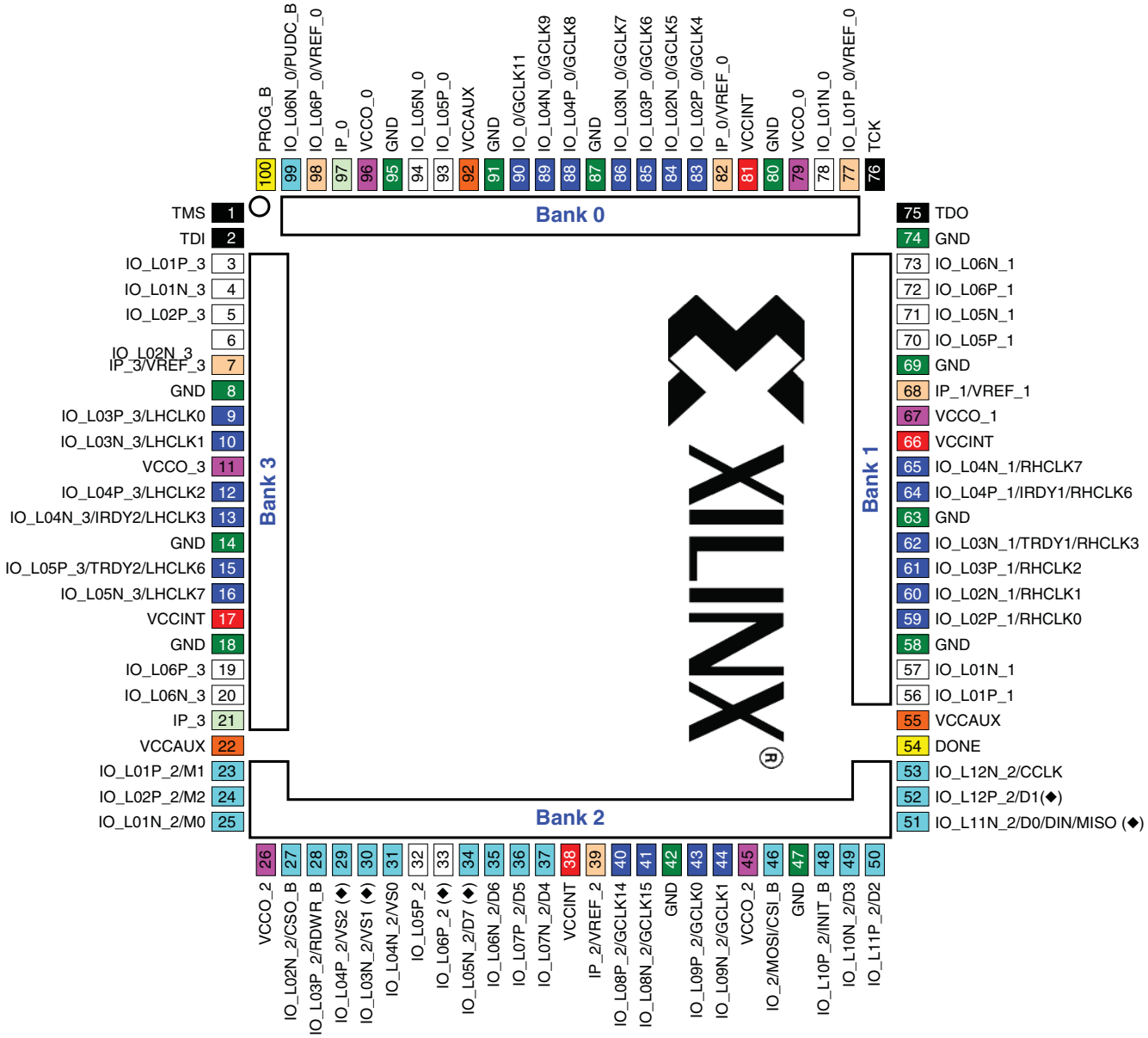

Figure 17: **VQ100 Package Footprint - XC3S50A (Top View)**

17	**I/O:** Unrestricted, general-purpose user I/O	20	**DUAL:** Configuration pins, then possible user I/O	6	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	23	**CLK:** User I/O, input, or global buffer input	6	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	3	**VCCAUX:** Auxiliary supply voltage

VQ100 Footprint (XC3S200A)

Note pin 1 indicator in top-left corner and logo orientation.

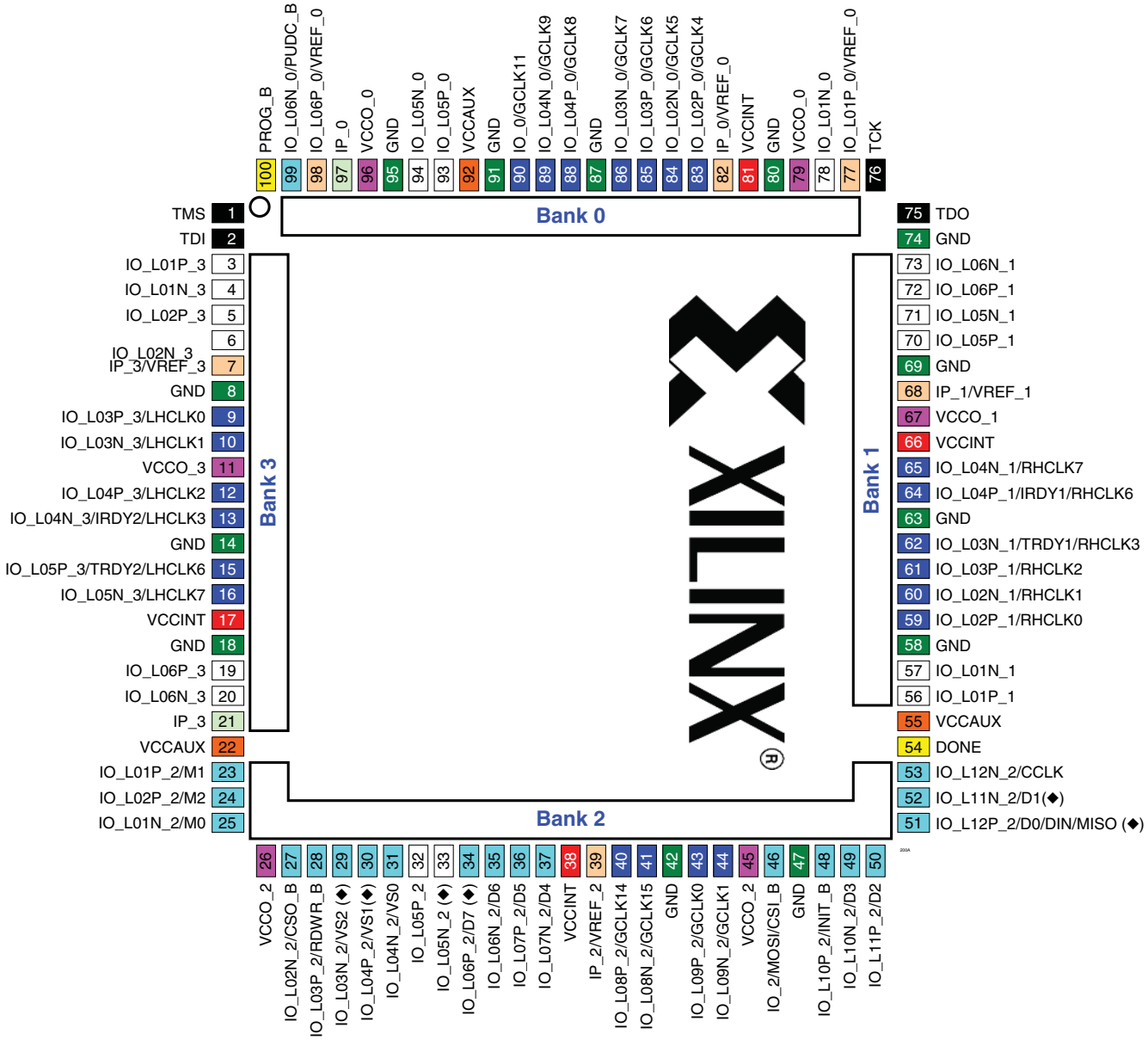

Figure 18: **VQ100 Package Footprint - XC3S200A (Top View)**

17	**I/O:** Unrestricted, general-purpose user I/O	20	**DUAL:** Configuration pins, then possible user I/O	6	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	23	**CLK:** User I/O, input, or global buffer input	6	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	3	**VCCAUX:** Auxiliary supply voltage