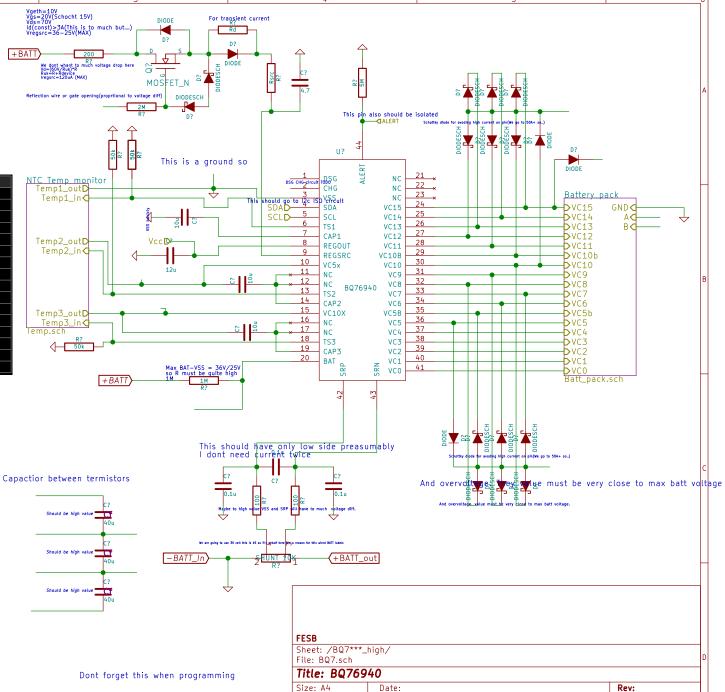


Pin configuration

PIN	NAME	TYPE	DESCRIPTION
1	DSG	0	Discharge FET driver
2	CHG	0	Charge FET driver
3	VSS	_	Chip VSS
4	SDA	I/O	I ² C communication to the host controller
5	SCL	ı	I ² C communication to the host controller
6	TS1	ī	Thermistor #1 positive terminal ⁽¹⁾
7	CAP1	0	Capacitor to VSS
8	REGOUT	Р	Output LDO
9	REGSRC	1	Input source for output LDO
10	VC5X	Р	Thermistor #2 negative terminal
11	NC	_	No connect (short to CAP2)
12	NC	_	No connect (short to CAP2)
13	TS2	Ī	Thermistor #2 positive terminal ⁽¹⁾
14	CAP2	0	Capacitor to VC5X
15	VC10X	Р	Thermistor #3 negative terminal
16	NC		No connect (short to CAP3)

	NAME	TYPE	DESCRIPTION
17	NC	_	No connect (short to CAP3)
18	TS3	- 1	Thermistor #3 positive terminal ⁽¹⁾
19	CAP3	0	Capacitor to VC10X
20	BAT	Р	Battery (top-most) terminal
21	NC	_	No connect
22	NC	_	No connect
23	NC	_	No connect
24	VC15	1	Sense voltage for 15th cell positive terminal
25	VC14	- 1	Sense voltage for 14th cell positive terminal
26	VC13	- 1	Sense voltage for 13th cell positive terminal
27	VC12	- 1	Sense voltage for 12th cell positive terminal
28	VC11	- 1	Sense voltage for 11th cell positive terminal
29	VC10B	- 1	Sense voltage for 10th cell negative terminal
30	VC10	1	Sense voltage for 10th cell positive terminal
31	VC9	1	Sense voltage for 9th cell positive terminal
32	VC8	1	Sense voltage for 8th cell positive terminal
33	VC7		Sense voltage for 7th cell positive terminal
34	VC6	1	Sense voltage for 6th cell positive terminal
35	VC5B	1	Sense voltage for 6th cell negative terminal
36	VC5	- 1	Sense voltage for 5th cell positive terminal
37	VC4	- 1	Sense voltage for 4th cell positive terminal
38	VC3	1	Sense voltage for 3rd cell positive terminal
39	VC2	1	Sense voltage for 2nd cell positive terminal
40	VC1	1	Sense voltage for 1st cell positive terminal
41	VC0	1	Sense voltage for 1st cell negative terminal
42	SRP	1	Negative current sense (nearest VSS)
43	SRN	1	Positive current sense



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