High-Voltage Auxiliary Power Supply Using Series-Connected MOSFETs and Floating Self-Driving Technique

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***Abstract*—This paper deals with high-voltage auxiliary switching-mode power supplies (SMPSs). An overview of the state of the art is given, and a novel solution is proposed. The proposed solution is based on a single-ended flyback or forward topology with the main switch arranged as a series connection of two metal–oxide–semiconductor field-effect transistors (MOSFETs). The bottom MOSFET is driven directly by an ordinary control circuit and gate driver, while the top MOSFET is driven by a floating self-supplied gate driver. The floating gate driver is connected to the input filter capacitors' midpoint. This gate driver plays two roles: driving of the top MOSFET and control of distribution of the blocking voltage among the series-connected MOSFETs, in steady state as well as during commutation. The series connection of lower voltage MOSFETs has two important advantages compared to that of a single high-voltage MOSFET: lower conduction losses and lower cost. When several switches are series connected, each switch supports a fraction of the total blocking voltage, and therefore, each switch can be rated for lower voltage. The total ON-state resistance and the cost of such a switch arrangement are lower compared to that of a single switch that supports the full blocking voltage. The proposed SMPS is theoretically analyzed and experimentally verified. The experimental results are presented and discussed.**

***Index Terms*—Dynamic voltage-balancing circuit, gate driver, high-voltage dc–dc, power metal–oxide–semiconductor field-effect transistor (MOSFET) series connection, switching-mode power supply (SMPS).**

I. Introduction

AN AUXILIARY power supply is the heart of any power converter: variable-speed drive converter, uninterruptible power supply, active filter, or any other power processing device. The auxiliary power supply provides auxiliary voltages in the range of 3.3–48 V and powers all the analog/digital control and driving circuitry of the converter. Rated power is usually below 100 W. The input is a dc voltage in the range of 200–1200 V, even more in some special applications. The power supply size and the overall cost and efficiency are the key design issues. Nowadays, auxiliary power supplies are exclusively based on switching-mode power supplies, so-called SMPSs. The topology varies from application to application, depending on the input voltage, power rating, complexity, and so on.

This paper gives an overview of the most commonly used high-voltage auxiliary power supplies, particularly focusing on the topologies and the switch technologies. Thereafter, a novel, efficient, and cost-effective solution is proposed. An active switch arranged as a series connection of two high-voltage metal–oxide–semiconductor field-effect transistors (MOSFETs) is the core of the solution presented. The bottom MOSFET is driven directly by an ordinary control and drive circuit, while the top MOSFET is driven by a floating self-powered gate driver. The floating gate driver is connected to the input filter capacitors' midpoint and to the gate–source terminal of the top MOSFET. The input filter capacitors' midpoint is also connected to a nondissipative circuit that controls the distribution of the input voltage among series-connected input filter capacitors. The floating gate driver has two functions: 1) driving of the top MOSFET and 2) controlling the distribution of the blocking voltage among series-connected MOSFETs, in steady state as well as during commutation.

Compared to existing solutions, the newly proposed SMPS has advantages of better efficiency and lower overall cost. The nondissipative control of distribution of the input dc bus voltage among series-connected input filter capacitors is an additional advantage. The proposed SMPS is theoretically analyzed and experimentally verified. The experimental results are presented and discussed.

A. High-Voltage SMPS Topology—State of the Art

The existing low-power high-voltage SMPSs belong to two quite different groups. The first group covers standard power supplies based on ordinary flyback or forward converters [1] [see Fig.1(a)]. This kind of SMPS is the simplest and the most cost-effective solution, particularly in applications where the input dc voltage is limited to 800 V and the rated power is up to 50 W. The main drawback and a limiting factor for broad application of such a simple topology are the voltage stress of the main switch SW. Another drawback of this topology is relatively low switching frequency, which is limited by the losses on the resistor capacitor diode (RCD) clamp circuit. The RCD clamp circuit is connected in parallel with the transformer to discharge the energy stored in the transformer leakage inductance and to prevent large overvoltage during turn-off of the main switch [1].

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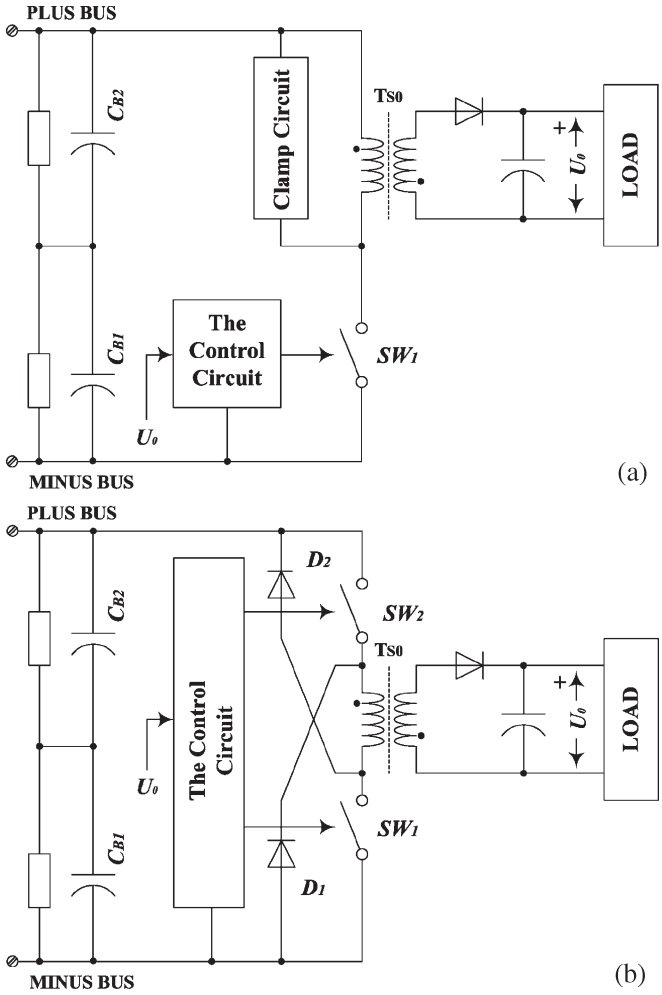

Fig. 1. SMPS based on flyback topologies. (a) Single switch and (b) asymmetric half-bridge.

Another topology from the first group, which is frequently used in applications where the input dc voltage could be up to 1200 V, is a half-bridge flyback converter [see Fig. 1(b)]. The topology provides less voltage stress of the switches and higher efficiency compared to the single-ended topology shown in Fig. 1(a).

The second group of high-voltage SMPSs belongs to the so-called input-series–output-parallel (ISOP)-connected converters. The conversion system consists of N dc–dc converters, whose inputs are series connected, while the outputs are parallel connected to the common output voltage U_0. The output parallel connection could be via magnetic field of the common transformer [2]–[5], as shown in Fig. 2(a), or a direct parallel connection of the completely isolated secondary rectifiers [6]–[9], as shown in Fig. 2(b).

Fig. 2(a) shows an SMPS based on the stacked flyback converters [2], [3]. The inputs of two flyback converters are series connected, while the outputs are parallel connected via the common transformer T_{S0}. The switches are driven synchronously from a common control circuit via isolated gate drivers. A similar solution based on a double zero-voltage-switch forward converter with active clamping is proposed in [4] and [5].

An example of two ISOP-connected converters, where the outputs are directly parallel connected, is shown in Fig. 2(b)

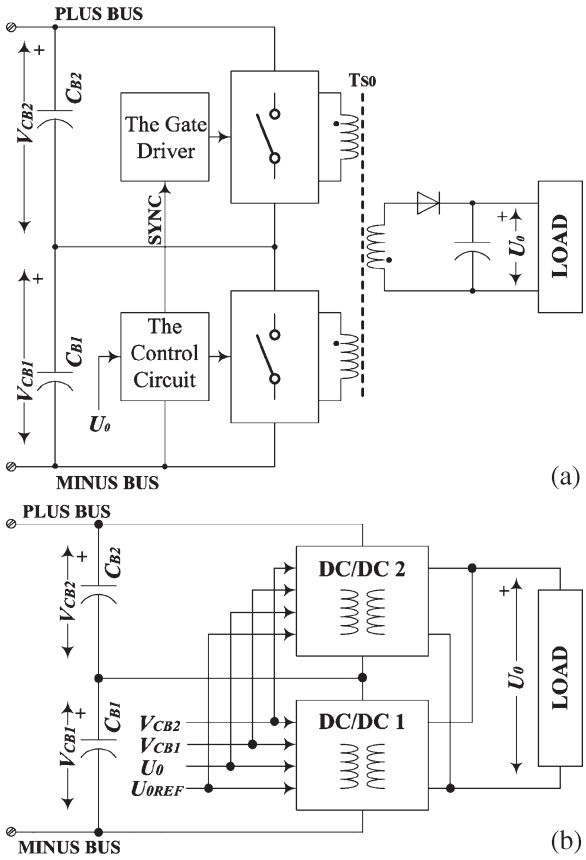

Fig. 2. ISOP-based SMPS topologies. (a) The common transformer magnetic parallel connection and (b) direct parallel connection.

[6]–[9]. When the outputs are parallel connected via magnetic field of the common transformer, the input voltages V_{CB1} and V_{CB2} are balanced automatically, owing to the transformer volt–second balance [2]. In contrast to this, the ISOP-based SMPS having directly connected outputs requires a complex control circuit that is able to control the distribution of the input voltage among the series-connected inputs [6]–[8]. A simple master/slave-based control is proposed and discussed in [9].

A topology recently coming to the focus is a multilevel topology and its derived topologies [10]–[12]. This topology is well established in high-voltage medium-power applications, while in low-power low-cost application, this is not used very often because of the cost and complexity.

B. High-Voltage Switch Arrangement

In low-power auxiliary SMPS based on single-ended flyback or forward converter, the most stressed and the most costly component is the main switch SW. The stress factor defined as a product of the peak current and peak blocking voltage is very high. Overall requirements for the switch could be summarized as follows:

1) relatively high current capability: up to 5 A for applications up to 100-W rated power;
2) high-voltage blocking capability: usually 30%–50% higher than the dc input voltage.

In three phase supplied variable speed drives and UPS applications, the required blocking voltage goes up to 1700 V;

switching losses and overall switching performance of the switch are important too, particularly in a compact SMPS design, when higher switching frequency is required. The typical switching frequency in high-voltage SMPS applications is 50–100 kHz.

Nowadays, fast semiconductor switches used in SMPS applications belong to the three main switch technology groups: high-voltage MOSFET, insulated-gate bipolar transistor (IGBT), and emitter-switched bipolar transistor (ESBT), well known as a cascode switch.

High-voltage MOSFET is a fast switching device that is superior to other switching device regarding the switching speed. It, however, suffers from a high ON-state resistance R_{Dson} which depends strongly on the rated voltage. The ON-state resistance is roughly proportional to $(BV_{\mathrm{DS}})^{2.6}$, where BV_{DS} is the breakdown voltage of the MOSFET [6]. A recently introduced MOSFET using superjunction and CollMos technology shows better performance compared to standard VMOSFETs [13]. The ON-state resistance is significantly reduced in the voltage range up to 800 V. Unfortunately, at higher voltage, there is still no significant improvement.

High-voltage IGBTs show better conduction but worse switching performances in comparison to a high-voltage MOSFET. This kind of device has found a broad application in high-power medium-switching-frequency power converters. In low-power high-switching-frequency applications, such as auxiliary SMPS applications, an IGBT is not used very often.

A hybrid high-voltage high-speed switch arranged as a series connection of a high-voltage bipolar junction transistor (BJT) and a low-voltage MOSFET was recently introduced [14]–[16]. This topology is well known as a cascode switch or recently introduced as a monolithic ESBT. This switch shows the best overall performances compared to the high-voltage MOSFET and IGBT. The major drawback of this switch is cost and the gate drive requirements. An ESBT is a four-terminal device which requires a bias circuit for the BJT and gate driver for the low-voltage MOSFET. This makes an ESBT switch less attractive in low-cost compact SMPS design.

II. SMPS Topology Based on Series-Connected Gate-Insulated Devices

A high-voltage switch made by a higher number of series-connected gate-insulated devices is often used in high-voltage high-power applications [17], [18]. Series connection of MOSFETs is utilized in specific low-power high-voltage high-switching-frequency applications [19], [20]. This concept has some advantages compared to other high-voltage switch arrangements. When a higher number of MOSFET devices are series connected, each device supports a fraction of the total blocking voltage. Let us consider N series-connected devices, which share equally the total blocking voltage. The equivalent ON-state resistance can be computed by taking into account the fact that a high-voltage MOSFET ON-state resistance is roughly proportional to $(BV_{\mathrm{DS}})^{2.6}$ [6]

$$\sum R_{\mathrm{DS}} = \frac{1}{N^{1.6}} \cdot R_{\mathrm{DS(HV)}} \tag{1}$$

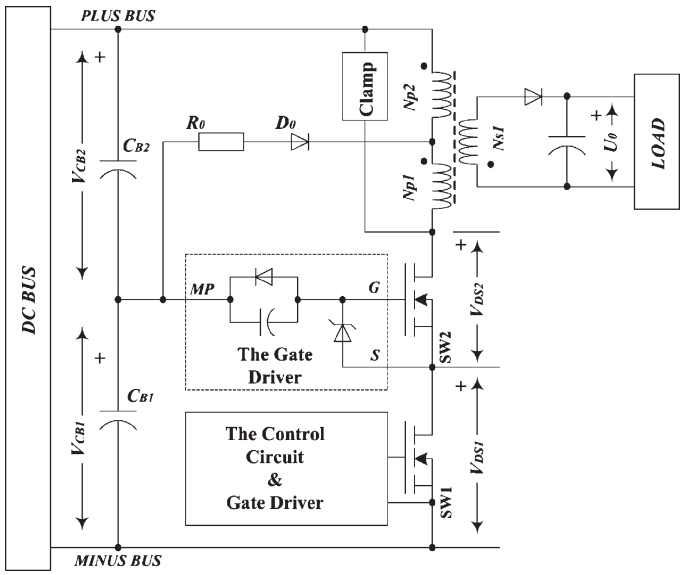

Fig. 3. Simplified block diagram of the proposed SMPS topology.

where $R_{\mathrm{DS(HV)}}$ is the on-resistance of a single device that supports the full blocking voltage and N is the number of the series-connected devices. It can be seen from (1) that the total ON-state resistance of such a switch is lower compared to a single device that supports the full blocking voltage.

To ensure dynamic as well as static distribution of the total blocking voltage among the series-connected devices, active gate drivers are required to actively drive and control the floating gate insulated devices [17]. In low-cost applications, which are discussed in this paper, this kind of active gate driving technique is not acceptable due to the total cost and complexity. A simple capacitive gate driving technique for the stacked MOSFETs is proposed in [19] and [20]. The method is cost effective and simple for implementation. Voltage across each series-connected device depends on the capacitance of the capacitor divider and the device parasitic capacitance. This, however, makes it difficult to control the blocking voltage when the device parasitic capacitance varies a lot. In addition, the steady-state blocking voltages are not well controlled, and therefore, an additional dissipative balancing circuit is required.

An auxiliary high-voltage SMPS based on asymmetric neutral point clamped (NPC) and flying capacitor topologies is presented in [21] and [22]. The switches' transient blocking voltage is determined by the input intermediate voltages, in the same way as an ordinary NPC converter operates. However, since the asymmetric NPC converter is not able to control and balance the input intermediate voltages, an additional dissipative balancing circuit is used. This makes the solution in [21] less attractive in compact SMPS applications.

III. New Solution for Series Connection of Power MOSFETs

A high-voltage switch arranged as two series-connected MOSFETs associated with the series-connected input filter capacitors is a core of the solution proposed in [23] and [24]. A simplified circuit diagram of this solution is shown in Fig. 3. The SMPS is composed of two series-connected input filter

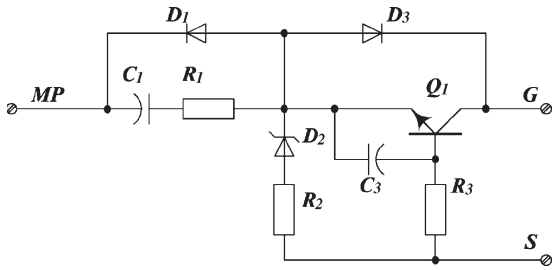

Fig. 4. Circuit diagram of the top-side gate driver.

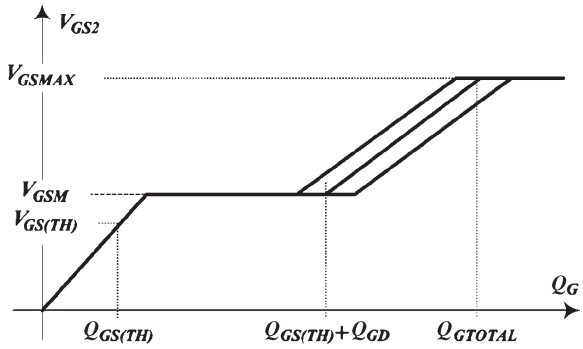

Fig. 5. MOSFET gate charge profile.

capacitors C_{B1} and C_{B2}, a high-voltage switch arranged as series-connected MOSFETs SW_1 and SW_2, associated gate drivers, and an output voltage control circuit. The role of diode D_0 and resistor R_0 is not important at the moment. It will be explained in Section IV.

The bottom MOSFET SW_1 is driven directly by an integrated gate driver, while the top MOSFET SW_2 is driven via a floating three-terminal gate driver.

The floating gate driver plays the following roles:

1) fast switch-on and switch-off of the top MOSFET;
2) control of the switches' blocking voltages in steady state as well as during the transients.

Fig. 4 shows a schematic diagram of a gate driver that satisfies the requirements. The driver consists of the coupling capacitor C_1, damping resistor R_1, turn-off bypass diode D_1, gate protection diode D_2, turn-on speed-up diode D_3, gate filter R_3C_3, resistor R_2, and turn-off transistor Q_1. The terminal designated as MP (midpoint) is connected to the input filter capacitors' midpoint. The terminals G and S are connected to the gate and source of the top MOSFET SW_2.

A. Turn-On

The simplest method to analyze turn-on is to use the gate charge profile. A typical gate charge profile of a gate-isolated device is shown in Fig. 5.

The charge $Q_{\mathrm{GS(TH)}}$ is a charge that is required to elevate the gate–source voltage from zero to the threshold voltage $V_{\mathrm{GS(TH)}}$. The value designated as Q_{GD} represents a charge that covers the gate–drain displacement current and charges the nonlinear gate–drain capacitance while the drain–source voltage varies, either falls or rises. The third part is the total gate charge, designated as Q_{GTOTAL}, which represents the charge injected into the gate to boost the gate–source voltage to the maximum V_{GSMAX}.

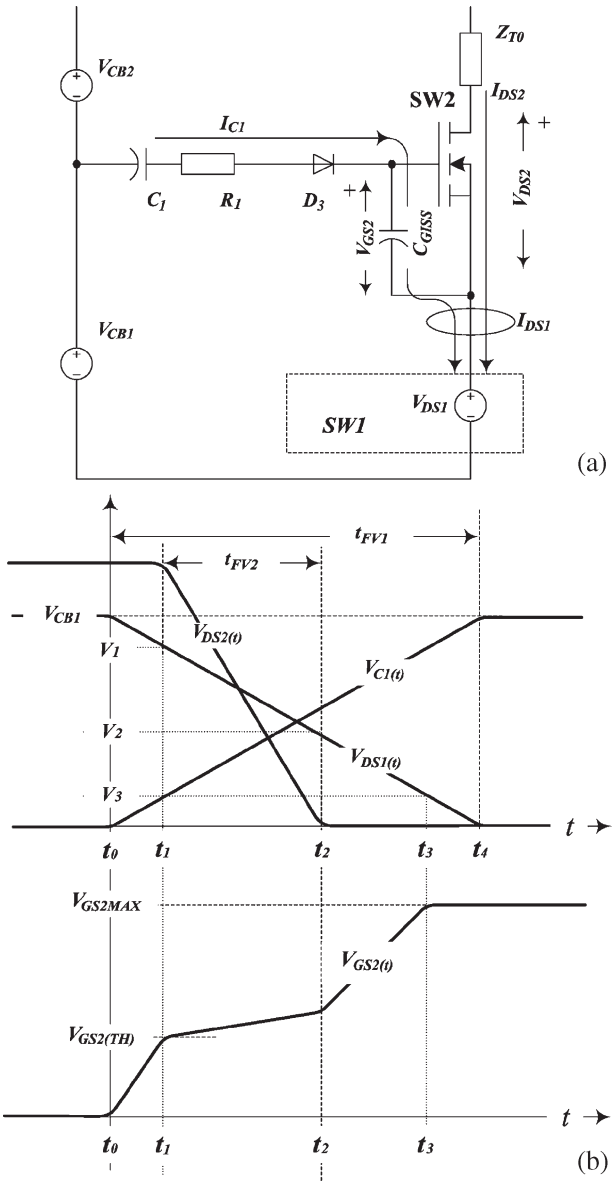

Fig. 6. Turn-on of the top MOSFET.

A simplified equivalent circuit diagram that will be used in the analysis is shown in Fig. 6(a). A sketch of the drain–source voltages V_{DS1} and V_{DS2}, the capacitor voltage V_{C1}, and the gate–source voltage V_{GS2} waveforms is shown in Fig. 6(b). The input filter capacitors C_{B1} and C_{B2} are modeled as voltage sources V_{CB1} and V_{CB2}. This is a reasonably accurate approximation since the time constant of the input filter is much greater than the switching period T_{SW}. The SMPS transformer and the RCD clamp circuit are modeled by the impedance Z_{T0}.

The bottom MOSFET SW_1 is modeled as a voltage source V_{DS1}

$$V_{\mathrm{DS1}} = \begin{cases} V_{\mathrm{CB1}}, & t \le 0 \\ V_{\mathrm{CB1}}\left(1 - \frac{t}{t_{\mathrm{FV1}}}\right), & 0 < t \le t_{\mathrm{FV1}} \\ 0, & t_{\mathrm{FV1}} \le t \end{cases} \tag{2}$$

where the fall time t_{FV1} is determined by the bottom gate driver. V_{CB1} is the bottom filter capacitor voltage.

At the moment t_0, the bottom MOSFET SW_1 begins commutation. The drain–source voltage V_{DS1} falls, and the capacitor C_1 is charged by the current I_{C1} through the resistor R_1, diode D_3, and the gate capacitance C_{GISS}. Therefore, the gate–source voltage V_{GS2} rises. The gate charge Q_{GS} required to elevate the gate–source voltage from zero to threshold voltage $V_{\mathrm{GS(TH)}}$ is

$$Q_{\mathrm{GS(TH)}} = C_1(\Delta V_{\mathrm{DS1}} - V_{\mathrm{TH}}) = C_1(V_{\mathrm{CB1}} - V_1 - V_{\mathrm{TH}}) \quad (3)$$

where $Q_{\mathrm{GS(TH)}}$ is the gate charge of the MOSFET SW_2 and ΔV_{DS1} is variation of the bottom MOSFET drain–source voltage. The voltage designated as V_1 is the drain–source voltage at the moment t_1 [see Fig. 6(b)]. The significance of this voltage will be described shortly after.

Once the gate–source voltage V_{GS2} has reached the threshold voltage $V_{\mathrm{GS(TH)}}$, the drain current I_{D2} starts to flow and discharges the gate–drain and drain–source capacitances. The drain–source voltage V_{DS2} falls. The fall time is t_{FV2}. The gate–source voltage V_{GS2} increases slightly during this period, but much slower than before because of the Miller's effect. From Fig. 6(b), one can find the following relationship:

$$\frac{V_{\mathrm{CB1}}}{t_{\mathrm{FV1}}} = \frac{V_1 - V_2}{t_2 - t_1} = \frac{V_1 - V_2}{t_{\mathrm{FV2}}} \quad (4)$$

where V_1 and V_2 are the bottom MOSFET drain–source voltages at the moments t_1 and t_2 [see Fig. 6(b)]. From the gate circuit follows

$$\Delta Q_{C1} = (V_1 - V_2)C_1 = Q_{\mathrm{GD}} \quad (5)$$

where Q_{GD} is the gate–drain charge given as a parameter of the MOSFET. Inserting (5) into (4) yields a relationship between the fall times t_{FV1} and t_{FV2}

$$t_{\mathrm{FV2}} = t_{\mathrm{FV1}} \left(\frac{Q_{\mathrm{GD}}}{C_1 V_{\mathrm{CB1}}} \right). \quad (6)$$

The top MOSFET SW_2 is fully switched on at the moment t_2. Since the drain–source voltage is zero and remains constant, the drain–gate displacement current is zero, and therefore, the gate–source voltage starts to increases faster. The gate–source voltage reaches the maximum V_{GSMAX} at the moment t_3. The bottom drain–source voltage V_{DS1} at that moment is V_3. The total gate charge Q_{TOTAL} is computed as

$$Q_{\mathrm{TOTAL}} = C_1(V_{\mathrm{CB1}} - V_3 - V_{\mathrm{GSMAX}}) \quad (7)$$

where V_{GSMAX} is maximum of the gate–source voltage determined by the external clamping Zener diode D_2. To ensure that the gate–source is charged to the maximum, V_{GSMAX}, the voltage V_3 must be > 0. The bottom MOSFET SW_1 is fully switched on at the moment t_4, and the commutation is finished. The capacitor C_1 is charged on the voltage $V_{C1} = V_{\mathrm{CB1}} - V_{\mathrm{GSMAX}}$.

Let us now explain the significance of the voltage V_1 in (3). The value of this voltage is more or less irrelevant in a hypothetical case, when the SMPS transformer and the clamping circuit are modeled as a current source or a pure inductance. In the real case, however, the transformer primary winding has a significant parasitic capacitance. This capacitance holds the total drain–source voltage, $V_{\mathrm{DS}} = V_{\mathrm{DS1}} + V_{\mathrm{DS2}}$, which is constant during a short period $t_1 - t_0$. As the voltage V_{DS1} decreases, the voltage V_{DS2} must increase for the same value. To prevent the voltage V_{DS2} from increasing above the breakdown voltage, the voltage V_1 has to be as high as possible. Based on experience, one can define a condition $V_1 \geq 0.9 V_{\mathrm{CB1\,max}}$.

The capacitor C_1 selection criterion is obtained from (3), (6), and (7) as

$$C_1 = \max\left\{ \frac{Q_{\mathrm{GS(TH)}}}{(V_{\mathrm{CB1}} - V_1 - V_{\mathrm{TH}})}; \frac{t_{\mathrm{FV1}}}{t_{\mathrm{FV2}}} \frac{Q_{\mathrm{DG}}}{V_{\mathrm{CB1}}}; \frac{Q_{\mathrm{TOTAL}}}{(V_{\mathrm{CB1}} - V_{\mathrm{GSMAX}})} \right\} \quad (8)$$

where the charges $Q_{\mathrm{GS(TH)}}$, Q_{DG}, and Q_{TOTAL} are given in the MOSFET date sheet as parameters.

The energy of the capacitor C_1 is dissipated as power losses on the bottom MOSFET and partially on the damping resistor R_1. To compute the power losses, let us first compute the average current that flows from the filter capacitors' midpoint

$$I_{C1} = \frac{1}{T_{\mathrm{SW}}} \int_0^T i_c dt = f_{\mathrm{SW}} Q_{C1} = f_{\mathrm{SW}} \frac{1}{2} C_1 (V_{\mathrm{CB1}} - V_{\mathrm{GSMAX}}). \quad (9)$$

Now, the power dissipation is computed as

$$P_{C1} = I_{C1} \cdot V_{\mathrm{CB1}} \cong f_{\mathrm{SW}} \frac{1}{2} C_1 (V_{\mathrm{CB1}})^2. \quad (10)$$

B. Turn-Off

For simplicity of the analysis, the SMPS transformer primary current I_p is assumed to be constant during a short period of commutation. Discontinuous conduction mode (DCM) of the SMPS is considered too. The bottom MOSFET SW_1 is modeled in the same way as before; as a voltage source V_{DS1}

$$V_{\mathrm{DS1}} = \begin{cases} 0, & t \leq 0 \\ V_{\mathrm{CB1}} \frac{t}{t_{\mathrm{RV1}}}, & 0 < t \leq t_{\mathrm{RV1}} \\ V_{\mathrm{CB1}}, & t_{\mathrm{RV1}} \leq t \end{cases} \quad (11)$$

where the rise time t_{RV1} is determined by the bottom gate driver. V_{CB1} is the bottom filter capacitor voltage. This model is reasonably accurate if the drain current, in this case the primary current I_p, is high enough to charge the Miller's capacitance. In this case, the drain–source voltage rise time t_{RV1} is defined by the gate resistance and the MOSFET parasitic capacitances.

The equivalent circuit diagram and a sketch of the waveforms are shown in Fig. 7. At the moment t_0, the MOSFET SW_1 is switched-off and the voltage V_{DS1} starts to rise, while the voltage across the capacitor C_1 falls with the same rate. The capacitor C_1 is discharged with the current I_{C1} through diode D_2. At the moment t_3, the voltage V_{DS1} reaches V_{CB1}, and the diode D_1 begins to conduct. At that moment, the capacitor C_1 is completely discharged and bypassed by the diode D_1. Once the voltage V_{DS1} stabilizes at V_{CB1}, the drain current I_{DS1} of the bottom MOSFET starts falling. At the moment t_4, the current I_{DS1} reaches zero, and the MOSFET SW_1 is fully switched off.

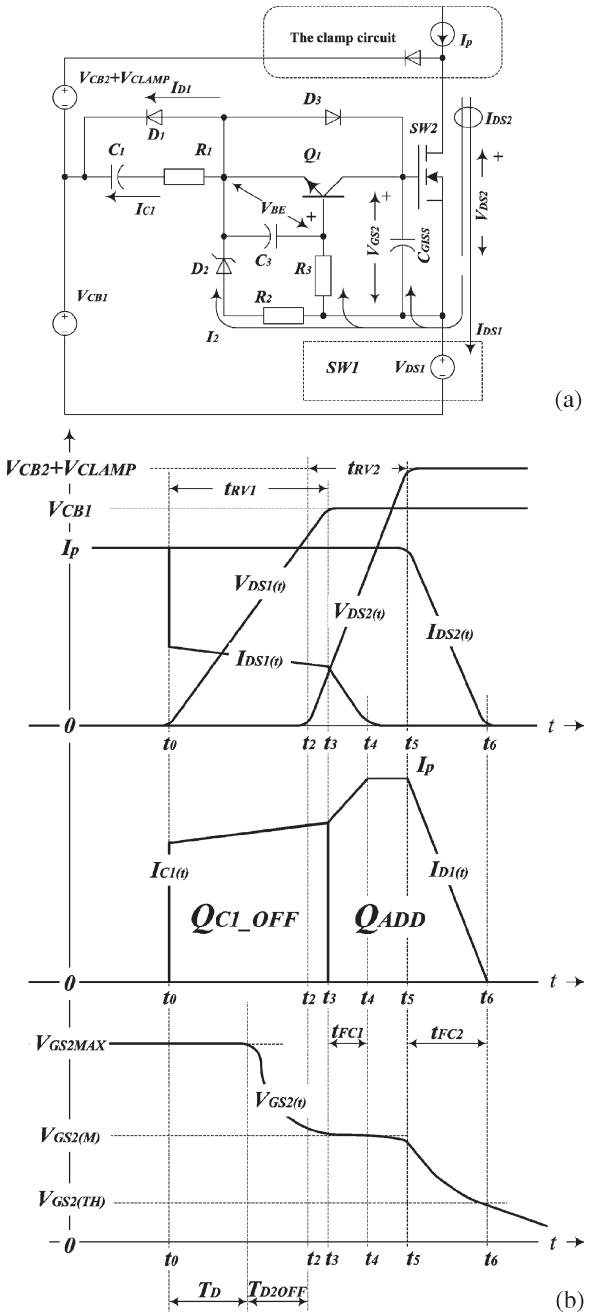

Fig. 7. Turn-off of the top-side MOSFET.

The load current I_p is completely diverted to the bus capacitors' midpoint via the diodes D_1 and D_2.

In parallel with this process, and since moment t_0, the capacitor C_3 is charged through the resistor R_3. The base–emitter voltage of transistor Q_1 therefore rises. At the moment t_1, the base–emitter voltage reaches threshold voltage $V_{\mathrm{BE(TH)}}$ and the transistor Q_1 is switched on. The gate–source capacitance C_{GISS} is then discharged through the transistor Q_1, and the gate–source voltage V_{GS2} decreases. The gate–source voltage reaches the Miller's plateau at the moment t_2, and the drain–source voltage V_{DS2} starts to rise; commutation of the MOSFET SW_2 begins. At the moment t_6, the gate–source voltage reaches the threshold voltage $V_{\mathrm{GS(TH)}}$, the drain current I_{DS2} drops to zero, and the commutation is completed.

The total charge injected in the filter capacitors' midpoint is the charge of the capacitor C_1 and the additional charge due to conduction of the bypass diode D_1

$$Q_{\mathrm{INJ}} = Q_{C1\_\mathrm{ON}} + Q_{C1\_\mathrm{OFF}} + Q_{\mathrm{ADD}}. \tag{12}$$

To satisfy the capacitor charge balance, the total charge of the capacitor C_1 must be zero in steady state. Hence, the charge injected in the midpoint over the switching period T_{SW} is equal to the additional charge Q_{ADD}

$$Q_{\mathrm{INJ}} = Q_{\mathrm{ADD}}. \tag{13}$$

The average current I_{ADD} injected in the filter capacitors' midpoint is

$$\begin{aligned} I_{\mathrm{ADD}} &= \frac{1}{T_{\mathrm{SW}}} \cdot Q_{C1\_\mathrm{ON}} + \frac{1}{T_{\mathrm{SW}}} \left(\int_{t0}^{t3} I_{C1}(t)dt + \int_{t3}^{t6} I_{D1}(t)dt \right) \\ &= f_{\mathrm{SW}} \cdot Q_{\mathrm{ADD}} \end{aligned} \tag{14}$$

where f_{SW} is the switching frequency.

The additional charge Q_{ADD} computed in Fig. 7(b) is

$$\begin{aligned} Q_{\mathrm{ADD}} &= I_p \left(\frac{t_{\mathrm{FC1}}}{2} + \frac{t_{\mathrm{FC2}}}{2} + t_5 - t_4 \right) \\ &= I_p \left(\frac{t_{\mathrm{FC2}}}{2} - \frac{t_{\mathrm{FC1}}}{2} + t_{\mathrm{RV2}} - t_{\mathrm{RV1}} + T_D + T_{\mathrm{D2OFF}} \right) \end{aligned} \tag{15}$$

where I_p is the transformer current, t_{FC1} and t_{FC2} are fall times of the bottom and top MOSFET drain current, t_{RV1} and t_{RV2} are rise times of the bottom and top MOSFET drain–source voltage, $T_D = t_1 - t_0$ is the command delay time, and $T_{\mathrm{DOFF}} = t_2 - t_1$ is the top MOSFET turn-off delay time.

To compute the command delay time T_D, the base circuit in Fig. 7(a) is used. Let us consider that the bottom MOSFET SW_1 is conducting. The top MOSFET SW_2 gate–source voltage is $V_{\mathrm{GS2\,max}}$, clamped by the Zener diode D_2. This voltage is reflected to the base–emitter junction of the transistor Q_1 via the resistor R_3. As the voltage $V_{\mathrm{GS2\,max}}$ is normally greater than the reverse base–emitter breakdown voltage $V_{\mathrm{BE(BR)}}$, the base–emitter junction is in breakdown. The base current is limited by the resistor R_3, and therefore, one can consider that the base–emitter junction works as a Zener diode. The capacitor C_3, which is parallel connected with the base–emitter, is charged on the voltage $-|V_{\mathrm{BE(BR)}}|$. As the reverse base–emitter breakdown voltage is negative (for NPN transistor), the abs notation is used to avoid misunderstanding.

Once the bottom MOSFET SW_1 starts commutation, the drain–source voltage V_{DS1} begins to rise, causing current I_2 through the capacitor C_1 and resistor R_2. At that moment, the turn-on bypass diode D_3 is blocked. The capacitor C_3 is charged from the initial voltage $v_{C3}(0) = -|V_{\mathrm{BE(BR)}}|$ via the resistor R_3. The voltage of the capacitor C_3, which is equal to the base–emitter voltage, is

$$\begin{aligned} v_{C3} = v_{\mathrm{BE}}(t) = &- \left(|V_{\mathrm{BE(BR)}}| + R_2 I_2 + V_D \right) \\ &\times \exp\left(-\frac{t}{R_3 C_3} \right) + R_2 I_2 + V_D \end{aligned} \tag{16}$$

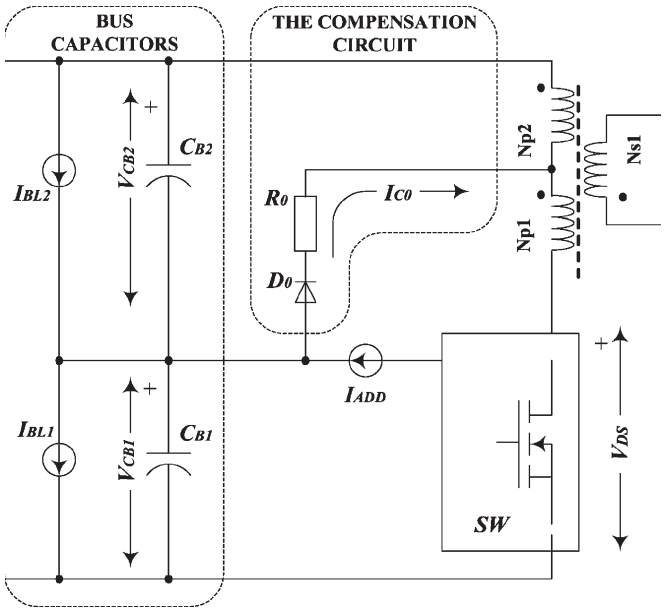

Fig. 8. Compensation circuit.

where V_D is the forward voltage of the diode D_2 and the current I_2 is approximated as

$$I_2 \cong C_1 \frac{V_{C1}}{t_{\mathrm{RV1}}}. \tag{17}$$

At the moment t_1, the base–emitter voltage reaches the threshold voltage, and the transistor Q_1 is turned on. The command delay time T_D is finished. Substituting (17) and the condition $v_{\mathrm{BE}}(T_D) = V_{\mathrm{BE(ON)}}$ into (15) yields the command delay time T_D

$$T_D = -R_3 C_3 \cdot \ln\left(\frac{R_2 C_1 \frac{V_{C1}}{t_{\mathrm{RV1}}} + V_D - V_{\mathrm{BE(ON)}}}{R_2 C_1 \frac{V_{C1}}{t_{\mathrm{RV1}}} + V_D + \left|V_{\mathrm{BE(BR)}}\right|}\right) \tag{18}$$

where $V_{\mathrm{BE(ON)}}$ is the base–emitter threshold voltage.

IV. Voltage Balancing Issue

As a result of injection of the current I_{ADD} (14) in the filter capacitors' midpoint, the bottom capacitor voltage V_{CB1} has a tendency to increase. The voltage V_{CB1} will increase until the destruction of the bottom capacitor or the bottom MOSFET SW_1. To prevent such a failure, an additional balancing circuit, either passive or active, is mandatory. An active loss-free balancing circuit is proposed in [24]. The basic circuit diagram of that solution is shown in Fig. 8. One can distinguish the input filter capacitor arranged as a series connection of two capacitors, the compensation circuit, primary side of an SMPS transformer, a switch SW, and a current source I_{ADD}.

The compensation circuit is composed of the compensation diode D_0 and resistor R_0 that are connected to the transformer midpoint. The switch SW represents a high-voltage switch made by two series-connected MOSFETs, as it has been described in Section III. The current source I_{ADD} represents a current injected from the top-side gate driver, as it was mentioned in Section III in (14). The capacitor leakage currents are modeled by current sources I_{BL1} and I_{BL2}. In the application that is discussed, the input capacitors are high-quality polypropylene capacitors with no leakage current. In some application, however, the filter capacitor is arranged as a series connection of two electrolytic capacitors that have significant leakage current [24].

Let us assume that the switch SW is closed. The switch voltage V_{DS} is equal to zero, and the voltage across the transformer primary winding N_{P2} is positive according to the connection diagram in Fig. 8. The bottom capacitor is charged by the current I_{ADD}, and the voltage V_{CB1} increases. Since the total dc bus voltage $V_{\mathrm{BUS}} = V_{\mathrm{CB1}} + V_{\mathrm{CB2}}$ is assumed to be constant, the voltage V_{CB2} of the top capacitor C_{B2} decreases. If the voltage V_{CB2} is lower than the primary voltage V_{P2}, the diode D_0 conducts and the compensation current I_{C0} flows from the midpoint of the filter capacitors through the primary winding N_{P2}. This current charges the top capacitor C_{B2} and discharges the bottom capacitor C_{B1}. During the complementary state, when the switch SW is opened, the voltage on the primary winding turns negative to ensure demagnetization of the transformer. The compensation diode D_0 blocks, and the compensation current I_{C0} falls to zero.

The capacitor voltages are constant in equilibrium. Hence, all the currents injected into and sunk from the midpoint of the capacitors are in balance. The voltage across the top capacitor C_{B2} is roughly equal to the primary voltage V_{P2}. The bottom capacitor voltage V_{CB1} can be computed as

$$V_{\mathrm{CB1}} \cong V_{\mathrm{BUS}} \frac{N_{P1}}{N_{P1}+N_{P2}} + (I_{\mathrm{ADD}} + I_{\mathrm{BL2}} - I_{\mathrm{BL1}}) \frac{R_0}{d_1} \tag{19}$$

where d_1 is the switch duty cycle, I_{ADD} is the current injected in the capacitors' midpoint by the top gate driver, and I_{BL1} and I_{BL2} are the filter capacitor leakage currents. The ratio between the primary turns N_{P1} and N_{P2} is chosen in such a way to achieve a desired ratio between the bottom- and top-side bus capacitor voltages

$$\frac{N_{P2}}{N_{P1}} = \frac{V_{\mathrm{BUS\,max}}}{\left(V_{\mathrm{DS1\,max}} - V_{\mathrm{GS\,max}} - (I_{\mathrm{ADD}} + I_{\mathrm{BL2}} - I_{\mathrm{BL1}}) \frac{R_0}{d_1}\right)} - 1 \tag{20}$$

where $V_{\mathrm{BUS\,max}}$ is the maximum bus voltage, V_{DS1} is the maximum blocking voltage of the bottom-side MOSFET, and $V_{\mathrm{GS\,max}}$ is the maximum of the gate–source voltage.

V. Experimental Results

The proposed SMPS was experimentally verified on a laboratory setup. The setup, whose circuit diagram is shown in Fig. 9, consists of a high voltage supply, two series-connected filter capacitors of 270 μF/450 V each, and 36-W auxiliary power supply in flyback topology operating at 50 kHz in DCM. The MOSFETs are 800-V and 2-A rated devices in TO252 package. The bottom gate driver and the output voltage control circuit are a widely used integrated control circuit from the UC28xx family, while the top-side gate driver is a custom-made circuit described in Section II. Several tests under different conditions

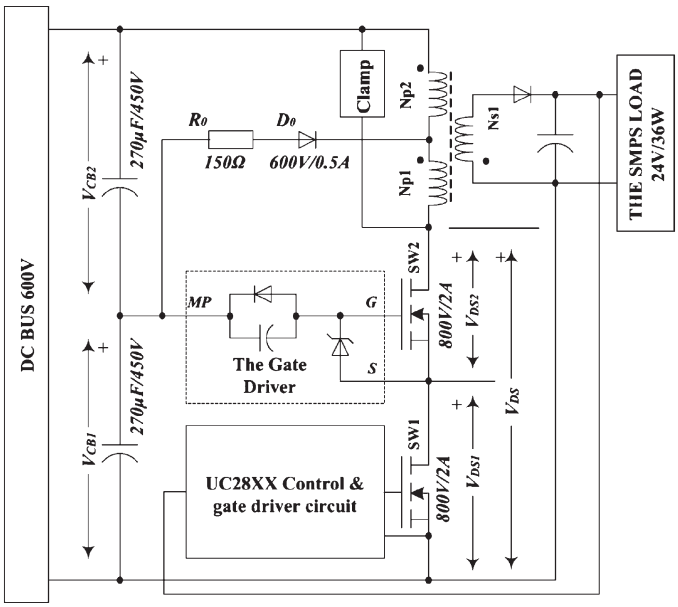

Fig. 9. Experimental setup.

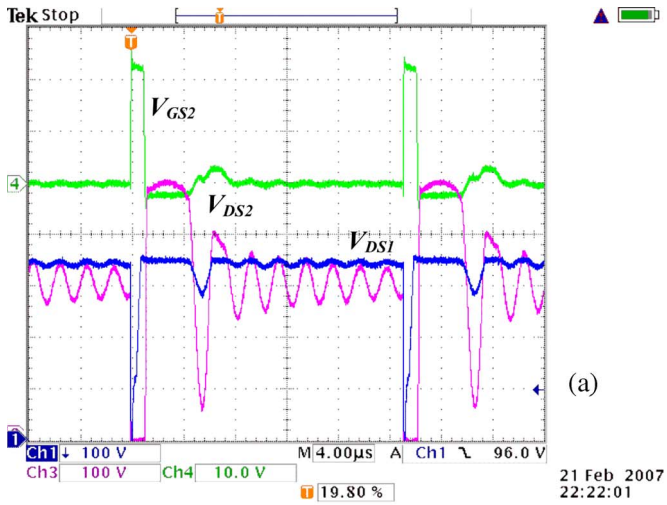

Fig. 10. V_{DS1}(CH1), V_{DS2}(CH3), and V_{GS2}(CH4). The bus voltage $V_{\mathrm{BUS}} = 600$ V. (a) Light load and (b) heavy load.

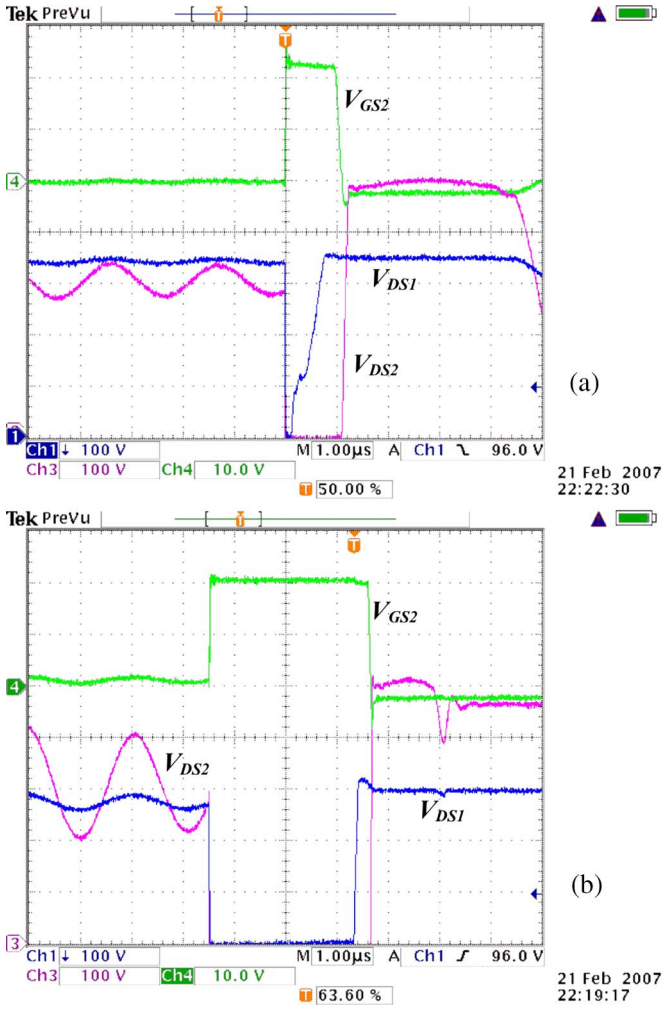

Fig. 11. V_{DS1}(CH1), V_{DS2}(CH3), and V_{GS2}(CH4). The bus voltage $V_{\mathrm{BUS}} = 600$ V. (a) Light load and (b) heavy load.

were done. The input dc bus voltage was set at the nominal value of 600 V for all the tests. The results are presented hereinafter.

Fig. 10 shows waveforms of the drain–source voltages V_{DS1} and V_{DS2} and the gate–source voltage V_{GS2}.

The waveforms have been recorded at light load and full load, as shown in Fig. 10(a) and (b), respectively. Zoom of these waveforms is shown in Fig. 11. As shown in Fig. 11(a), the bottom MOSFET is turned on for a very short time and then turned off again. The drain–source voltage V_{DS1} increases slowly because the load current I_p is not enough to charge the drain–source capacitance rapidly. In contrast to this, the top MOSFET drain–source voltage increases much faster, but with a delay T_D. Fig. 11(b) shows the waveforms for a fully loaded SMPS.

Details of turn-off waveforms when the SMPS is slightly loaded and fully loaded are shown in Fig. 12. The top MOSFET gate–source voltage waveform is clean, without any parasitic oscillation or ringing. The top MOSFET turn-off delay time T_D depends on the load. This is in contrast to (18). However, (18) has been derived under the condition that the load current is high enough to charge the equivalent drain capacitance, in which case, the drain–source voltage rise time could be considered as constant regardless of the load. This is not the

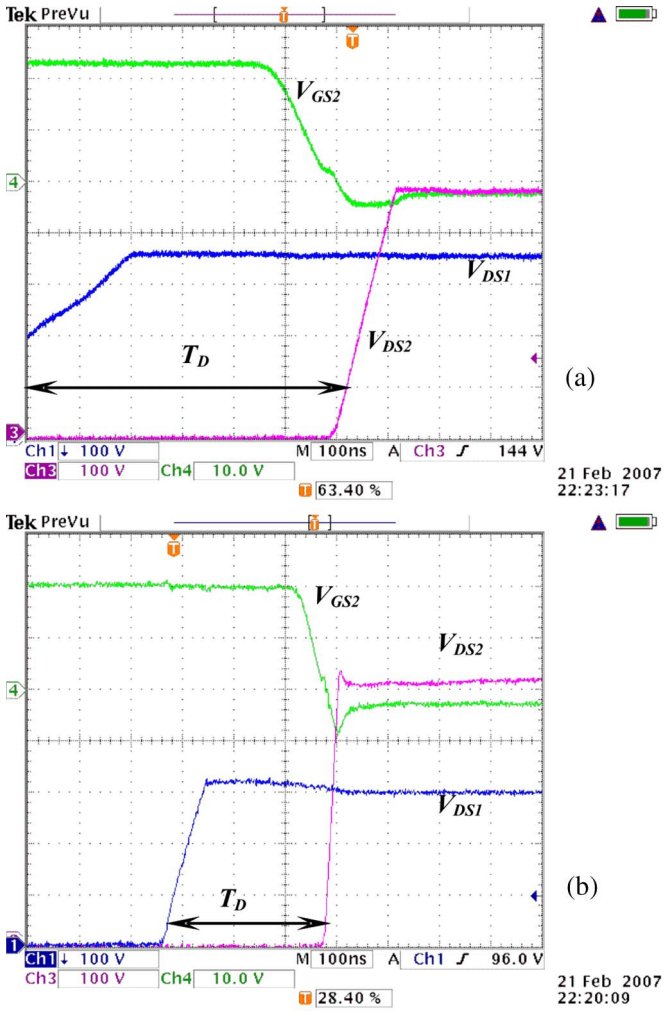

Fig. 12. V_{DS1}(CH1), V_{DS2}(CH3), and V_{GS2}(CH4). The bus voltage $V_{\mathrm{BUS}} = 600$ V. (a) Light load and (b) heavy load.

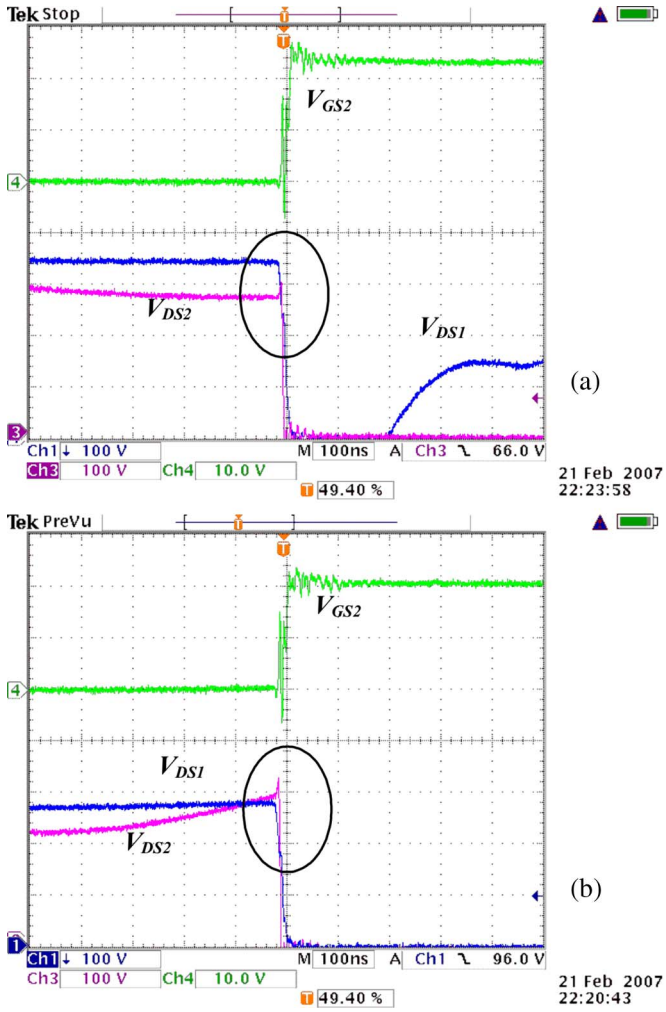

Fig. 13. V_{DS1}(CH1), V_{DS2}(CH3), and V_{GS2}(CH4). The bus voltage $V_{\mathrm{BUS}} = 600$ V. (a) Light load and (b) heavy load.

case shown in Fig. 12(a), and therefore, variation of the delay time T_D with the load is expected.

Details of turn-on waveforms are shown in Fig. 13(a) for light load and Fig. 13(b) for full load. The top and bottom drain–source voltages fall almost simultaneously. The voltage slope is quite independent on the SMPS load. The top drain–source voltage V_{DS2} shows a slight overshoot of approximately 30 V at the beginning of the commutation, and then, the voltage quickly falls to zero. This overshoot issue was discussed in Section II.

Fig. 14 shows the functionality of the input voltage balancing circuit R_0, D_0. The input capacitor voltages V_{CB1} and V_{CB2} were measured, and the voltage error ΔV_C was calculated. Fig. 14(a) shows the waveforms when the compensation circuit is disconnected. When the SMPS starts to operate, the top gate driver begins injecting the current I_{ADD} in the capacitors' midpoint. Hence, the voltage V_{CB1} and the voltage error ΔV_C increase with no control. If this is not prevented, it will finish with breakdown of the bottom capacitor C_{B1} or MOSFET SW_1. In contrast to this, when the compensation circuit is connected, the voltage error is well maintained [see Fig. 14(b)]. The initial voltage error was approximately -3 V. Then, this error increased up to -8 V due to the current injected from the top-side gate driver.

VI. Conclusion

An overview of the state of the art of high-voltage auxiliary SMPS was given, and a new topology was proposed. The proposed SMPS was theoretically analyzed and experimentally verified on a laboratory setup. The experimental results were presented and discussed. The results show a good agreement with the theoretical analysis.

The proposed topology has two important advantages compared to the existing solutions. First, the use of a series connection of two MOSFETs provides reduction of the SMPS losses, cost, and size. Second, the voltages of the input series-connected filter capacitors are balanced without an additional dissipative balancing circuit. It gives us an opportunity to use this topology as an active balancing circuit in the main dc bus, where the dc bus capacitor is arranged as a series connection of two electrolytic capacitors. It further reduces the overall cost and improves efficiency of the converter.

Future work on this solution includes the following:

1) extension of the proposed SMPS topology on higher voltage application by the use of higher number series-connected MOSFETs and the input bus capacitors;

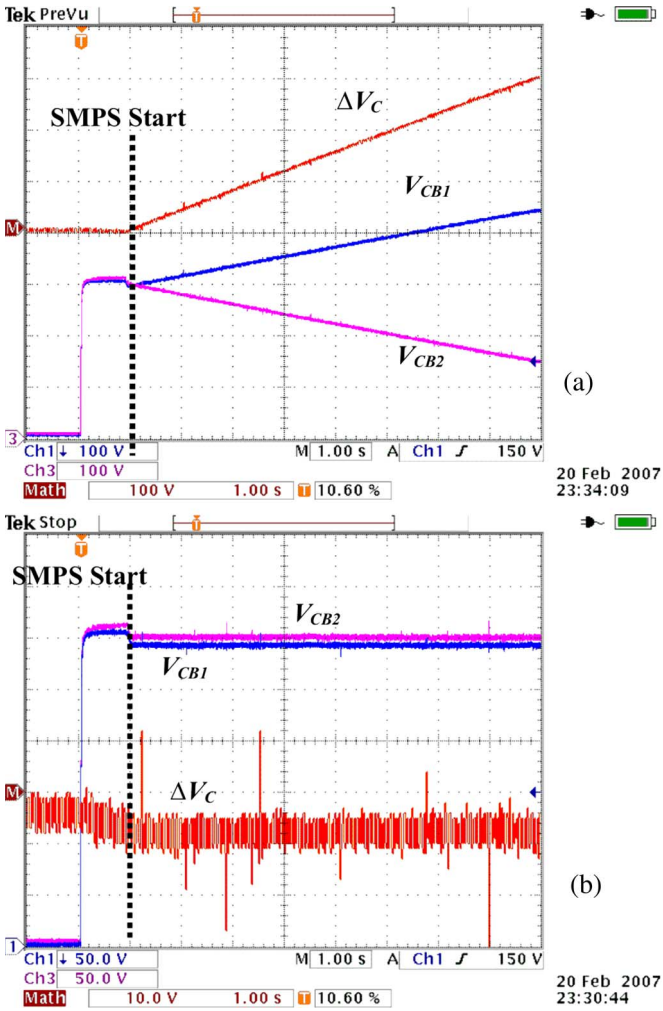

Fig. 14. V_{CB1}(CH1), V_{CB2}(CH3), and ΔV_C (Math). The SMPS nominal load, $V_{\mathrm{BUS}} = 600$ V, (a) without the compensation circuit and (b) with the compensation circuit.

2) possible improvement of the EMC behavior by adjustment of the top MOSFET turn-off delay;
3) large and small signal modeling and analysis of effects of the delay time on the output voltage controller design and the SMPS stability.

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