Analysis and design of a single-phase AC/DC step-down converter for universal input voltage

T.-J. Liang, L.-S. Yang and J.-F. Chen

Abstract: This work presents a single-phase AC/DC step-down converter, which is composed of two power stages, buck-boost converter and buck converter. The front stage is used for a power-factor-correction (PFC) circuit and is operated in discontinuous conduction mode (DCM) by using the pulse-width modulation (PWM) technique to achieve almost unity power factor and low total harmonic distortion of input current (THD_i). The rear stage is also operated in DCM to achieve voltage step-down and low DC-link voltage. The proposed converter can be applied for universal input voltage (85–265 V) and wide output power range. Also, the steady-state analysis of voltage gain and boundary operating condition are presented. Moreover, the selections of inductors, capacitors and input filter are depicted. Finally, a hardware circuit with simple control logic is implemented to illustrate the theoretical analysis.

1 Introduction

The DC source is widely used for many applications, such as DC power supply, lighting system, inverter and so on. Traditionally, the diode bridge rectifier or thyristor rectifier is used for AC/DC power conversion [1]. However, these rectifiers have some drawbacks including pulsating input current, high harmonic, high electromagnetic interference (EMI), low power factor and so on. In order to overcome these problems, some topologies have been presented [2–17]. Many boost-type converters have been proposed [2–7], but the boost types are only used for voltage step-up applications. If voltage step-down is required, these converters need to cascade with another DC/DC converter. It results in system complexity and cost increment. Hence, some single-stage circuits are presented for voltage step-down applications, such as CUK type [8, 9], boost-forward type [10], boost-flyback type [11], buck type [12, 13] and buck-boost type [14–16]. These types can achieve almost unity power factor and adjustable output voltage. Nevertheless, the DC-link voltage is higher than the peak input voltage [8–11]. The total harmonic distortion of input current (THD_i) is about 10–15% [10, 11] higher. As for the buck and buck-boost converters, the converters are operated in continuous conduction mode (CCM) with larger inductor which will result in lower power density [12–15]. Also, more control signals, such as input voltage, output voltage or inductor current, are used [12–16]. Wu presents a buck-boost converter cascaded with a flyback converter [17]. This converter, operated in discontinuous conduction mode (DCM), uses simple control logic to achieve almost unity power factor, low THD_i and adjustable output voltage. But, this converter is not suitable for universal input voltage and wide output power range.

This paper proposes a single-phase AC/DC step-down converter, which is an AC/DC buck-boost converter cascaded with a DC/DC buck converter. The proposed converter can achieve unity power factor, low THD_i, adjustable step-down output voltage for universal input voltage and wide output power range. In addition, the DC-link voltage is less than the peak input voltage. Also the buck-boost converter and buck converter are both operated in DCM by using a simple pulse-width modulation (PWM) control strategy and only a feedback control signal of output voltage is used. As the proposed converter is operated in DCM, the peak inductor current is higher. To avoid higher current stress for power semiconductor devices, this conveter is suitable for low power applications.

2 Operation principle of the proposed converter

Fig. 1 illustrates the proposed converter, which consists of two power stages. The front stage is an AC/DC buck-boost converter, and the rear stage is a DC/DC buck converter. The two stages are both operated in DCM with a fixed duty ratio by using a simple PWM controller. Two inductors L_1 and L_2 with same inductance are adopted in the front stage. L_1 and L_2 are charged by series when S_1 and S_2 are turned on, and are discharged by parallel when S_1 and S_2 are turned off. The discharged time will be shortened, namely the duty ratio can be extended. Thus, the front stage can be operated with larger duty ratio variation than the conventional buck-boost converter with DCM operation. Therefore, the front stage becomes more suitable for universal input voltage and wide output power range. Fig. 2 shows the input voltage, the unfiltered input current, the input inductor currents and the control signal for $0 < \omega t < 2\pi$, where ω is the line angular frequency. Also, some typical waveforms in one switching period are shown in Fig. 3. Owing to the symmetrical characteristics of single-phase system, the following operating principle is analysed for $0 < \omega t < \pi$.

doi:10.1049/iet-epa:20060471

Paper first received 19th November 2006 and in revised form 29th January 2007

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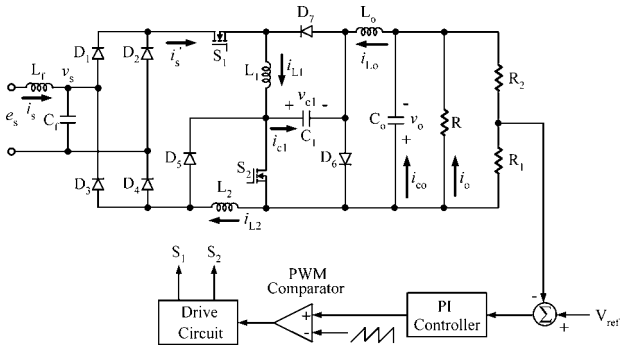

Fig. 1 *Circuit configuration of the proposed converter*

Mode 1: When S_1 and S_2 are turned on during time interval $[kT_s, t_{k1}]$, the inductors L_1 and L_2 are charged by series from line source and the energy stored in DC-link capacitor C_1 is discharged to output inductor L_o, output capacitor C_o and load. The equivalent circuit is shown in Fig. 4*a*.

Mode 2: While S_1 and S_2 are turned off during time interval $[t_{k1}, t_{k2}]$, the energies stored in L_1 and L_2 are released by parallel to C_1 and the energy stored in L_o is released to C_o and load. The equivalent circuit is shown in Fig. 4*b*.

Mode 3: While S_1 and S_2 are still turned off during time interval $[t_{k2}, t_{k3}]$. The i_{L1} and i_{L2} are equal to zero at $t = t_{k2}$. The energy stored in L_o is still transferred to C_o and load. The equivalent circuit is shown in Fig. 4*c*.

Mode 4: While S_1 and S_2 are still turned off during time interval $[t_{k3}, (k+1)T_s]$, the energy stored in L_o is released to empty at $t = t_{k3}$. The load is supplied from C_o. The equivalent circuit is shown in Fig. 4*d*.

3 Steady-state analysis of the proposed converter

For simplicity, the effectiveness of the input filter is ignored and it is assumed that the line voltage is given as follows

$$e_s(t) = v_s(t) = \sqrt{2}V_{rms}\sin\omega t = V_m \sin\omega t \qquad (1)$$

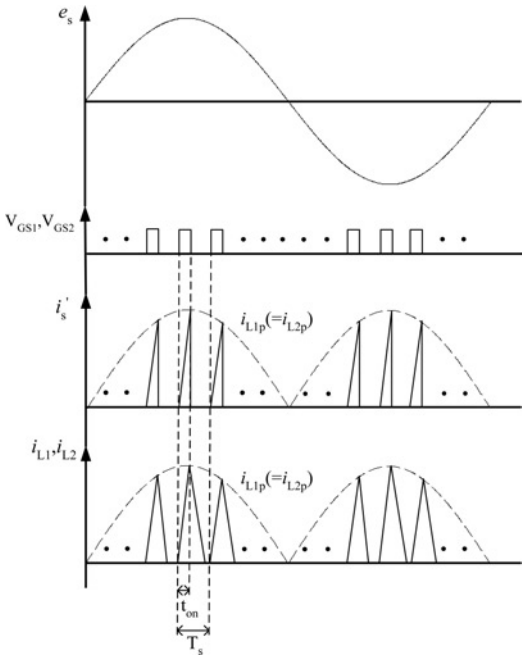

Fig. 2 *Waveforms of input voltage, unfiltered input current, inductor currents and control signal for $0 < \omega t < 2\pi$*

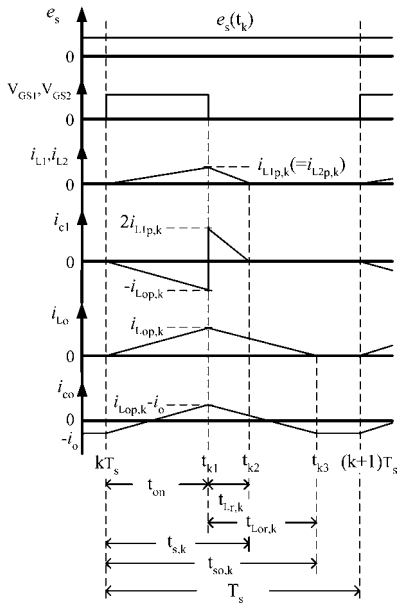

Fig. 3 *Some typical waveforms in one switching period for $0 < \omega t < \pi$*

where V_{rms} and V_m are the effective value and the amplitude of line voltage.

As the switching frequency f_s ($f_s = 1/T_s$) is much larger than the line frequency f_1, the line voltage can be considered as a piecewise constant during each switching period.

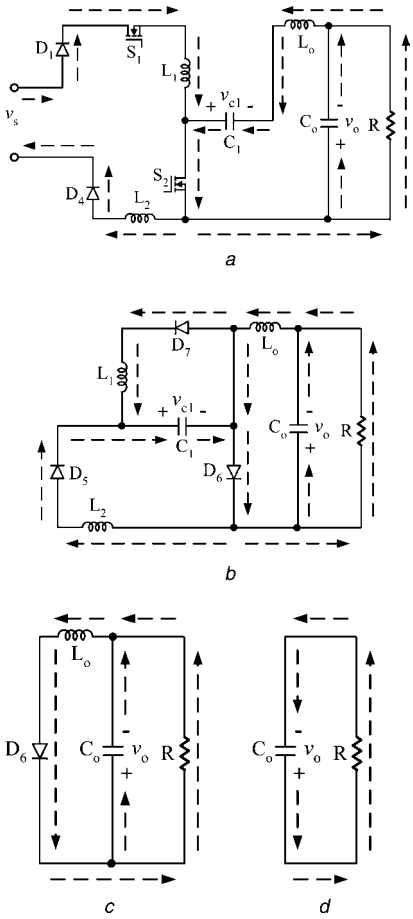

Fig. 4 *Equivalent circuit of operating principle for $0 < \omega t < \pi$*

a Mode 1
b Mode 2
c Mode 3
d Mode 4

Assuming n is the switching number within time interval $[0,\pi/\omega]$, then n is equal to $f_s/2f_1$. The following analysis is considered during the switching period $[kT_s, (k+1)T_s]$, where $k = 0,1, \ldots, n-1$, and let $L_1 = L_2 = L/2$.

When S_1 and S_2 are ON, the following equations can be obtained.

$$\begin{cases} \dfrac{di_{L1}(t)}{dt} = \dfrac{di_{L2}(t)}{dt} = \dfrac{|e_s(t_k)|}{L} \\ \dfrac{di_{Lo}(t)}{dt} = \dfrac{v_{c1} - v_o}{L_o} \end{cases}, \quad kT_s \le t \le t_{k1} \tag{2}$$

From (2), the three inductor currents i_{L1}, i_{L2} and i_{Lo} are derived as

$$\begin{cases} i_{L1}(t) = i_{L2}(t) = \dfrac{|e_s(t_k)|}{L}(t - kT_s) \\ i_{Lo}(t) = \dfrac{v_{c1} - v_o}{L_o}(t - kT_s) \end{cases}, \quad kT_s \le t \le t_{k1} \tag{3}$$

At $t = t_{k1}$, the three peak currents of L_1, L_2 and L_o can be written as

$$\begin{cases} i_{L1p,k} = i_{L2p,k} = \dfrac{|e_s(t_k)|}{L} t_{on} = \dfrac{|e_s(t_k)|}{L} dT_s \\ i_{Lop,k} = \dfrac{v_{c1} - v_o}{L_o} t_{on} = \dfrac{v_{c1} - v_o}{L_o} dT_s \end{cases} \tag{4}$$

where $t_{on} = dT_s$ and d is the duty ratio.

While S_1 and S_2 are OFF, the following equations can be obtained.

$$\begin{cases} \dfrac{di_{L1}(t)}{dt} = \dfrac{di_{L2}(t)}{dt} = -\dfrac{2v_{c1}}{L}, & t_{k1} \le t \le t_{k2} \\ \dfrac{di_{Lo}(t)}{dt} = -\dfrac{v_o}{L_o}, & t_{k1} \le t \le t_{k3} \end{cases} \tag{5}$$

Solving (5), the i_{L1}, i_{L2}, and i_{Lo} can be derived.

$$\begin{cases} i_{L1}(t) = i_{L2}(t) = \\ -\dfrac{2v_{c1}}{L}(t - t_{k1}) + i_{L1p,k}, & t_{k1} \le t \le t_{k2} \\ i_{Lo}(t) = -\dfrac{v_o}{L_o}(t - t_{k1}) + i_{Lop,k}, & t_{k1} \le t \le t_{k3} \end{cases} \tag{6}$$

As $i_{L1}(t_{k2}) = 0$, $i_{L2}(t_{k2}) = 0$ and $i_{Lo}(t_{k3}) = 0$, the peak currents of L_1, L_2 and L_o can be expressed as

$$\begin{cases} i_{L1p,k} = i_{L2p,k} = \dfrac{2v_{c1}}{L} t_{Lr,k} \\ i_{Lop,k} = \dfrac{v_o}{L_o} t_{Lor,k} \end{cases} \tag{7}$$

where $t_{Lr,k} = t_{k2} - t_{k1}$ and $t_{Lor,k} = t_{k3} - t_{k1}$.

Using (4) and (7), the following two time durations $t_{Lr,k}$ and $t_{Lor,k}$ can be obtained.

$$\begin{cases} t_{Lr,k} = \dfrac{|e_s(t_k)|}{2v_{c1}} dT_s \\ t_{Lor,k} = \dfrac{v_{c1} - v_o}{v_o} dT_s \end{cases} \tag{8}$$

3.1 Unfiltered input current i_s'

From Fig. 2, the average unfiltered input current i_s' in one switching period T_s can be derived as

$$i'_{s,avg}(t) = \frac{t_{on} i_{L1p}}{2T_s} = \frac{d^2 T_s V_m}{2L} |\sin \omega t| \tag{9}$$

Equation (9) indicates that the average unfiltered input current is sinusoidal and in phase with the input voltage. Moreover, the harmonic components of i_s' are distributed over the multiples of the switching frequency. Thus, it is very easy to filter out the harmonic components by employing a set of input filter $L_f - C_f$ with the cutoff frequency, $f_c = 1/2\pi\sqrt{(L_f C_f)}$, much lower than the switching frequency.

3.2 Voltage gain

From Fig. 3, the average currents of i_{c1} and i_{co} can be derived during the switching period $[kT_s, (k+1)T_s]$ as follows

$$\begin{cases} i_{c1,k} = \dfrac{(-i_{Lop,k}) t_{on} + 2 i_{L1p,k} t_{Lr,k}}{2T_s} \\ i_{co,k} = \dfrac{\frac{1}{2} i_{Lop,k}(t_{on} + t_{Lor,k}) - i_o T_s}{T_s} \end{cases} \tag{10}$$

Substituting (1), (4) and (8) into (10) yields

$$\begin{cases} i_{c1,k} = \dfrac{d^2 T_s V_m^2}{2L v_{c1}} \sin^2 \omega t_k - \dfrac{d^2 T_s (v_{c1} - v_o)}{2L_o} \\ i_{co,k} = \dfrac{d^2 T_s v_{c1}(v_{c1} - v_o)}{2L_o v_o} - \dfrac{v_o}{R} \end{cases} \tag{11}$$

Thus the average current of i_{c1} during time interval $[0, \pi/\omega]$ is

$$\begin{aligned} i_{c1,avg} &= \frac{\omega}{\pi} \sum_{k=0}^{n-1} i_{c1,k} T_s \\ &= \frac{\omega}{\pi} \sum_{k=0}^{n-1} \left[\frac{d^2 T_s V_m^2}{2L v_{c1}} \sin^2 \omega t_k - \frac{d^2 T_s (v_{c1} - v_o)}{2L_o} \right] T_s \end{aligned} \tag{12}$$

As $n \gg 1$, the previous equation can be approximated as

$$\begin{aligned} i_{c1,avg} &= \frac{\omega}{\pi} \int_0^{\frac{\pi}{\omega}} \left[\frac{d^2 T_s V_m^2}{2L v_{c1}} \sin^2 \omega t \right. \\ &\quad \left. - \frac{d^2 T_s (v_{c1} - v_o)}{2L_o} \right] dt \\ &= \frac{d^2 T_s V_m^2}{4L v_{c1}} - \frac{d^2 T_s (v_{c1} - v_o)}{2L_o} \end{aligned} \tag{13}$$

Therefore the differential equation of v_{c1} during time interval $[0, \pi/\omega]$ is

$$\begin{aligned} \frac{d}{dt} v_{c1} &= \frac{i_{c1,avg}}{C_1} \\ &= \frac{1}{C_1} \left[\frac{d^2 T_s V_m^2}{4L v_{c1}} - \frac{d^2 T_s (v_{c1} - v_o)}{2L_o} \right] \end{aligned} \tag{14}$$

From (11), the differential equation of v_o during one switching period is derived as

$$\frac{d}{dt} v_o = \frac{i_{co,k}}{C_o} = \frac{1}{C_o} \left[\frac{d^2 T_s v_{c1}(v_{c1} - v_o)}{2L_o v_o} - \frac{v_o}{R} \right] \tag{15}$$

Using (14) and (15), the following equation of DC model can be derived.

$$\begin{cases} \dfrac{V_m^2}{2LV_{c1}} = \dfrac{V_{c1} - V_o}{L_o} \\ \dfrac{D^2 V_{c1}(V_{c1} - V_o)}{2L_o f_s V_o} = \dfrac{V_o}{R} \end{cases} \tag{16}$$

where V_{c1}, V_o and D are the DC quantities of v_{c1}, v_o and d, respectively.

The normalised inductor time constants of the two stages are defined as

$$\begin{cases} \tau_L \equiv \dfrac{Lf_s}{R} \\ \tau_{Lo} \equiv \dfrac{L_o f_s}{R} \end{cases} \tag{17}$$

Therefore substituting (17) into (16), the voltage gains are derived as

$$M = \frac{V_o}{V_m} = M_1 M_2 \tag{18}$$

where

$$\begin{cases} M_2 = \dfrac{V_o}{V_{c1}} = \dfrac{\sqrt{D^4 + 8\tau_{Lo}D^2} - D^2}{4\tau_{Lo}} \\ M_1 = \dfrac{V_{c1}}{V_m} = \sqrt{\dfrac{L_o}{2L(1 - M_2)}} = \sqrt{\dfrac{\tau_{Lo}}{2\tau_L(1 - M_2)}} \end{cases} \tag{19}$$

3.3 Boundary condition between CCM and DCM

To ensure that the two power stages of the proposed converter are operated in DCM, the inductor currents i_{L1}, i_{L2} and i_{Lo} must go to zero in each switching period. The time duration $t_{s,k}$ is defined as the period when $i_{L1} > 0$ and $i_{L2} > 0$. Similarly, the time duration $t_{so,k}$ is defined as the period when $i_{Lo} > 0$. From Fig. 3, $t_{s,k}$ and $t_{so,k}$ can be computed as

$$\begin{cases} t_{s,k} = t_{on} + t_{Lr,k} = \dfrac{D}{f_s}\left(\dfrac{2V_{c1} + |e_s(t_k)|}{2V_{c1}}\right) \\ t_{so,k} = t_{on} + t_{Lor,k} = \dfrac{DV_{c1}}{f_s V_o} \end{cases} \tag{20}$$

When the maximum of $t_{so,k}$ is equal to T_s, the rear stage is operated in boundary conduction mode (BCM). Similarly, if the maximum of $t_{s,k}$ is equal to T_s when the absolute value of $e_s(t_k)$ is equal to V_m, the front stage is operated in BCM. From (20), the voltage gain of boundary condition can be found to be

$$M_{bc} = M_{1,bc} M_{2,bc} \tag{21}$$

where

$$\begin{cases} M_{2,bc} = D \\ M_{1,bc} = \dfrac{D}{2(1 - D)} \end{cases} \tag{22}$$

The normalised inductor time constants of boundary condition τ_{LoB} and τ_{LB} can be found when the voltage gains M_2 and M_1 are equal to the voltage gains of boundary condition $M_{2,bc}$ and $M_{1,bc}$, respectively. By using (19) and (22), τ_{LoB} and τ_{LB} can be derived as

$$\tau_{LoB} = \frac{1 - D}{2} \tag{23}$$

$$\tau_{LB} = \frac{2\tau_{Lo}(1 - D)^2}{D^2(1 - M_2)} = \frac{8\tau_{Lo}^2(1 - D)^2}{D^2(4\tau_{Lo} - \sqrt{D^4 + 8\tau_{Lo}D^2} + D^2)} \tag{24}$$

From (23), the drawing of τ_{LoB} is plotted in Fig. 5*a*. It depicts that the rear stage is operated in DCM when $\tau_{Lo} < \tau_{LoB}$. Assuming $\tau_{Lo} = 0.3$ and substituting this value into (24), the curve of τ_{LB} is plotted in Fig. 5*b*. It shows that the front stage is operated in DCM while $\tau_L < \tau_{LB}$.

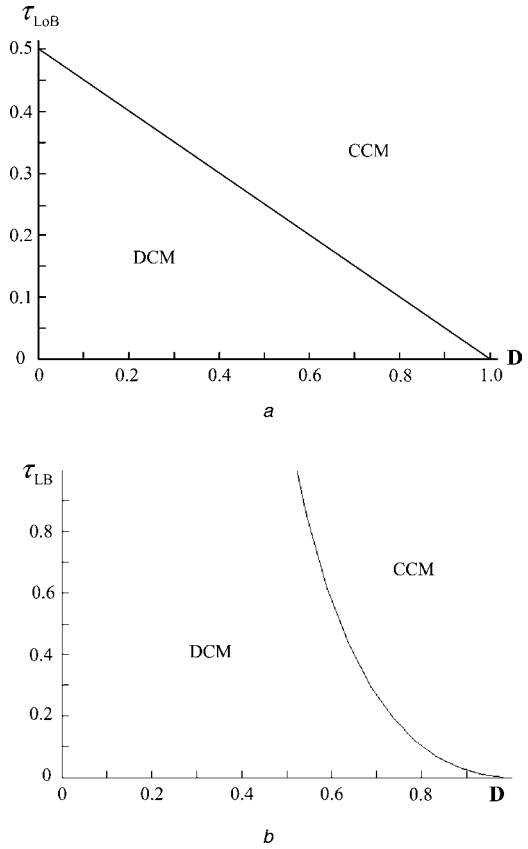

Fig. 5 *Boundary condition of the proposed converter*
a Rear stage
b Front stage (under $\tau_{Lo} = 0.3$)

4 Selection of inductors and a capacitor

4.1 Selection of inductors L_o, L_1 and L_2

To ensure that the front and rear stages are both operated in DCM, the appropriate τ_{LoB} and τ_{LB} can be selected under the required voltage gain. Thus, the L_o and L must satisfy the following inequality.

$$\begin{cases} L_o < \dfrac{R}{f_s}\tau_{LoB} \\ L < \dfrac{R}{f_s}\tau_{LB} \end{cases} \tag{25}$$

4.2 Selection of DC-link capacitor C_1

From (11), the average capacitor current $i_{c1,k}$ per switching period can be rewritten as

$$\begin{aligned} i_{c1,k} &= \left[\frac{D^2V_m^2}{4Lf_sV_{c1}} - \frac{D^2(V_{c1}-V_o)}{2L_of_s}\right] \\ &\quad - \frac{D^2V_m^2}{4Lf_sV_{c1}}\cos 2\omega t_k \\ &= \frac{D^2}{2f_s}\left(\frac{V_m^2}{2LV_{c1}} - \frac{V_{c1}-V_o}{L_o}\right) \\ &\quad - \frac{D^2V_m^2}{4Lf_sV_{c1}}\cos 2\omega t_k \end{aligned} \tag{26}$$

Substituting (16) into (26), the ripple of DC-link voltage per switching period is obtained as

$$\Delta V_{c1,k} = \left(-\frac{D^2V_m^2}{4LC_1f_sV_{c1}}\cos 2\omega t_k\right)T_s \tag{27}$$

Hence, the function of the ripple of DC-link voltage per half AC source period can be computed as

$$\begin{aligned} \Delta V_{c1}(t) &= \int_0^t \left(-\frac{D^2V_m^2}{4LC_1f_sV_{c1}}\cos 2\omega t\right)dt \\ &= -\frac{D^2V_m^2}{4LC_1f_sV_{c1}}\frac{\sin 2\omega t}{2\omega} \end{aligned} \tag{28}$$

From this equation, the ripple of DC-link voltage per half AC source period is derived as

$$\begin{aligned} V_{c1,ripple} &= 2|\Delta V_{c1}(t)|_{peak} = \frac{D^2V_m^2}{4\omega LC_1f_sV_{c1}} \\ \frac{V_{c1,ripple}}{V_{c1}} &= \frac{D^2V_m^2}{4\omega LC_1f_sV_{c1}^2} = \frac{D^2}{4\omega LC_1f_sM_1^2} \end{aligned} \tag{29}$$

Therefore to satisfy the specification of the ripple percentage of DC-link voltage, the capacitor C_1 needs to satisfy the following inequality.

$$C_1 \geq \frac{D^2}{4\omega Lf_sM_1^2}\frac{V_{c1}}{V_{c1,ripple}} \tag{30}$$

5 Experimental results

To verify the theoretical analysis of the proposed converter, a hardware circuit with simple control logic is implemented

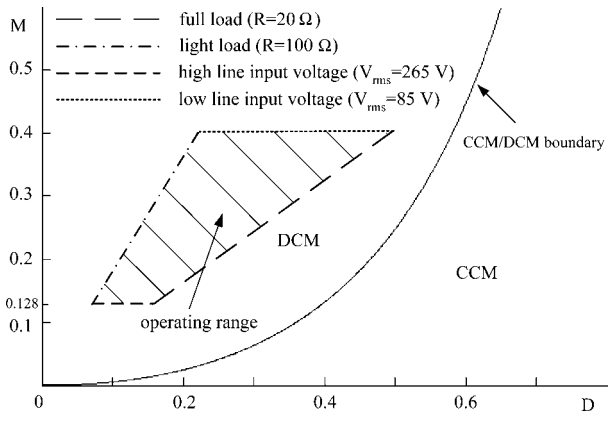

Fig. 6 *Operating range of the experimental prototype*

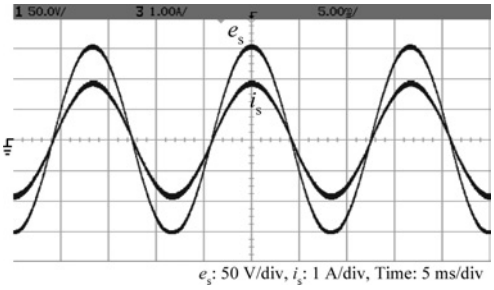

Fig. 7 *Waveforms of input voltage and input current*

in the laboratory. The circuit parameters are chosen as follows

(i) Output voltage: $V_o = 48$ V
(ii) Universal input voltage: $V_{rms} = 85$–265 V ($V_m = 120$–375 V)
(iii) Load: $P_o = 23.04$–115.2 W ($R = 20$–$100\ \Omega$)
(iv) Line frequency: $f_l = 60$ Hz
(v) Switching frequency: $f_s = 24$ kHz
(vi) Input filter: $L_f = 6$ mH, $C_f = 320$ nF.

To ensure that the output voltage is kept constant for the universal input voltage, the voltage gain M is varied from 0.128 to 0.4. Substituting $M = 0.4$ into (21), the

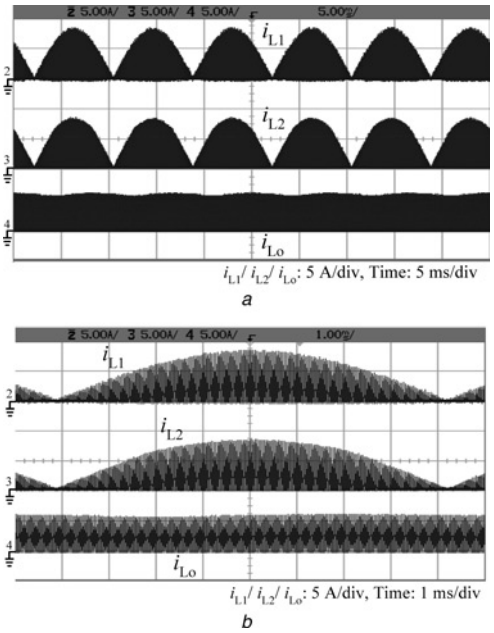

Fig. 8 *Waveforms of inductor currents*

a i_{L1}, i_{L2} and i_{Lo}
b Expansion of i_{L1}, i_{L2} and i_{Lo}

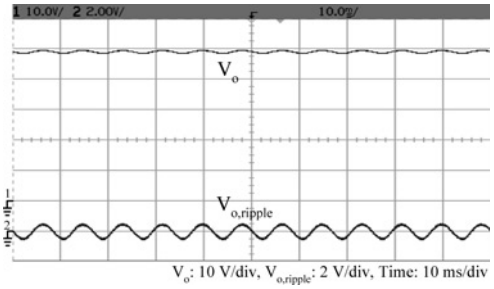

Fig. 9 *Waveforms of output voltage and its ripple*

maximum duty ratio D_{max} can be found to be 0.58. Substituting $D_{max} = 0.58$ into (23), τ_{LoB} is obtained as 0.21. Then, substituting $D_{max} = 0.58$ and $\tau_{Lo} = 0.21$ into (24), τ_{LB} is computed as 0.52. Using (25), the following inequality of inductors can be derived.

$$L_o < \frac{R}{f_s}\tau_{LoB} = \frac{20}{24k} \cdot 0.21 = 175\ \mu H$$

$$L < \frac{R}{f_s}\tau_{LB} = \frac{20}{24k} \cdot 0.52 = 433\ \mu H$$

As $L_1 = L_2 = L/2$, L_1 and L_2 are selected as 155 μH, and L_o is chosen as 155 μH.

Thus, τ_{Lo} and τ_L are 0.186 and 0.372 under full load condition $R = 20\ \Omega$, τ_{Lo} and τ_L are 0.037 and 0.074 under light load condition $R = 100\ \Omega$. Substituting τ_{Lo} and τ_L into (18), the operating range of the experimental prototype is shown in Fig. 6. It illustrates that the proposed converter is operated in DCM.

Under the conditions $V_{rms} = 85$ V and $R = 20\ \Omega$, the M and D can be found to be 0.4 and 0.49 from (18). Substituting $\tau_{Lo} = 0.186$, $\tau_L = 0.372$ and $D = 0.49$ into (19), M_2 and M_1 can be computed as 0.54 and 0.74, respectively. Also, the ripple percentage of V_{c1} is selected to be 6%. Thus, the following inequality of C_1 can be obtained from (30).

$$C_1 \geq \frac{D^2}{4\omega L f_s M_1^2}\frac{V_{c1}}{V_{c1,ripple}} = 656\ \mu F$$

C_1 is selected as 660 μF, and C_o is chosen as 330 μF.

Under the conditions $V_{rms} = 110$ V, $V_o = 48$ V and $P_o = 115.2$ W, some experimental results are shown in Figs. 7–9. From Fig. 7, one can see that the input current is purely sinusoidal and is in phase with the input voltage. The inductor currents i_{L1}, i_{L2} and i_{Lo} and the expansion of i_{L1}, i_{L2} and i_{Lo} are shown in Figs. 8*a* and *b*; it is obvious that the two power stages are both operated in DCM. Fig. 9 shows the DC output voltage and its ripple component, the output voltage is controlled at 48 V and its ripple component is rather small. In addition, the measured power factor, THD_i, efficiency and DC-link voltage V_{c1} under the operating range of the specified design are shown in Fig. 10. From Fig. 10*a*, when the output power is above 57.6 W, the measured power factor is above 0.99. Even in the light load, the power factor is still above 0.951. The measured THD_i is less than 4% as shown in Fig. 10*b*. Fig. 10*c* shows the measured efficiency; one can see that the efficiency is 81.7–83.1% under $P_o = 115.2$ W for universal input voltage. It is seen from Fig. 10*d* that the measured V_{c1} varies with the input voltage, and the maximum of V_{c1} is equal to 209 V at the condition $V_{rms} = 265$ V.

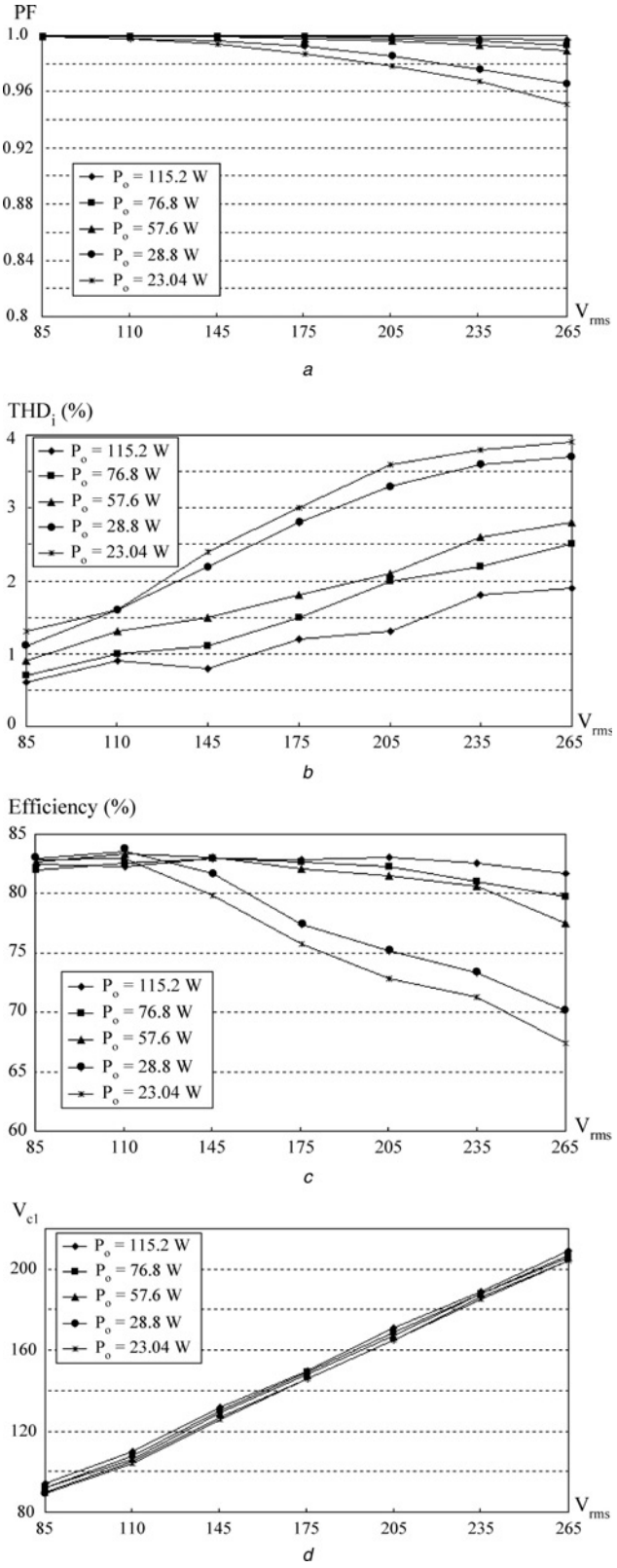

Fig. 10 *Some measured results against universal input voltage for various output power*

a Power factor
b Total harmonic distortion of input current
c Efficiency
d V_{c1}

6 Conclusions

In this paper, a single-phase AC/DC converter by cascading a buck-boost converter with a buck converter is proposed. The proposed converter has many merits, such as unity power factor, low THD_i, low DC-link voltage and adjustable output voltage. Also this converter can be used for universal input voltage and wide output power range. Moreover, the steady-state analyses of voltage gain and boundary operating condition are presented. The selections of inductors, capacitors and input filters are depicted. To illustrate the theoretical analysis, a hardware circuit with simple control logic is implemented. Under the operating range of the specified design, one can obtain good performances that the measured power factor is larger than 0.951, the measured THD_i is less than 4% and the maximum V_{c1} is equal to 209 V at the condition $V_{rms} = 265$ V.

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