External Memory Interface

MicropendousX-LPC182x-GPS-EMI.sch

USB

MicropendousX-LPC182x-GPS-USB.sch

System

MicropendousX-LPC182x-GPS-System.sch

Position_Sensors

MicropendousX-LPC182x-GPS-Position_Sensors.sch

RF

MicropendousX-LPC182x-GPS-RF.sch

LCD

MicropendousX-LPC182x-GPS-LCD.sch

Power Supply

MicropendousX-LPC182x-GPS-Power.sch

Vias

MicropendousX-LPC182x-GPS-Vias.sch

Notes:
 — Design targets Revision 'A' of the LPC182x
 — Pins with more than one function are labeled
   with their pin name and function(s) used
 — VDD controls LPC182x, RF Transceiver, LCD Touchscreen Controller,
   and Motion Sensor so that these can wake up the device
 — VDDIO powers microSD, GPS Module, and LCD Display
   along with all LPC182x IO pins so that these can be
   disabled in low-power modes.
 — Only WAKEUP pin can wake up device from Deep Sleep and Power-Down Modes
 — USB0 can wake up device only from Sleep Mode
 — Power Consumption: Normal 10mA+, Sleep 5.5mA+, Other <1mA

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Opendous Inc.
File: MicropendousX-LPC182x-GPS.sch
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Title: MicropendousX-LPC182x-GPS
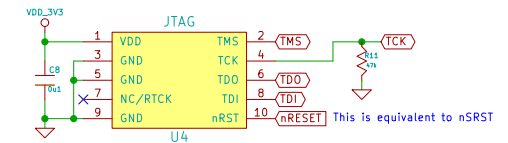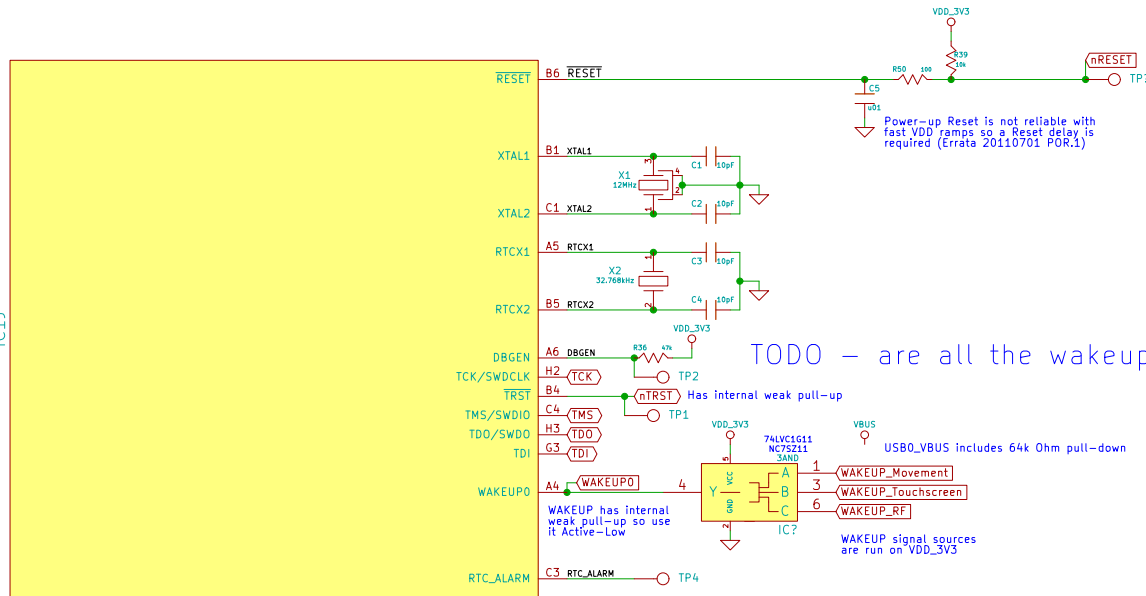Size: A4 | Date: 1 jun 2012 | Rev: 1.0
KiCad E.D.A. | Id: 1/9

Notes:
- Run core system on always-on VDD_3V3
- Rpu is min. 45k Ohm, so for boot selection pull-down resistor,
  19k is max. usable as 3.3(19/(19+45))=0.98V < Vil=(3.3*.3)=1V
- LTC3559 soft-start takes 500us but Vih(EN2)=1.2V means
  that VDD ramp will begin VDDIO ramp after about 200us.
  VDDIO should be >2.0V=Vih(GPIO) about 300us after
  VDD>1.2V or 500us after VDD ramp begins.
  Vih(RESET)=0.8*(3.3-0.35)=2.3V which means RESET
  will be deasserted about 350us after VDD ramp starts.
  LPC182x has a 250us wake up delay after RESET which means
  that it will check boot mode pins after about 350+250=600us
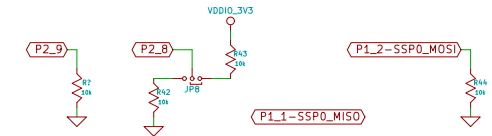 which is about 100us after VDDIO boot mode pull-ups are >Vih(GPIO)

JTAG

VDD_3V3

JTAG
1 VDD   TMS 2   TMS
3 GND   TCK 4   TCK
5 GND   TDO 6   TDO
7 NC/RTCK TDI 8   TDI
9 GND   nRST 10 nRESET   This is equivalent to nSRST
U4

TDO need not be pulled up since
TCK pull-down ensures no random
data is ever sent as TDO is only
valid when clock is valid.

C8
0u1

LPC182x
IC1J

B6 RESET

R50 100   C5 u01
R39
10k
VDD_3V3
nRESET
TP?

Power-up Reset is not reliable with
fast VDD ramps so a Reset delay is
required (Errata 20110701 POR.1)

XTAL1   B1 XTAL1
X1   C1 10pF
12MHz
XTAL2   C1 XTAL2
C2 10pF

RTCX1   A5 RTCX1
X2   C3 10pF
32.768kHz
RTCX2   B5 RTCX2
C4 10pF

DBGEN   A6 DBGEN   R36 47k   VDD_3V3
TCK/SWDCLK   H2 TCK   TP2
TRST   B4 nTRST   Has internal weak pull-up
TMS/SWDIO   C4 TMS   TP1
TDO/SWDO   H3 TDO
TDI   G3 TDI

WAKEUP0   A4 WAKEUP0   4
74LVC1G11
NC7SZ11
3AND
Y VCC
A 1   WAKEUP_Movement
B 3   WAKEUP_Touchscreen
C 6   WAKEUP_RF
GND
IC?
WAKEUP has internal
weak pull-up so use
it Active-Low
WAKEUP signal sources
are run on VDD_3V3

RTC_ALARM   C3 RTC_ALARM   TP4

VDD_3V3   VBUS
USB0_VBUS includes 64k Ohm pull-down

TODO — are all the wakeup signals Active-LOW

Boot Mode Selection

VDDIO_3V3

P2_9   P2_8   P1_2-SSP0_MOSI
R2   R43   R44
10k   10k   10k
R42   JP8   P1_1-SSP0_MISO
10k

Boot Mode	P2_9(A0)	P2_8(A8)	P1_1(A6)	P1_2(A7)
SPIFI	LOW	LOW	HIGH	LOW
USB0	LOW	HIGH	HIGH	LOW
USART0	LOW	LOW	LOW	LOW
EMC 8-Bit	LOW	LOW	LOW	HIGH
EMC 16-Bit	LOW	LOW	HIGH	HIGH
EMC 32-Bit	LOW	HIGH	LOW	LOW
USB1	LOW	HIGH	LOW	HIGH
SPI (SSP)	LOW	HIGH	HIGH	HIGH
USART3	HIGH	LOW	LOW	LOW

Note boot pins have weak internal pull-ups of about 50k Ohm to VDDIO

Taken from LPC18x0 Datasheet — Table 5

LPC182x
IC1K

P3_8/SSP0_MOSI/GPIO5[11]/SSP0_SSEL/SPIFI_CS   E7 P3_8-SPIFI_CS
P3_3/SSP0_SCK/CGU_OUT1/I2S0_TX_MCLK/I2S1_TX_SCK/SPIFI_SCK   A7 P3_3-SPIFI_SCK
P3_7/SSP0_MISO/GPIO5[10]/SSP0_MOSI/SPIFI_MOSI   D7 P3_7-SPIFI_MOSI
P3_6/GPIO0[6]/SSP0_SSEL/SSP0_MISO/SPIFI_MISO   C7 P3_6-SPIFI_MISO
P3_5/GPIO1[15]/U1_RXD/I2S0_TX_SDA/I2S1_RX_WS/LCD_VD12/SPIFI_SIO2   B7 P3_5-SPIFI_SIO2
P3_4/GPIO1[14]/U1_TXD/I2S0_TX_WS/I2S1_RX_SDA/LCD_VD13/SPIFI_SIO3   B8 P3_4-SPIFI_SIO3

VDD_3V3
C108
0u1

25Q
VDD_3V3
P3_8-SPIFI_CS   1 nCS   VCC 8
P3_6-SPIFI_MISO   2 DO/IO1 nHOLD/IO3 7   P3_4-SPIFI_SIO3
P3_5-SPIFI_SIO2   3 nWP/IO2 CLK 6   P3_3-SPIFI_SCK
   4 GND   DI/IO0 5   P3_7-SPIFI_MOSI
IC7
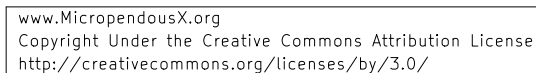DFN 6x5mm

Maximum 16MBit per
Errata R1.3 SPIFI.2

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KiCad E.D.A.   Id: 7/9

Notes:
 — Boot pins have weak internal pull—ups of about 50k Ohm to VDDIO
   so VDDIO_3V3 must be enabled at startup
 — HPWR and SUSP have 2M Ohm weak pull—downs
 — both regulators output 3.3V nominal but lowering the
   voltage to 3.0V will reduce power and be within
   all components' supply margins
 — use low ESL reverse geometry X?R caps closest to device
 — BAT54C reverse leakage is maximum 2uA. Take note of this
   if VBUS is used as a logic input since Ii for 74LVC is 5uA max.

VBAT must be < 3.6V

VDDA   VDDIO_3V3

VDD_3V3

TP5

C115
1u

VDDIO_3V3   VDDA   VDD_3V3   VDDIO_3V3

VDDIO_3V3

LPC182x
IC1M

USB0_VDDA_3V3_DRIVER
USB0_VDDA_3V3
VDDA
VDDREG
VDDREG
VDDREG
VDDIO
VDDIO

D1 D2   B2   E4 E5 F4   F10 K5

VBAT   C5

VDD_3V3

C24 C18 C17 C19 C50 C21
10u 1u0 4u7 0u1 33n 33n

USB0_RREF   F3   USB0_RREF

VDDA

C64
0u1

VSSA

VDDIO_3V3

C?? C27 C29 C34 C36 C37 C107 C22
1u0 10u 10u 10u 33n 1n0 u01   1u0

1%   R48   12k

USB0_VSSA_TERM
USB0_VSSA_REF

YSSA   VSS VSS VSS VSS VSS

C2   C8 D4 D5 G8 J3 J6

D3 F2

L1

VSSA

Power Management
Li—Ion Charger, Guage, and Dual Buck Regulators

+BATT

R4 1k

C9
1u0

C10
u22

STC3100

LTC3559_NTC

C11
4u7

TP6   IO0

IO0   VCC   VIN   SDA   3   P2_3—I2C1_SDA
      CG   GND—PAD   SCL 4   P2_4—I2C1_SCL

I2C1 from LCD Sheet

C26
2u2

R21
0R8

BAT1

GND

Li—Ion

1%
1206

R3
0R03

IC2

R6 200k
0.1%
0805

SUSP internal pull—down is too weak
to overcome LPC182x 45k+ pull—up
and requires external pull—down
3.3(5.1/(5.1+45))=0.34V < Vil=0.4V

VBUS

C13 C14
10u 0u1

1%   R13
     10k

LTC3559

VBUS

P1_3—GPIO0_10
From EMI Sheet

R2
4k1

R14 1k74
R14 = 1.74k limits USB
charge current to 500mA

VBUS

CHRG   R12 1k
D1

+BATT

NTC   BAT   2

VCC   PVin   7

PROG   SW1   6

CHRG   FB1   4

SUSP
HPWR   12

EN1   5
EN2   9
MODE   3

GND GND—PAD
IC6   17

L5 4u7uH

C30
22p
R16
36k
C54
10u
R17
36k

+BATT   R15 1k   LTC3559_HPWR

P6_5—GPIO3_4
From EMI Sheet

P6_4—GPIO3_3
From EMI Sheet

MODE HIGH
enables
lower power
Burst Mode

VBUS

R23
47k

+BATT

R9
47k

D2
BAT54C

If either VBUS or battery
are present, main VDD
power supply will be enabled.

VDD_3V3

R22
47k

In deep sleep mode
VDDIO can be
disabled.

R23

VDD_3V3   VDDIO_3V3

DNI   L2

For Testing

VDD_3V3

SW2   8   L6 4u7uH

FB2   10

C32
22p
R18
36k
C55
10u
R19
36k

VDDIO_3V3

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File: MicropendousX-LPC182x-GPS-Power.sch
Sheet: /Power Supply/

Title: MicropendousX—LPC182x—GPS

Size: A4   Date: 1 jun 2012   Rev: 1.0

KiCad E.D.A.   Id: 8/9

LTC3559_VCC   LTC3559_VCC
LTC3559_CHRG   LTC3559_CHRG

Notes:

LPC182x
IC1A

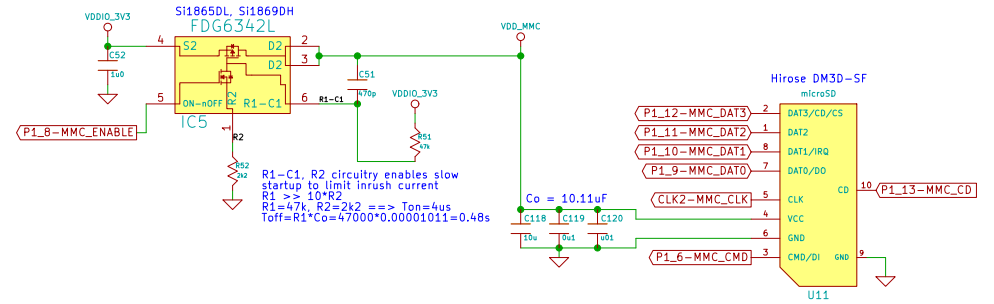| Pin	Signal	
B10	P2_9/GPIO1[10]/CTOUT_3/U3_BAUD/EMC_A0	P2_9 Used in System Sheet
E8	P2_10/GPIO0[14]/CTOUT_2/U2_TXD/EMC_A1	P2_10-GPIO0_14 Used in RF Sheet
A9	P2_11/GPIO1[11]/CTOUT_5/U2_RXD/EMC_A2	
B9	P2_12/GPIO1[12]/CTOUT_4/U2_UCLK/EMC_A3	P2_12-GPIO1_12 Used in RF Sheet
A10	P2_13/GPIO1[13]/CTIN_4/U2_DIR/EMC_A4	P2_13-GPIO1_13 Used in RF Sheet
H1	P1_0/GPIO0[4]/CTIN_3/SSP0_SSEL/EMC_A5	P1_0-SSP0_SSEL Used in RF Sheet
K2	P1_1/GPIO0[8]/CTOUT_7/SSP0_MISO/EMC_A6	P1_1-SSP0_MISO Used in RF and System Sheets
K1	P1_2/GPIO0[9]/CTOUT_6/SSP0_MOSI/EMC_A7	P1_2-SSP0_MOSI Used in RF and System Sheets
C6	P2_8/CTOUT_0/U3_DIR/GPIO5[7]/EMC_A8	P2_8 Used in System Sheet
C10	P2_7/GPIO0[7]/CTOUT_1/U3_UCLK/T3_MAT3/EMC_A9	TP3 P2_7 has weak internal pull-up to disable ISP
G9	P2_6/U0_DIR/USB0_IND0/GPIO5[6]/CTIN_7/T3_CAP3/EMC_A10	P2_6-GPIO5_6 Used in Position Sensors Sheet
F5	P2_2/U0_UCLK/USB0_IND1/GPIO5[2]/CTOUT_6/T3_CAP2/EMC_A11	
G7	P2_1/U0_RXD/USB0_PWR_FAULT/GPIO5[1]/T3_CAP1/EMC_A12	P2_1-U0_RXD Used in Position Sensors Sheet
G10	P2_0/U0_TXD/USB0_PWR_EN/GPIO5[0]/T3_CAP0/ENET_MDC/EMC_A13	P2_0-U0_TXD Used in Position Sensors Sheet
G4	P1_7/GPIO1[0]/U1_DSR/CTOUT_13/USB0_PWR_EN/EMC_D0	
H5	P1_8/GPIO1[1]/U1_DTR/CTOUT_12/MMC_VOLT0/EMC_D1	P1_8-MMC_ENABLE
J5	P1_9/GPIO1[2]/U1_RTS/CTOUT_11/MMC_DAT0/EMC_D2	P1_9-MMC_DAT0
H6	P1_10/GPIO1[3]/U1_RI/CTOUT_14/MMC_DAT1/EMC_D3	P1_10-MMC_DAT1
J7	P1_11/GPIO1[4]/U1_CTS/CTOUT_15/MMC_DAT2/EMC_D4	P1_11-MMC_DAT2
K7	P1_12/GPIO1[5]/U1_DCD/T0_CAP1/MMC_DAT3/EMC_D5	P1_12-MMC_DAT3
H8	P1_13/GPIO1[6]/U1_TXD/T0_CAP0/MMC_CD/EMC_D6	P1_13-MMC_CD
J8	P1_14/GPIO1[7]/U1_RXD/T0_MAT2/EMC_D7	
K4	P1_6/GPIO1[9]/CTIN_5/MMC_CMD/EMC_WE	P1_6-MMC_CMD
J1	P1_3/GPIO0[10]/CTOUT_8/USB0_IND1/SSP1_MISO/MMC_RST/EMC_OE	P1_3-GPIO0_10 Used in Power Supply Sheet
J4	P1_5/GPIO0[8]/CTOUT_10/USB0_PWR_FAULT/SSP1_SSEL/MMC_POW/EMC_CS0	P1_5-GPIO0_8 Used in Position Sensors Sheet
J2	P1_4/GPIO0[11]/CTOUT_9/USB0_IND0/SSP1_MOSI/MMC_VOLT1/EMC_BLS0	P1_4-GPIO0_11 Used in Position Sensors Sheet
F6	P6_4/GPIO3[3]/CTIN_6/U0_TXD/EMC_CAS	P6_4-GPIO3_3 Used in Power Supply Sheet
F9	P6_5/GPIO3[4]/CTOUT_6/U0_RXD/EMC_RAS	P6_5-GPIO3_4 Used in Power Supply Sheet
K3	CLK0/EMC_CLK0/CLKOUT/MMC_CLK/EMC_CLK01/ENET_TX_CLK/ENET_REF_CLK/SSP1_SCK	
K6	CLK2/CLKOUT/MMC_CLK/I2S1_RX_SCK/I2S0_TX_MCLK/EMC_CLK23/EMC_CLK3	CLK2-MMC_CLK

LPC182x
IC1E

Pin	Signal	
H4	PF_4/SSP1_SCK/GP_CLKIN/TRACECLK/I2S0_RX_SCK/LCD_CLKIN/I2S0_TX_MCLK	
A8	P3_0/I2S0_RX_MCLK/I2S0_TX_MCLK/SSP0_SCK/I2S0_RX_SCK/I2S0_TX_SCK	P3_0-SSP0_SCK Used in RF Sheet
G6	P3_2/CAN0_TD/USB1_IND0/GPIO5[9]/LCD_VD14/I2S0_RX_SDA/I2S0_TX_SDA	
F7	P3_1/CAN0_RD/USB1_IND1/GPIO5[8]/LCD_VD15/I2S0_RX_WS/I2S0_TX_WS	P3_1-GPIO5_8 Used in Position Sensors Sheet
H7	xP6_0/I2S0_RX_MCLK/I2S0_RX_SCK	
J9	xP6_2/GPIO3[1]/EMC_CKEOUT1/U0_DIR/T2_CAP1/I2S0_RX_SDA	
G5	xP6_1/GPIO3[0]/EMC_DYCS1/U0_UCLK/T2_CAP0/I2S0_RX_WS	

VDDIO_3V3

Si1865DL, Si1869DH
FDG6342L
IC5

VDD_MMC

C52
1u0

S2   D2
          D2
ON-nOFF   R1-C1
R2

C51
47p

VDDIO_3V3
R51
47k
R52
2k2

P1_8-MMC_ENABLE

R1-C1, R2 circuitry enables slow
startup to limit inrush current
R1 >> 10*R2
R1=47k, R2=2k2 ==> Ton=4us
Toff=R1*Co=47000*0.00001011=0.48s

Co = 10.11uF
C118   C119   C120
10u   0u1   u01

Hirose DM3D-SF
microSD
U11

Pin	Signal	
2	DAT3/CD/CS	P1_12-MMC_DAT3
1	DAT2	P1_11-MMC_DAT2
8	DAT1/IRQ	P1_10-MMC_DAT1
7	DAT0/D0	P1_9-MMC_DAT0
10	CD	P1_13-MMC_CD
5	CLK	CLK2-MMC_CLK
4	VCC	
6	GND	
3	CMD/DI	P1_6-MMC_CMD
9	GND	

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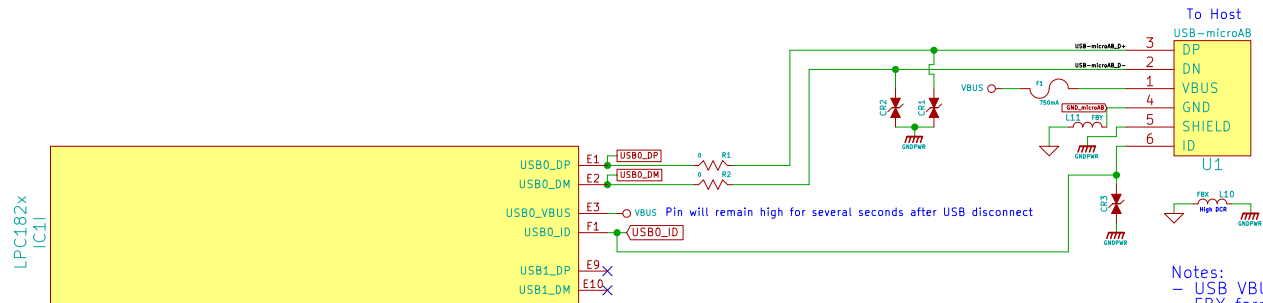Sheet: /External Memory Interface/
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LPC182x
IC11

USB0_DP   E1   USB0_DP
USB0_DM   E2   USB0_DM
USB0_VBUS E3   VBUS Pin will remain high for several seconds after USB disconnect
USB0_ID   F1   USB0_ID
USB1_DP   E9
USB1_DM   E10

0   R1
0   R2

To Host
USB-microAB
USB-microAB_D+   3   DP
USB-microAB_D-   2   DN
VBUS   F1   1   VBUS
750mA   4   GND
GND_microAB   5   SHIELD
L11   FBY   6   ID
U1

CR2   CR1
GNDPWR
GNDPWR

CR3
GNDPWR

FBX   L10
High DCR
GNDPWR

Notes:
– USB VBUS Fuse F1 limits inrush current
– FBX ferrite bead is high DCR 0805
– FBY ferrite beads are high current 0805
– all other FB are 1A 0603, moderate DCR

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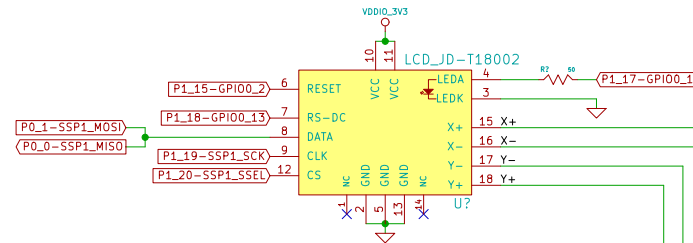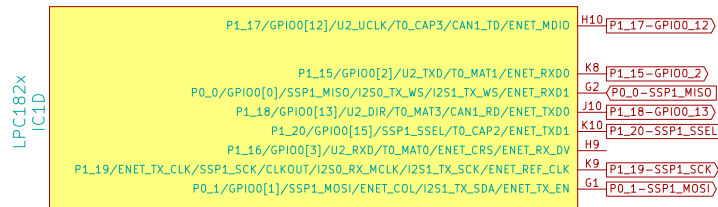KiCad E.D.A.   Id: 6/9
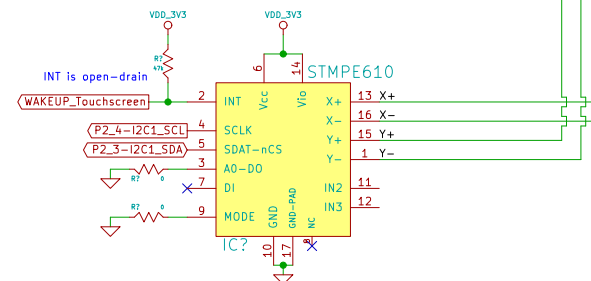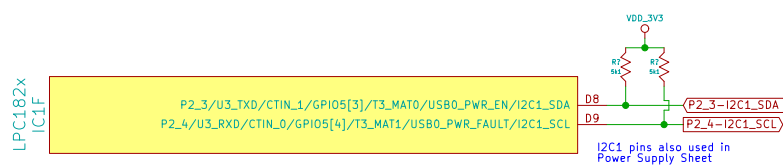
LCD and Resistive Touchscreen

Notes
- Enable the Touchscreen controller to wake up the processor
- Run STMPE610 on always-on VDD to enable Touchscreen wakeup
- Run LCD on VDDIO since it does not need to always be on
- GPIO0_12 is a High Drive Strength Pin that can source 32mA to the LCD Backlight LED

LPC182x
IC1D

P1_17/GPIO0[12]/U2_UCLK/T0_CAP3/CAN1_TD/ENET_MDIO   H10 P1_17-GPIO0_12

P1_15/GPIO0[2]/U2_TXD/T0_MAT1/ENET_RXD0   K8 P1_15-GPIO0_2
P0_0/GPIO0[0]/SSP1_MISO/I2S0_TX_WS/I2S1_TX_WS/ENET_RXD1   G2 P0_0-SSP1_MISO
P1_18/GPIO0[13]/U2_DIR/T0_MAT3/CAN1_RD/ENET_TXD0   J10 P1_18-GPIO0_13
P1_20/GPIO0[15]/SSP1_SSEL/T0_CAP2/ENET_TXD1   K10 P1_20-SSP1_SSEL
P1_16/GPIO0[3]/U2_RXD/T0_MAT0/ENET_CRS/ENET_RX_DV   H9
P1_19/ENET_TX_CLK/SSP1_SCK/CLKOUT/I2S0_RX_MCLK/I2S1_TX_SCK/ENET_REF_CLK   K9 P1_19-SSP1_SCK
P0_1/GPIO0[1]/SSP1_MOSI/ENET_COL/I2S1_TX_SDA/ENET_TX_EN   G1 P0_1-SSP1_MOSI

VDDIO_3V3

LCD_JD-T18002

P1_15-GPIO0_2   6 RESET   VCC VCC   LEDA   4 R? 50 P1_17-GPIO0_12
                                          LEDK   3
P1_18-GPIO0_13   7 RS-DC
P0_1-SSP1_MOSI   8 DATA   X+   15 X+
P0_0-SSP1_MISO   X-   16 X-
P1_19-SSP1_SCK   9 CLK   Y-   17 Y-
P1_20-SSP1_SSEL   12 CS   NC GND GND GND NC   Y+   18 Y+

U?

Resistive Touchscreen Controller

LPC182x
IC1F

P2_3/U3_TXD/CTIN_1/GPIO5[3]/T3_MAT0/USB0_PWR_EN/I2C1_SDA   D8 P2_3-I2C1_SDA
P2_4/U3_RXD/CTIN_0/GPIO5[4]/T3_MAT1/USB0_PWR_FAULT/I2C1_SCL   D9 P2_4-I2C1_SCL

VDD_3V3
R? R?
5k1 5k1

I2C1 pins also used in
Power Supply Sheet

VDD_3V3   VDD_3V3

INT is open-drain   R?
47k

STMPE610

WAKEUP_Touchscreen   2 INT   Vcc Vio   X+   13 X+
                                              X-   16 X-
P2_4-I2C1_SCL   5 SCLK   Y+   15 Y+
P2_3-I2C1_SDA   4 SDAT-nCS   Y-   1 Y-
                  3 A0-D0
                  7 DI   R? 0   IN2   11
                  9 MODE R? 0   IN3   12
                      GND GND-PAD NC
IC?   10   17

Notes:
 - Target 315MHz RF Band (Short Data Packets, No Streaming, Limited Power) for Sensor Nodes
 - Use to transfer Identification and Control signals between nodes
 - Refer to Linx Application Note AN-00125 for FCC15.231 A-D Overview
 - CC1125 DS 1.12: 315/40=7.9, 40*8=320, (320-315)=5>1MHz TX, similar for XOSC/2 for RX
 - Use always-on VDD for power to enable Wake-On-Radio function
 - MISO and MOSI are used in System sheet to define boot order
 - MISO (P1_1) has a 50k pull-up
 - MOSI (P1_2) has a 10k pull-down
 - All capacitors should be X7R or C0G/NPO
 - For CC1120, use a 32MHz X3

CAUTION: Current RF filter inductor
and capacitor values are for 420MHz

VDD_3V3   VDD_RF
FB   L4

VDD_RF

C?   C?   C?   C?   C?   C?   C?   C?   C?   C?
1u0   47n   47n   47n   47n   47n   47n   47n   47n   47n

VDD_RF

CC112X

C? 5p1

27n
L?

56n
L?

C?

L?
5p1

27n   L?

15n
L?

C?

315MHz
A?

C? DNI

C?
6p2

C? 39p   15n L?

C?
2p2

5p1

43n L?

22n L?

C?

30 XOSC_Q1   LNA_N 20
31 XOSC_Q2   LNA_P 19
32 EXT_OSC   TRX_SW 18
2   nRESET   PA   17
11 nCS   LPF0   23
8   SCLK   LPF1   24
7   SI   RBIAS 14
9   SO-GPIO1   DCPL   6
10 GPIO0   DCPL_VCO   21
4   GPIO2   DCPL_PFD_CHP 26
3   GPIO3   DCPL_XOSC   29

VDD_GUARD DVDD DVDD AVDD_IF AVDD_RF AVDD_SYNTH1 AVDD_PFD_CHP AVDD_SYNTH2 AVDD_XOSC
1 5 12 13 15 22 25 27 28

NC GND
46 33

IC9

C28 15p
X3 40MHz
C31 15p

VDD_3V3
R24
47n

From EMI Sheet P2_13-GPIO1_13
C?
47n

No OSC, using Crystal X3
R25 0

From EMI Sheet P1_0-SSP0_SSEL
From EMI Sheet P3_0-SSP0_SCK
From EMI Sheet, also used in System Sheet P1_2-SSP0_MOSI
From EMI Sheet, also used in System Sheet P1_1-SSP0_MISO
To System Sheet WAKEUP_RF
From EMI Sheet (U2_UCLK) P2_12-GPIO1_12
From EMI Sheet (U2_TXD) P2_10-GPIO0_14

C?
1n8

R?
56k

VDD_RF
C?
56p
R?
k8

56n
L?

VDD_RF
C?
u01
C?
100p

C?
u22

C?
u01

C?
47n

C?
47n

Opendous Inc.
File: MicropendousX-LPC182x-GPS-RF.sch
Sheet: /RF/
Title: MicropendousX-LPC182x-GPS
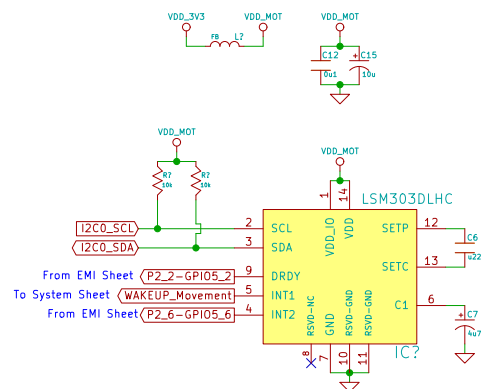Size: A4   Date: 1 jun 2012   Rev: 1.0
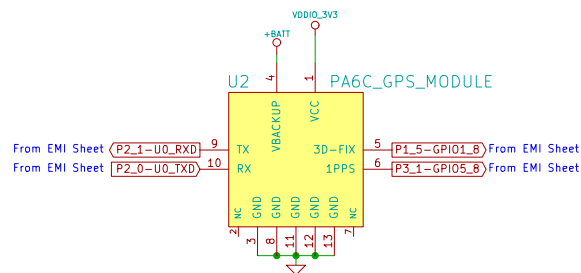KiCad E.D.A.   Id: 4/9

Notes:
- separate the LSM303 from all other electronics
- do not place a GND plane underneath the LSM303
- keep inductors and ferrites very far from the LSM303
- avoid ferrous materials like nickel near the LSM303
- X?R ceramic capacitor materials are ferrous, use C0G/NP0 or tantalum
- set LSM303 INT1 interrupt to Active-Low wakeup the LPC182x
- LSM303 is powered by always-on VDD_3V3 to
  enable the LSM303 to wake up the LPC182x when in motion
- PA6C is powered by VDDIO_3V3 so that it can be turned
  off when the device is not in motion
- PA6C VBACKUP is 2V to 4.3V so direct Li-Ion power is OK
- The 1PPS signal is connected to an interruptable GPIO
  pin so that it can be used as a global timebase for RF

Motion and Orientation Sensor

LSM303DLHC

IC?

GPS

U2   PA6C_GPS_MODULE

LPC182x
IC1G

Opendous Inc.

File: MicropendousX-LPC182x-GPS-Position_Sensors.sch
Sheet: /Position_Sensors/
Title: MicropendousX-LPC182x-GPS
Size: A4 | Date: 1 jun 2012 | Rev: 1.0
KiCad E.D.A. | Id: 2/9