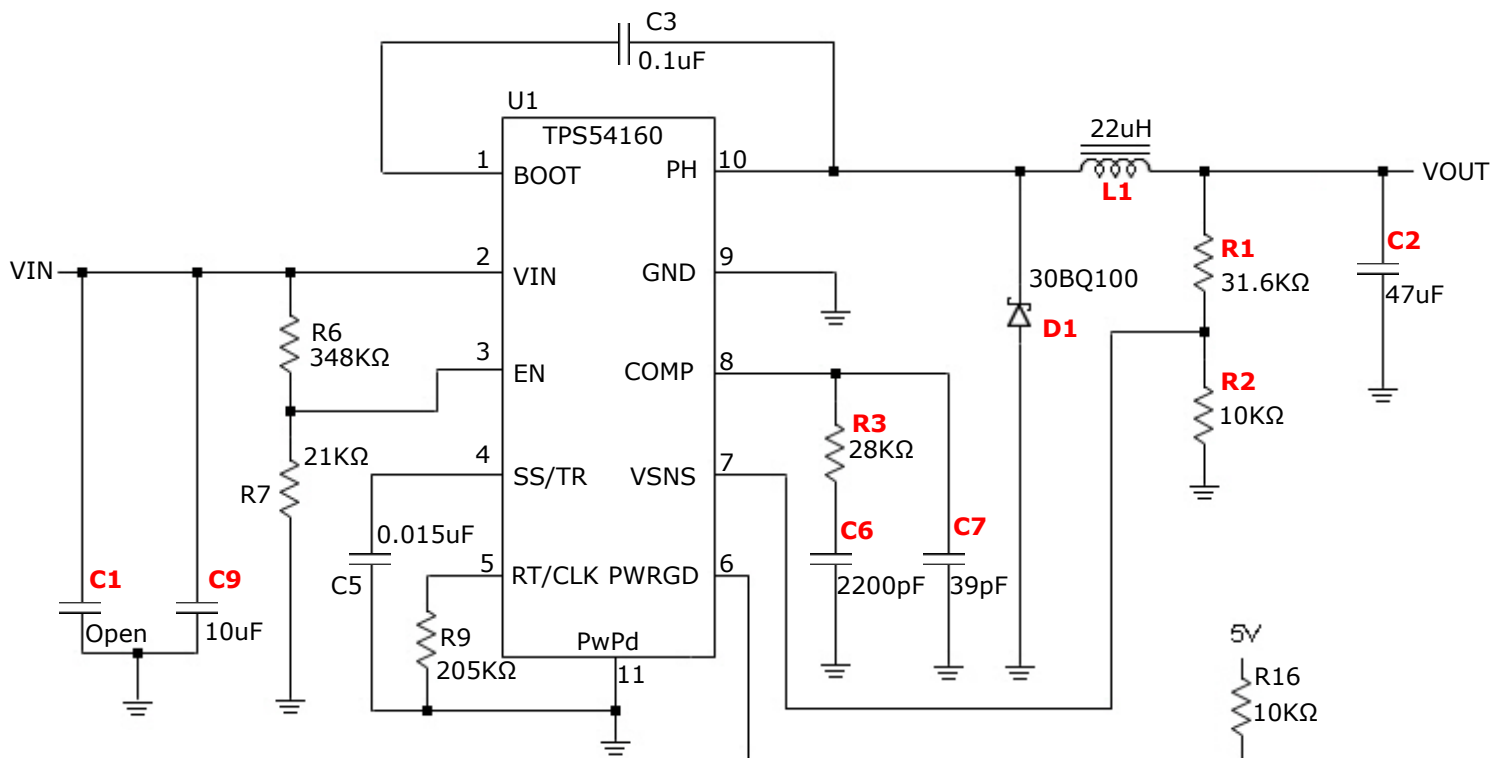


SwitcherPro Design Report Schematic

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A



i Calculated On-Time 92.4ns is below the 'Minimum Controllable On-Time' of the device (130ns) in the datasheet. Use the 'output' tab in the analysis section to view On-Time calculations. Calculated on-time below the minimum on-time may result in pulse skipping. This may or may not be acceptable in your application. For a BUCK converter, minimum on-time can be increased by reducing the maximum input voltage or the switching frequency.

SwitcherPro Design Report

Analysis - Main

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Input Voltage Volts - V	24.00	-	60.00	-	-	-	-	-	-
Input Ripple mVp-p - mVp-p	-	-	-	-	-	1200	-	-	34.0
UVLO(Start) Volts - V	-	-	-	-	-	-	-	21.65	-
UVLO(Stop) Volts - V	-	-	-	-	-	-	-	20.64	-
Switching Frequency KHz - KHz	-	-	-	-	570	-	-	-	-
Slow Start ms - ms	-	-	-	-	6.00	-	-	-	-
Estimated PCB Area mm ² - mm ²	-	-	-	-	-	-	-	750	-
Max Component Height mm - mm	-	-	-	-	-	25	-	-	20

SwitcherPro Design Report

Analysis - Output1

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Output Voltage Volts - V	-	3.300	-	-	-	-	3.212	-	3.447
Output Ripple mVp-p - mVp-p	-	-	-	-	-	66	-	-	3.1
Output Current Amps - A	-	-	1.000	0.100	-	-	-	-	-
Inductor Peak to Peak Current Amps - A	-	-	-	-	-	-	0.331	-	0.373
Current Limit Threshold Amps - A	-	-	-	-	2.700	-	-	-	-
Gain Margin dB - dB	-	-	-	-10	-	-	-	-19	-
Phase Margin Deg. - Deg.	-	-	-	60	-	-	-	63	-
Upper FET RDSon mOhms - mΩ	-	-	-	-	-	-	207	-	218
Duty Cycle % - %	-	-	-	-	-	-	6.5	-	16.0
On Time Min (switch) ns - ns	-	-	-	-	-	-	92.4	-	362.6
Cross Over Frequency KHz - KHz	-	-	-	-	-	-	-	17	-

SwitcherPro Design Report

Stress Results

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A

Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C9 (High Freq. Input Cap)	250V	60.3V	4A	0.37A	-	408uW	-
C2 (Bulk Output Cap)	6.3V	3.32V	3A	0.11A	-	12uW	-
L1 (Output Inductor)	-	-	1.5A	1.01A	-	81mW	-
D1 (Catch Diode)	100V	60.3V	3A	0.94A	-	538mW	50°C
U1 (Converter)	65V	60.3V	4A	0.4A	-	1.6W	115°C

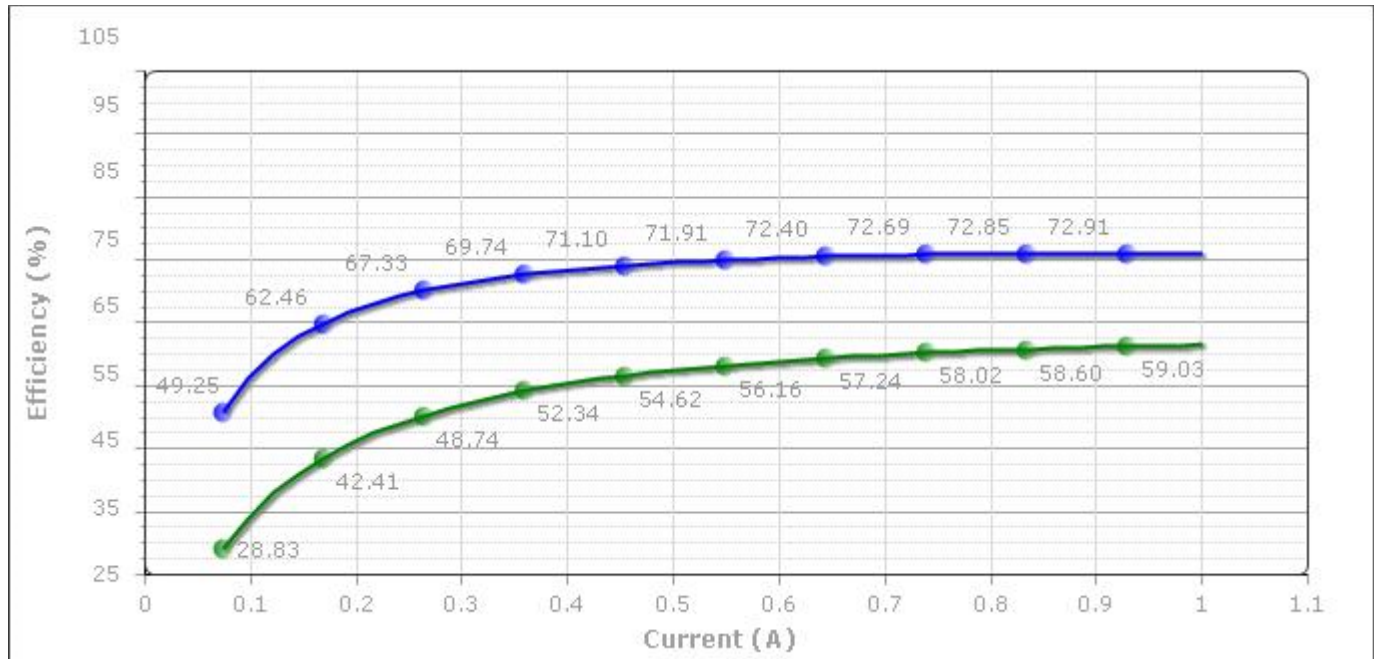
SwitcherPro Design Report

Efficiency

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A



— Efficiency For Vin Max
— Efficiency For Vin Min

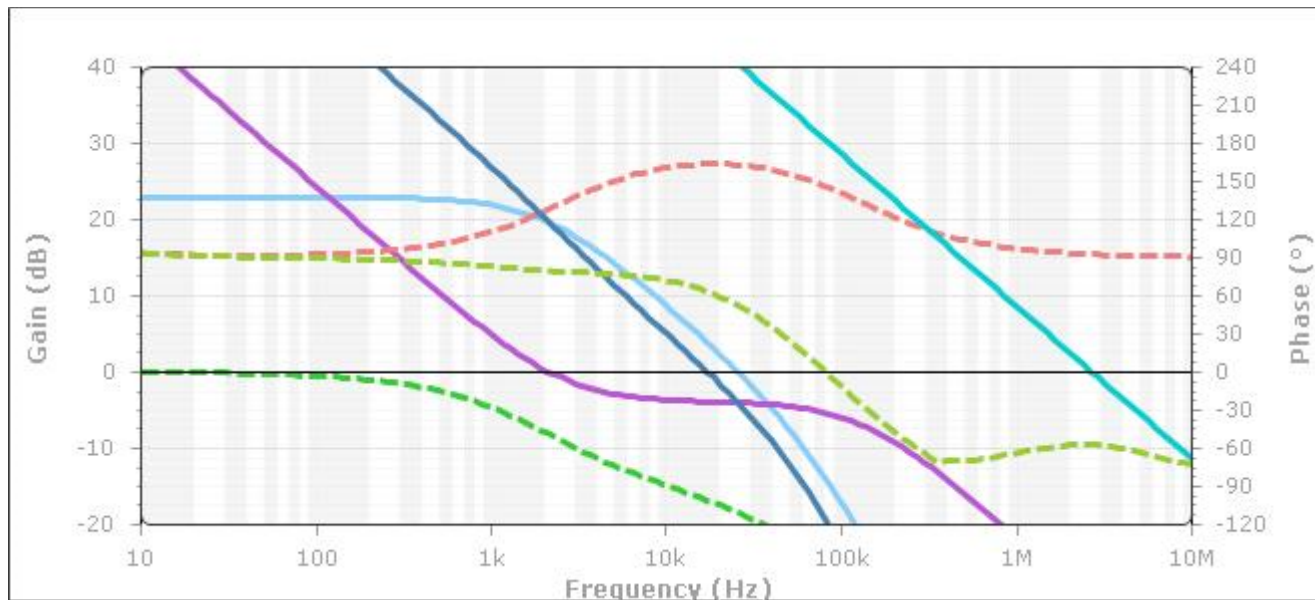
SwitcherPro Design Report

Loop Response

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A



— Power Stage Gain
— Power Stage Phase
— Compensation Gain
— Compensation Phase
— Error Amp Gain
— Total Gain
— Total Phase

SwitcherPro Design Report

Bill of Materials

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A

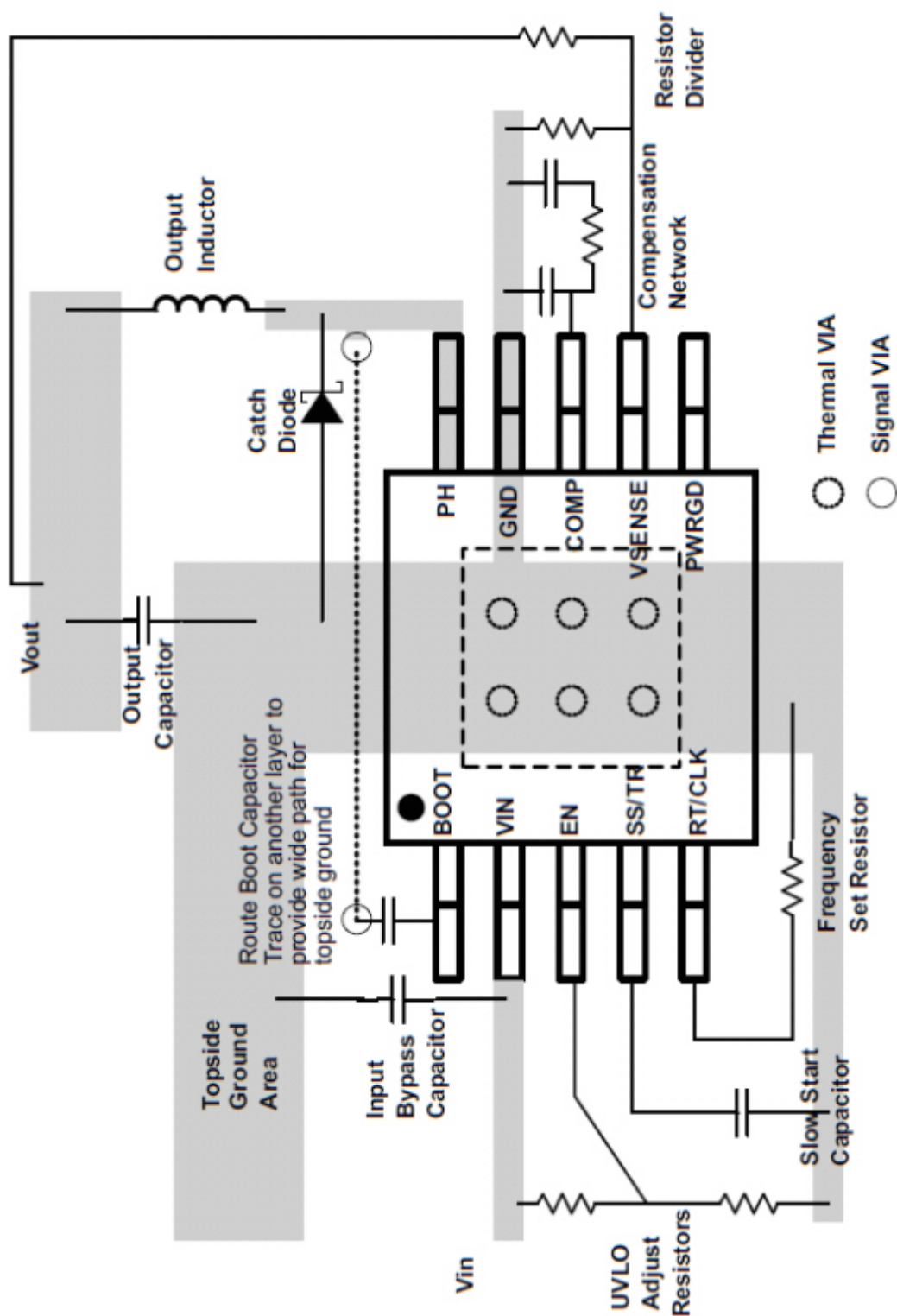
Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm ²)	Height(mm)
C2	1	GRM31CR60J476ME19L	Capacitor, Ceramic, 47uF, 6.3V, 20%	Murata Manufacturing	GRM31C 1206	7	1
C3	1	Standard	Capacitor, Ceramic, 0.1uF, 20V, 10%	Standard	0603	2	1
C5	1	Standard	Capacitor, Ceramic, 0.015uF, 10V, 20%	Standard	0603	2	1
C6	1	Standard	Capacitor, Ceramic, 2200pF, 10V, 20%	Standard	0603	2	1
C7	1	Standard	Capacitor, Ceramic, 39pF, 10V, 20%	Standard	0603	2	1
C9	1	KHD251E106M99C0B00	Capacitor, Electrolytic, 10uF, 250V, 20%	NIPPON CHEMI-CON	Radial	213	20
D1	1	30BQ100	Diode, Schottky, 100V, 3A	International Rectifier	SMC	42	2
L1	1	NPIS104T220MTRF	Inductor, 22uH, 1.5A, 80mΩ	NIC Components	Shielded	100	4
R1	1	Standard	Resistor, SurfaceMount, 31.6KΩ, 100mW, 1%	Standard	0603	2	1
R16	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
R2	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
R3	1	Standard	Resistor, SurfaceMount, 28KΩ, 100mW, 1%	Standard	0603	2	1
R6	1	Standard	Resistor, SurfaceMount, 348KΩ, 100mW, 1%	Standard	0603	2	1
R7	1	Standard	Resistor, SurfaceMount, 21KΩ, 100mW, 1%	Standard	0603	2	1
R9	1	Standard	Resistor, SurfaceMount, 205KΩ, 100mW, 1%	Standard	0603	2	1
U1	1	TPS54160	IC, Converter, 10 pins	Texas Instruments, Inc.	MSOP-Power PAD	16	2

SwitcherPro Design Report Layout

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A



SwitcherPro Design Report

Layout Notes

Design Name: TPS54160 60V to 3.3V @ 1A

Part: TPS54160

VinMin: 24V **VinMax:** 60V **Vout:** 3.3V **Iout:** 1A

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure for a PCB layout example. The GND pin should be tied directly to the power pad under the IC and the power pad. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Since the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.