

CSci 4230 Lab Assignment 3 (Assigned 4/6/2017, due 05/02/2017) :

You are provided a direct mapped cache implemented in systemverilog from the companion website for the textbook (<http://booksite.elsevier.com/9780124077263/appendices.php>) and need to solve the problems described below. Several useful tutorials for systemverilog can be found at <http://www.asic-world.com/systemverilog/>

Problem 1 (70 points):

Modify the given direct mapped cache and make it N-way set associative, where N can take values from 1 to 8. The top level module (dm_cache_fsm) should have an input parameter N which can be passed to it from the testbench. The replacement policy for the set-associative cache can be LRU (least recently used).

Problem 2 (30 points):

Modify the set-associative cache model you implemented to use the MRU cache replacement policy instead of the LRU cache replacement policy. The top level module should have an input parameter 'P' which can be used to select the active replacement policy. When P is 0 LRU should be active and when P is 1 then MRU should be active.

Handout :

You are provided a testbench (from the companion website), a direct-mapped cache implemented in systemverilog and this handout.

Handin :

Please turn in all the systemverilog files corresponding to your completed cache model in a tar.gz folder similar to the other lab assignments. It will be tested on a set of test-cases which are not provided to you. Your score will depend on the fraction of test-cases passed by the implemented cache model. Partial credit will be assigned if your code is well commented and documented but does not work.

Tools :

Please download Xilinx Vivado Webpack on your laptops (<https://www.xilinx.com/products/design-tools/vivado/vivado-webkit.html>) or use EDAPlayground (<https://www.edaplayground.com/>) to run your implemented code. Both these tools are available free of cost.