ECE 2700 Lab 3

Due the week of February 2, 2015 at the beginning of your session (100 points)

Objective

To become proficient in designing combinational circuits
using previously built components in Verilog.

1 Preparation

1. Read this document in its entirety.
2. Have the following circuit diagrams (or corresponding Verilog code) and truth tables ready **on paper in required format**.
   a) 3×8 decoder
   b) 3-bit majority function
   c) Voting System for Miniature University (you don't need to prepare a truth table for this one)

2 3×8 Decoder

Inside your `ECE2700` directory, create a new folder called `Lab3`. Start up Xilinx and create a new project called `Comb` inside the `Lab3` directory.

Create a new file called `dec3x8.v`. Inside, design a 3×8 decoder. Use the following declaration: `dec3x8(`$i2$`,` $i1$`,` $i0$`,` $d7$`,` $d6$`,` $d5$`,` $d4$`,` $d3$`,` $d2$`,` $d1$`,` $d0$`)`, where ix are the inputs and dx are the outputs ($i2$ is the most significant input bit and $d7$ is the most significant output bit).

Exhaustively test your design and show the results to the TA.

3 3-Bit Majority Function

Inside a new file called `maj.v`, design a 3-bit majority function. As its name implies, a majority function outputs (returns) 1 if more than half of the inputs are 1 (in our case, 2 or more input bits are 1). The inputs are a, b, and c. The output is F. **You are required to design this function using the 3×8 decoder you designed earlier**.

Exhaustively test your design and show the results to the TA.

4 Voting System for Miniature University

You are asked to design a voting system for Miniature University. The university has 3 students, 1 teacher, and 1 president. In this voting system, all the students get 1 vote collectively while both the professor and president each get one vote. Design your system in a file called `voting.v` **using instances of the 3-bit majority function constructed earlier**. The inputs to the system are $s2$, $s1$, $s0$, t, and p, where sx are students' votes, t is the teacher's vote, and p is the president's vote. The output is G.

Test your design. Since there are many test cases, you do not need to exhaustively test your system. However, select no fewer than 10 test cases and show the results to the TA. You are responsible for convincing the TA that your design is correct.

Implement your design on the Basys board. You have the freedom to assign pins as you see fit.

5 TA Checkoff

- (10 points) Prelab design
- (20 points) 3×8 decoder
- (20 points) Majority function
- (50 points) Voting system