EE 2361 - Le Jue 40 12/14/16

· Review

· Evaluations

Post Lectures 39, 40 + other odds & ends, + discussion is solution

## General Plann

Part 1. Introtou C + assembly and whitedure Part 2. Cooding for MC and bousic peripherale (I/O, PPS, Twens) Part 3. Advanced peripherals and other things

Final Exem 20 December 2016, 1:309 - 3:30 p In this room Same format as midterns 5 or 6 problema (weighted with regard to wictours)

## Review

1. Basic Computer Systems and mirrocontrollors

2. Instruction Sets and some computer whitectives (now do this fit together, how are mistructures executed)

Bosic to µ C is memory map 1. Harvard or von Neuman Archieter Justruct was dates in separato In same memou

PICRHFI'S a Harrowd Arch · ACME · Program Memora (Flash) 29-bit locations, these have additional "Jummy" 3-bits - Date memory (SRAM) 16 - bit words · SFR, (Specific Friction Registers)
(at motion of Jala momon) · Marchine instructions 201 bits (main reference is the Programmers Ref Manuel) Assembly hourgrage 1-1 with marking code · Higher Level language (like C) (XC16 User Manuel) all arress the Programuer Model

Assembly programming Several Classes of instructure · Arithmetic and hogic, etc.

operations CADD, SUB, MUL...) · Date Move instructions ( NOV ...

· Contral (BRA, JUMP. . . ) - Directures and pseudo-ops which tell the assention what to do

xvalue

Wn

Iwn?

· 6 addressing modes

The programmers model => registers to worry about PC - prog couler SR - stulus viegistes WO-WIS - working régisters · Resets and Interrupts Need to understand how an interrupt works.

Interrupts (PIC24F) vectored interrupts Interrupt Vector Tablo registers for each interrupt >> Flag bit IF. 1-bit
>>> Enable bit IE. + this - Interrupt Priorily IP-3 bits difference between interrupt and traip

## Date Structures

· FIFO grever (buffer)

· FILO gueur (steek)

Peripherals Control Régisters which are in the section of data memory where the SFRS also located. macros used in C to aces and domanique bite ex: PORTBbits.RBØ ?
- RBØ

Baric Periphernals - I/O: Bot, hatch, TRIS registor · PPS - peripheral più select · Times: Timer, Timers 2/3, 4/5 TROON, PRX I interocept, with peripherals

Advanced Peripherals - Communication (no cloch signed) Asynchronous SPI, IZC (have a clock) Synchronous > countrul, data hand vate associated registers

A/D paripheroal

- · How to configure PIN'S
- . Scomming /nosconning
  - . Samplehy
    - · Converting

under stend the truing (Tad, Tay)

Capture, Conpare, and PWM · Input compete coupling · Output conparce Lo Oc mode (1 or 2 tuers) L> PWM

Misc stuff - Low-Powerr - WAT