EE2361 - lecture 25

11/4/16

Note: New HW 4, due 11/9

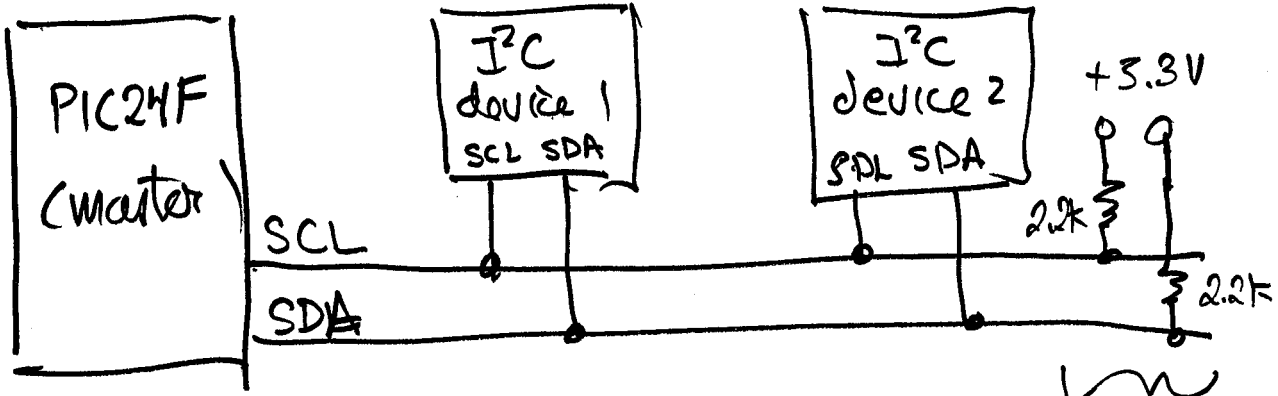
I^2C —

- Lucio Di Jasio, Programming 16-bit Microcontrollers in C: Learning to Fly the PIC24 (chapter 17) — SPI and I^2C.
- PIC24F FRM Section 24.
- Microchip, Using the C30 Compiler and the I^2C Peripheral to Interface Serial EEPROMS with dsPIC33F, AN1079.

I^2C = Inter-Integrated Circuit bus

- I^2C was introduced in 1980s by Philips (now NXP), has a formal specification
- Used to connect peripheral devices (as in other chips) to a microcontroller. Uses only 2-wires
- Simple, two wire, bi-directional serial interface

Configuration, I^2C



SCL = serial clock

SDA = serial data

need these for I^2C to work

Example of a Microchip E^2PROM 24xx256 has 3 pins A2, A1, A0

I^2C communicates with devices via a transaction, this is everything involved in sending data with the I^2C bus

Bytes on an I^2C bus are always sent MSb to LSb

The master always generates the clock signal and initiates transactions

Transactions start with SDA going from high to low when SCL is high

The byte of the transaction is a "command" byte containing the address and bit determing if this is a read or write

9th bit time is when the device receiving the data can acknowledge it.

0 — ACK acknowledgement

1 — NAK not acknowledge

Stop is indicated by a SDA low-to-high transition while SCL is high

⇒ the slave can hold SCL low to force a master into a wait condition

Example

Suppose we see the bytes 0xA4, 0x30, 0xAD, 0x4C (command byte | data) sent on an I^2C bus

- Is this a read or write transaction?

  0xA4 = 1010 010 0 ⇒ write

  (1010 010: address of the I^2C device)

- How many bytes of data are transferred?

  3 bytes, first byte is a command byte

Next Is implementing I^2C on the PIC24F

- Use the PIC24F I^2C modules
- Do bit-banging

PIC24F

17- registers associated with the I^2C module

(see the FRM, section 24)