EE2361 - Lecture 38
12/9/16

Last Time - Low-Power

2 references

AN1416 ⇒ Low-Power Design Guide

PIC24F ⇒ FRM, section 10 Power Saving Features

Power Saving Features in PIC24F devices

These include

- Clock Manipulation
- Instruction Based Power Saving
- Hardware based Doze Mode
- Selective Peripheral Control

⇒ discussed PIC24F FRM section 10

Clock Manipulation

clock speed is roughly proportional to dynamic power consumption.

For most µC you can

- Change Clock Speed
- Use Mulipe clock sources

Ref: is section 6 of PIC24F FRM

Instruction Based Power-Saving Modes
(All microchip 16-bit devices support these modes)

- Sleep Mode

  CPU, System Clock, any peripherals that use the system clock are disabled
  This is the lowest-power mode

- Idle Mode

  CPU is disabled, but not the system clock or peripherals that depend on it

There is an instruction that puts us in three modes

Format

PWRSAV #0 ; enter sleep mode

or

PWRSAV #1 ; enter idle mode

These are assembly instruction which is documented in the 16-bit Programmer's ref manual

User wake-up (exit sleep or idle modes)

with

- an enabled interrupt
- a WDT time-out
- a device reset

Doze Mode

⇒ Peripheral continues to operate at normal speed.

⇒ However the CPU is slowed.

In doze mode these two clock sources are synchronized so can continue to access the SFRs

Selective Peripheral Control

- Bit 15 in the control registers are the enable (on/off) bit
- Bit 13 is a selective disable bit, disable the peripheral in idle mode
  - ~~Port~~ Peripheral Module Disable bit in the PMD register