Lecture 2

9/9/16

Instructions

The operations done by a processor are controlled by a sequence of instructions. This sequence of instructions determines what operation the processor performs and even what instruction to execute next.

Instructions, like data, are binary words. In the PIC24 instructions are 24-bits in size! For the device we use in lab there are 76 base instructions.

(The PIC24 uses 16-bit data, which is why it is considered a 16-bit device)

PIC24 instructions are classed as[2]

move instructions	compare/skip and compare branch "
math "	program flow "
logic "	shadow/stack "
rotate/shift "	control "
bit "	

[2] 16-bit MCU and DSC Programmers Reference Manual, sec 3.2
[1] with the exception of CALL, DO, and GOTO which require 32-bits

On a stored program machine the program - a sequence of instructions is stored in memory. There are two ways to organize memory

A Harvard architecture stores the data and instructions in separate memories

A Von Neuman architetore store datce and instructions in the same memory

In a stored program machine the most fundamental operation is

fetch, decode, and execute

of instructions. This determines what operation is to be performed.

All the information needed for the machine to perform an operation is contained in the instruction for that operation

At the heart of all this is the idea of an instruction set is the idea of an instruction set architecture (ISA). The ISA is the complete specification of the interface between instructions and the underlaying computer hardware.

> "The ISA is an abstraction that describes the interface between hardware and low-level software"
>
> – Patterson & Hennessy [1]

The ISA will specify

- The set of instructions
- data Types
- addressing modes
- address space

We next take a look at the PIC24, specifically the PIC24FJ64A002 which is used in lab

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[1] David Patterson and John Hennessy, Computer Organization and Design, (Morgan Kaufmann, 2012)

Microcontroller History (is there a reference for this)

Background

- Modern (Electronic) computers have origins in machines built by

  Konrad Zuse (Z3)
  Mauchly & Eckert (ENIAC)
  Aiken (Mark I)

- Subsequent Development and commercialization

  - EDVAC (concept)
  - UNIVAC (commercial)

- Tube, transistor, IC → Technology
- Intel 4004, 8080 and 6800 ← to replace logic

  microprocessor – faster, expensive

  microcontroller – smaller, cheaper

- Other stuff – FPGAs etc

Microchip Microcontroller

The PIC24FJ64A002 microcontroller

Most modern PIC microcontrollers have their origins in the 8-bit PIC1650, a small NMOS microcontroller developed by General Instruments Microelectronics Division. The Microelectronics Division was bought by a group of venture capitalists in 1989 and became Microchip

Microchip currently has 3 main classes of microcontrollers

- 8-bit (data size)

  PIC10, PIC12, PIC16, PIC18

- 16-bit

  PIC24 and dsPIC

- 32-bit

  PIC32

generally, the number with PIC represents the instruction size

The PIC24FJ64GA002 Microcontroller

The PIC24 and the dsPIC families of devices comprise Microchips 16-bit micro controllers. Microchip describes the PIC24 as an MCU (microcontroller unit) and dsPIC as a DSC (digital signal controller)

Both families share a common architecture and instruction set. The dsPIC devices however contain additional hardware and instructions to facilitate "number crunching"

The PIC24 family has 3 main catagories,

- PIC24F lower speed / lower power 3.3V
- PIC24H first high speed to 40MIPS 3.3V
- PIC24E latest high speed to 70 MIPS 3.3V

For dsPIC

- dsPIC30 5.0 V
- dsPIC33F & dsPIC33E 3.3V

PIC24FJ64GA004 FAMILY

28/44-Pin General Purpose, 16-Bit Flash Microcontrollers

High-Performance CPU

- Modified Harvard Architecture
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Internal Oscillator with 4x PLL Option and Multiple Divide Options
- 17-Bit by 17-Bit Single-Cycle Hardware Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16-Bit x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture:
  - 76 base instructions
  - Flexible addressing modes
- Two Address Generation Units (AGUs) for Separate Read and Write Addressing of Data Memory

Special Microcontroller Features

- Operating Voltage Range of 2.0V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins
- Flash Program Memory:
  - 10,000 erase/write
  - 20-year data retention minimum
- Power Management modes:
  - Sleep, Idle, Doze and Alternate Clock modes
  - Operating current: 650 μA/MIPS, typical at 2.0V
  - Sleep current: 150 nA, typical at 2.0V
- Fail-Safe Clock Monitor (FSCM) Operation:
  - Detects clock failure and switches to on-chip, low-power RC oscillator
- On-Chip, 2.5V Regulator with Tracking mode
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with On-Chip, Low-Power RC Oscillator for Reliable Operation
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Debug (ICD) via 2 Pins
- JTAG Boundary Scan Support

Analog Features

- 10-Bit, up to 13-Channel Analog-to-Digital Converter:
  - 500 ksps conversion rate
  - Conversion available during Sleep and Idle
- Dual Analog Comparators with Programmable Input/Output Configuration

Peripheral Features

- Peripheral Pin Select (PPS):
  - Allows independent I/O mapping of many peripherals
  - Up to 26 available pins (44-pin devices)
  - Continuous hardware integrity checking and safety interlocks prevent unintentional configuration changes
- 8-Bit Parallel Master/Slave Port (PMP/PSP):
  - Up to 16-bit multiplexed addressing, with up to 11 dedicated address pins on 44-pin devices
  - Programmable polarity on control lines
- Hardware Real-Time Clock/Calendar (RTCC):
  - Provides clock, calendar and alarm functions
- Programmable Cyclic Redundancy Check (CRC)
- Two 3-Wire/4-Wire SPI modules (support 4 Frame modes) with 8-Level FIFO Buffer
- Two I^2C™ modules Support Multi-Master/Slave mode and 7-Bit/10-Bit Addressing
- Two UART modules:
  - Supports RS-485, RS-232, and LIN/J 2602
  - On-chip hardware encoder/decoder for IrDA®
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
  - 4-level deep FIFO buffer
- Five 16-Bit Timers/Counters with Programmable Prescaler
- Five 16-Bit Capture Inputs
- Five 16-Bit Compare/PWM Outputs
- Configurable Open-Drain Outputs on Digital I/O Pins
- Up to 3 External Interrupt Sources

Device	Pins	Program Memory (bytes)	SRAM (bytes)	Remappable Peripherals						I^2C™	10-Bit A/D (ch)	Comparators	PMP/PSP	JTAG
				Remappable Pins	Timers 16-Bit	Capture Input	Compare/ PWM Output	UART w/ IrDA®	SPI					
PIC24FJ16GA002	28	16K	4K	16	5	5	5	2	2	2	10	2	Y	Y
PIC24FJ32GA002	28	32K	8K	16	5	5	5	2	2	2	10	2	Y	Y
PIC24FJ48GA002	28	48K	8K	16	5	5	5	2	2	2	10	2	Y	Y
PIC24FJ64GA002	28	64K	8K	16	5	5	5	2	2	2	10	2	Y	Y
PIC24FJ16GA004	44	16K	4K	26	5	5	5	2	2	2	13	2	Y	Y
PIC24FJ32GA004	44	32K	8K	26	5	5	5	2	2	2	13	2	Y	Y
PIC24FJ48GA004	44	48K	8K	26	5	5	5	2	2	2	13	2	Y	Y
PIC24FJ64GA004	44	64K	8K	26	5	5	5	2	2	2	13	2	Y	Y

CPU or Processor

Fig 1-1 outlines the PIC24F CPU core block diagram.

Two main parts of this are important.

The 16-bit W register array consists of 16 working registers which are mostly general purpose registers which hold data used in instructions.

The data is processed by the 16-bit ALU which used to implement many operations such as add, sub, logic operations, shift operation, etc.

arithmetic and logic unit

Note that additional hardware such as the hardware multiplier and divide support are included to enhance these operations.

Much of the remainder of the block diagram concerned with accessing memory

FIGURE 3-1: PIC24F CPU CORE BLOCK DIAGRAM

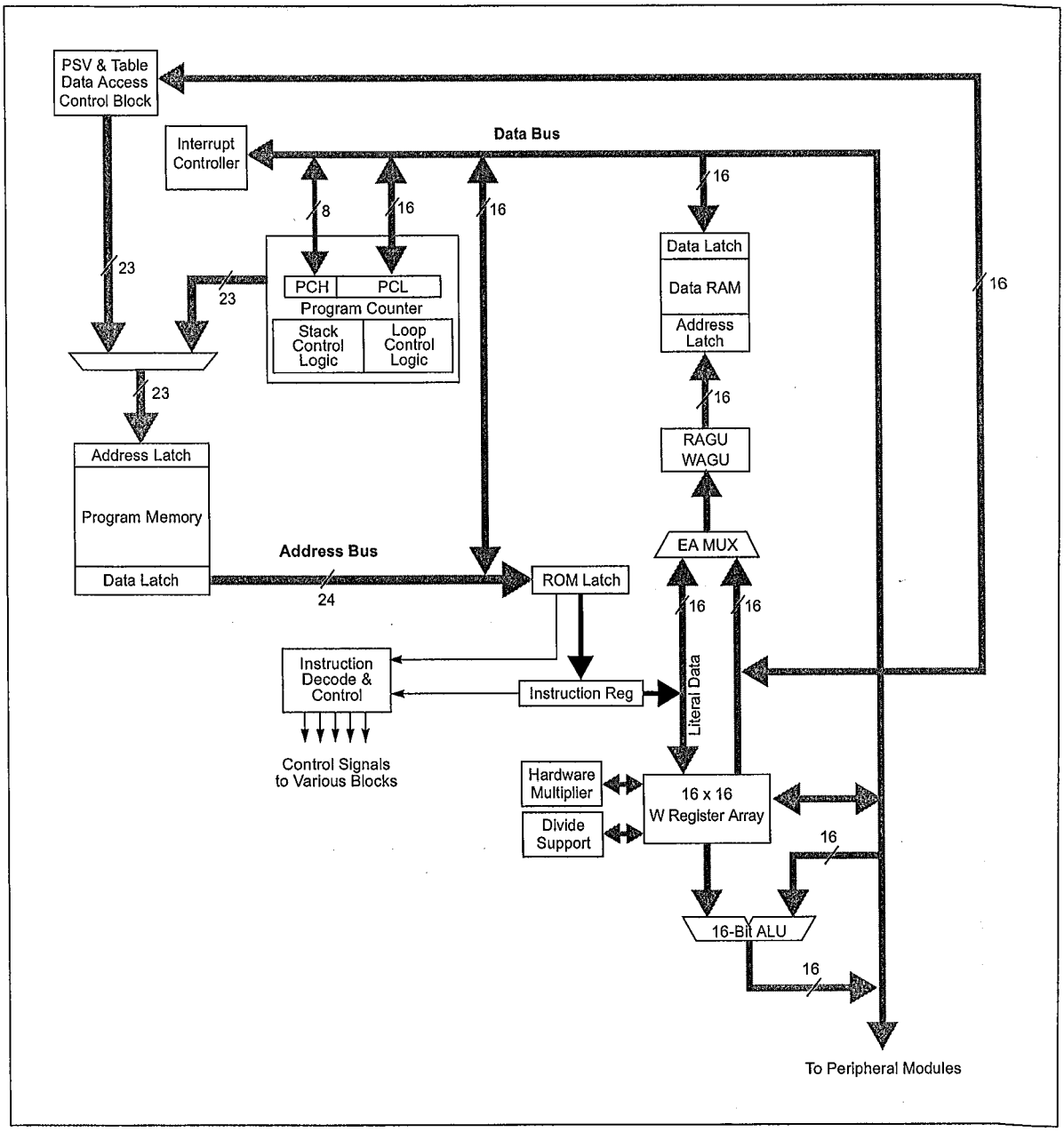
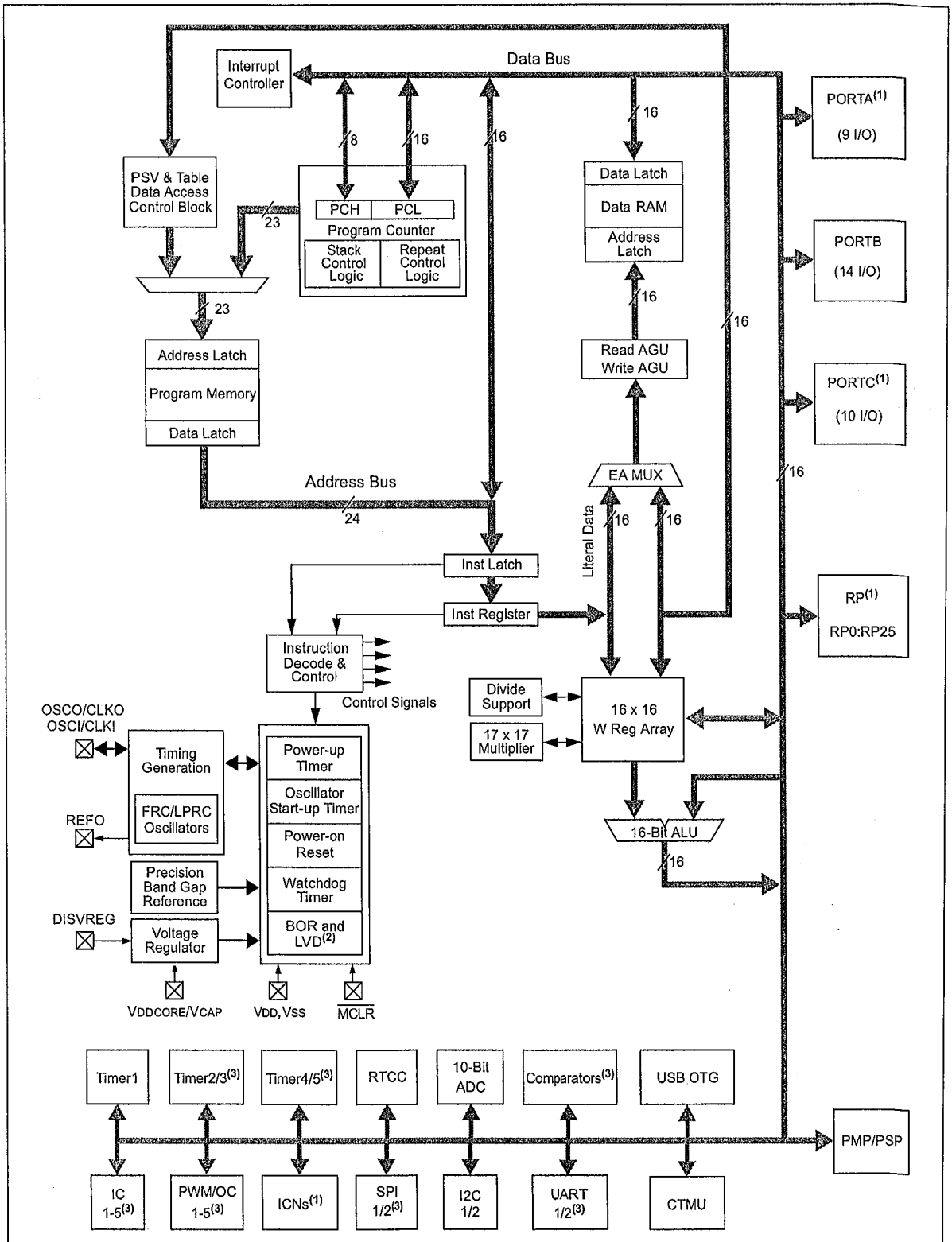
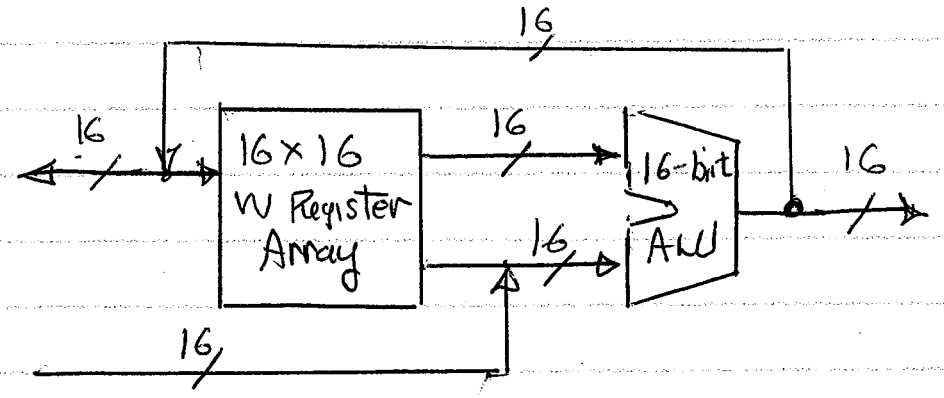


FIGURE 1-1: PIC24FJ64GB004 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-2 for specific implementations by pin count.
2: BOR functionality is provided when the on-board voltage regulator is enabled.
3: These peripheral I/Os are only accessible through remappable pins.

Basically we have



Note that the data is all 16-bits

Figure 1-1 shows the overall arrangement of the microcontroller

CPU - Instruction decode
working registers and ALU

Memory - Program Memory (Instructions)
Data Memory (Data)

I/O - PortA, PortB, PortC

Peripherals - Timers, RTCC, ADC,
Comparators I2C, SPI,
etc.

TABLE 3-1: CPU CORE REGISTERS

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
PSVPAG	Program Space Visibility Page Address Register
RCOUNT	Repeat Loop Counter Register
CORCON	CPU Control Register

FIGURE 3-2: PROGRAMMER'S MODEL