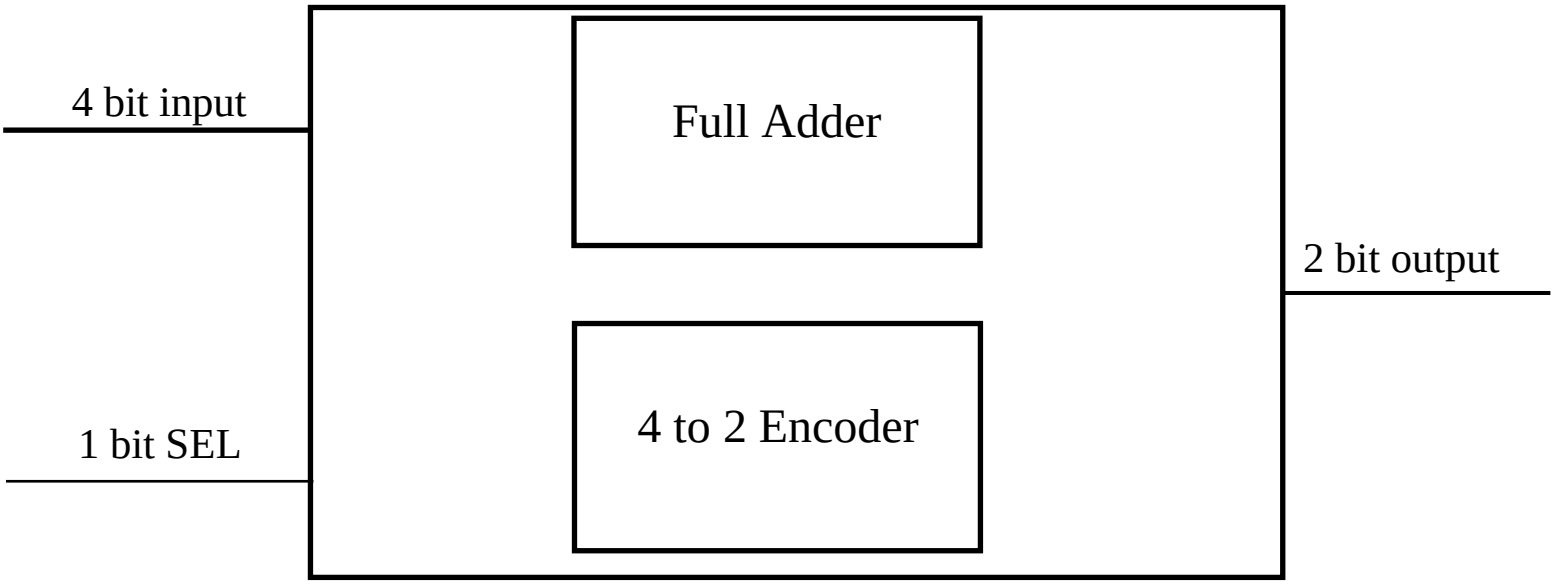
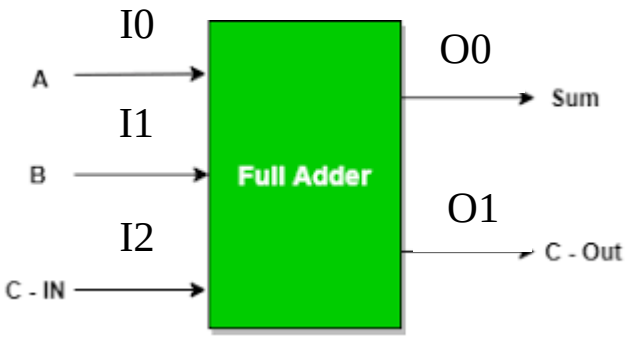
Assignment 1

Write source code and testbench for the entity



Full Adder



4 to 2 Encoder

Input				Output	
I3	I2	I1	I0	O1	O0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

*1 bit SEL decides to output the result of Full Adder or Encoder

*No need to consider other input situations in 4 to 2 Encoder

*Submit the project folder in compressed format (e.g., zip) with a screenshot of simulation wave in Modelsim