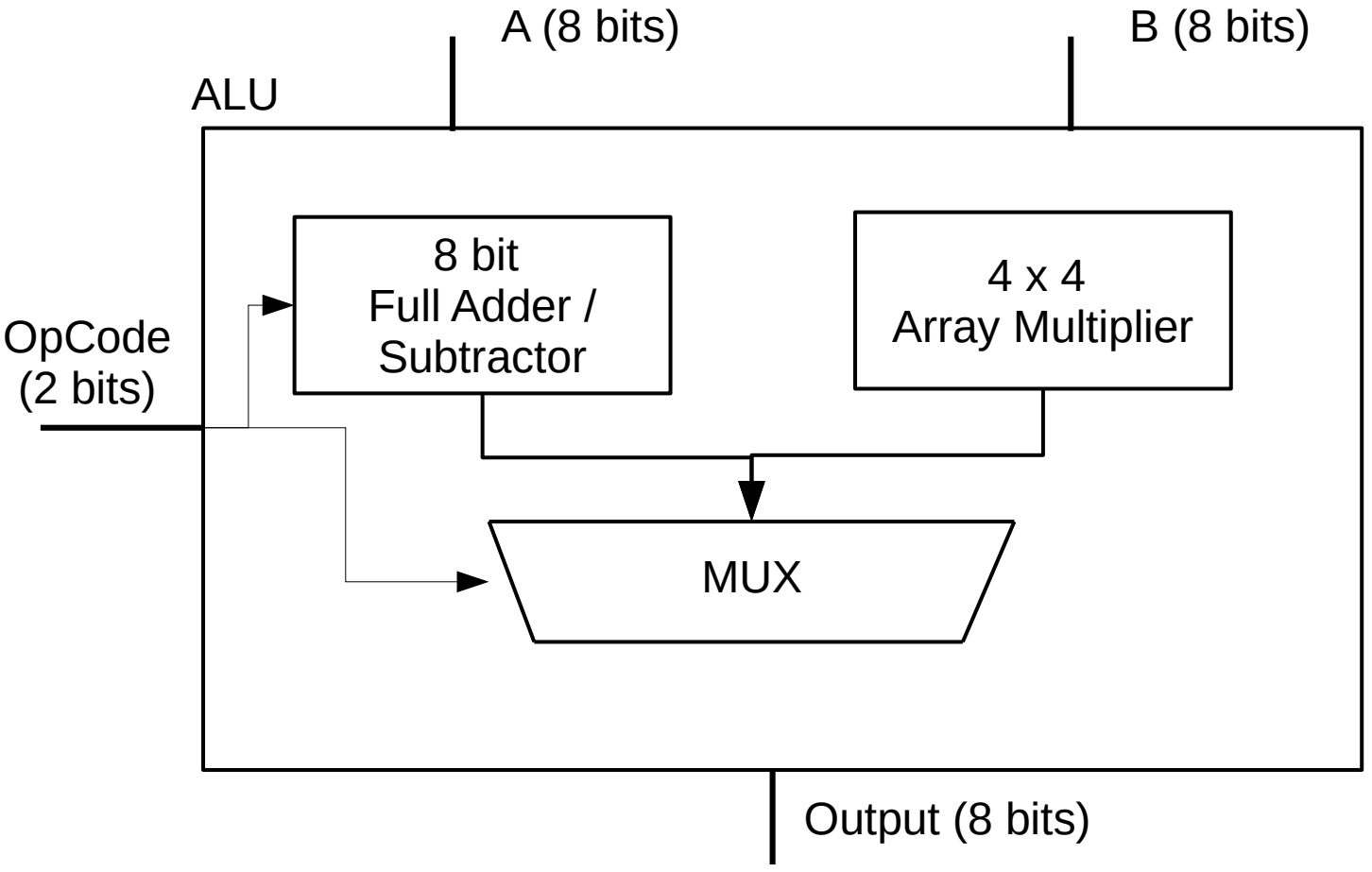
Simple 8 bit ALU (Arithmetic Logic Unit)



OpCode	Operation
0 0	A + B
0 1	A - B
1 0	A * B

top level entity includes both structural and dataflow (same logic as in assignment 1)

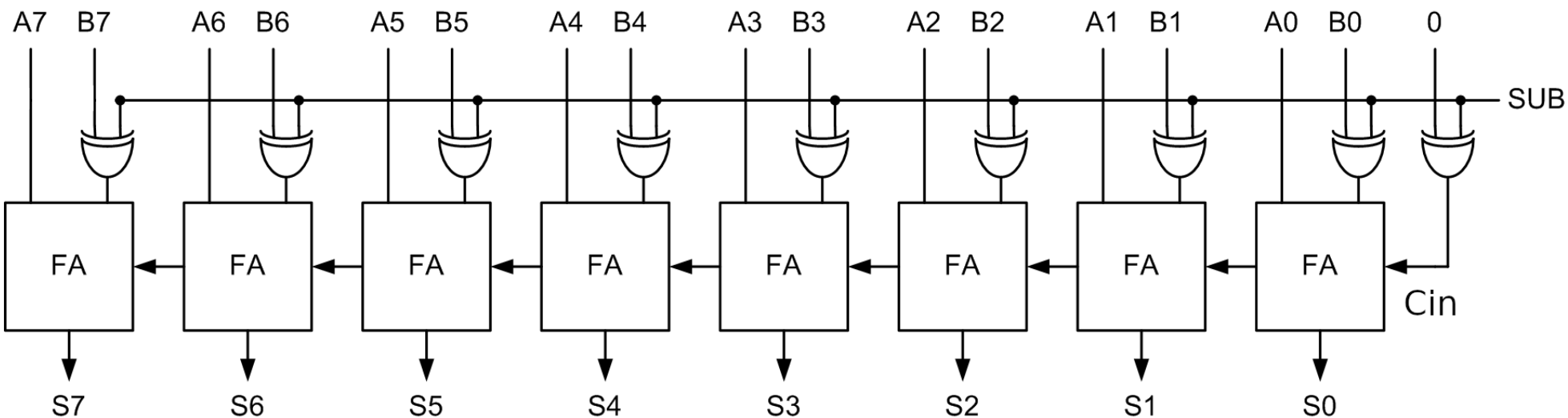
For the input of the 4 x 4 Array Multiplier **please use A[3:0],B[3:0]**

8 bit Adder / Subtractor

FA = Full Adder, all gates are **XORs**

When **SUB** = 0 the circuit works as an Adder, otherwise as a Subtractor.

Please use generate command! (structural code please)



4x4 Array Multiplier

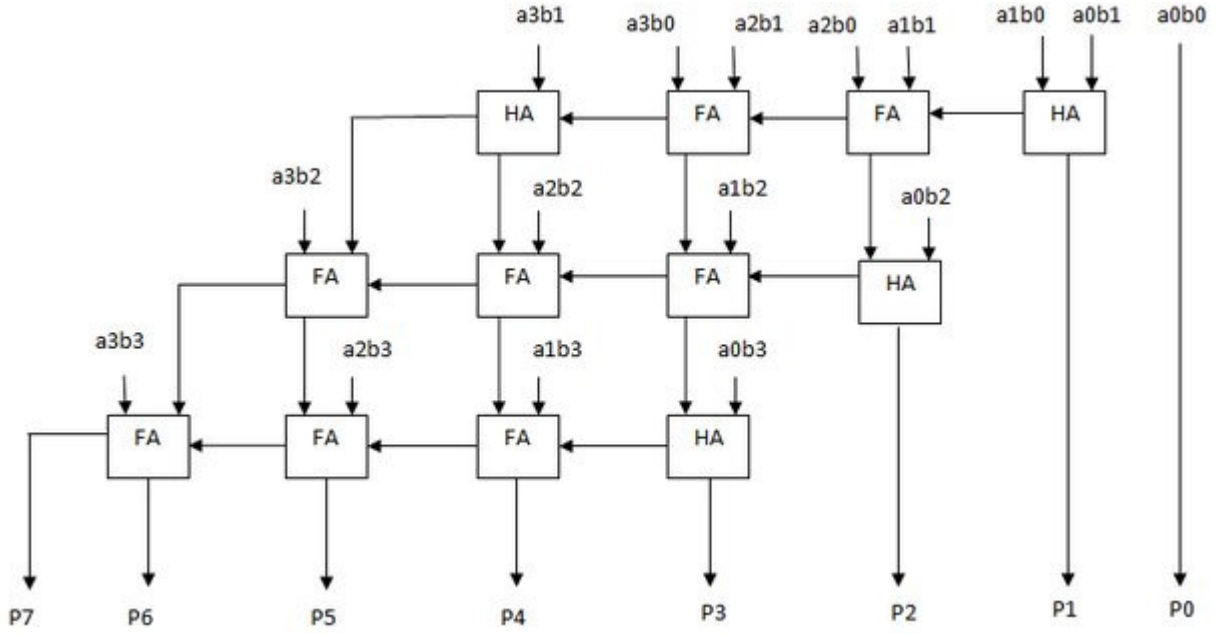
a0b0 → A0 AND B0
a0b1 → A0 AND B1
etc...
In total we need 16 AND gates!

FA = Full Adder, **HA** = Half Adder

P0...7 = 8bit Product

Please use generate command! (structural code please)

This is a Shift-Add implementation of an array multiplier. First we compute a set of partial products and then we sum the partial products together. Same as we multiply numbers on paper.



Please upload your code (including testbench)

+ a pdf with screenshots of your results.