LITERATURE REVIEW

Exploring the Viability of Widespread Adoption of RISC-V Architecture in Mobile Phones: Prospects and Challenges

Haoting Chen

ANU | U7227871

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1. Introduction

1.1 Introduction to RISC-V

RISC-V is an instruction set architecture (ISA) first published by UC-Bakery in 2010 [1]. The design of RISC-V is modular, with the basic instruction set containing only 47 instructions and various official and custom extensions providing different functionalities, such as vector operations [2]. This allows RISC-V to be flexibly adopted in many areas, from embedded systems to high-performance computing (HPC) [2]. RISC-V is also open-source, which means everyone can contribute to its development and use without paying a proprietary fee [1]. In recent years, RISC-V has become a research hotspot in industry and academics [1,6,8]. Some authors think RISC-V can potentially end the dominant situation of x86 and ARM on ISA in the future [6,8].

1.2 Proposal Introduction

The objective of this research is to assess the viability of the widespread adoption of RISC-V in mobile phones. The outcome holds significance for researchers, investors, and engineers who wonder if RISC-V has a bright future in the mobile phone area before conducting substantial studies and investments in RISC-V development. The analysis will cover RISC-V mobile phones' intrinsic properties, hardware ecosystem, software ecosystem, security, and other external factors. Sources will mainly be obtained from literature articles, news, industry reports, and technical specification documents. SWOT analysis will be used in the final stage to summarise all the internal and external factors impacting the viability. The evaluation will focus on the data collection and processes, decisions made during the research and the quality of the outcome. [11]

1.3 Literature Review Introduction

The literature review is conducted by visiting the digital database of ACM (Association for Computing Machinery), CNKI (China National Knowledge Infrastructure), and IEEE (Institute of Electrical and Electronics Engineers). Throughout the literature, some articles have been found to discuss the prospect of RISC-V [6,7,8] explicitly. However, most are from a general perspective or the view of Internet of Things (IoT) applications [2,6,7,8]. By 18 May 2023, searching with the combination of the keywords “RISC-V” and “mobile phone” on ACM, CNKI, and IEEE would find no result. Nevertheless, there are still personal videos and blog articles online explicitly discussing the RISC-V mobile phone prospect. Therefore, the research gap is to relate RISC-V and mobile phones academically. Ten articles were selected as the most relevant sources during the literature review. The findings of these articles, the advantages and challenges of RISC-V from different perspectives, provide valuable base knowledge and evidence to answer the research question. Since most articles are from general perspectives and some may not be up to date, the literature review also reveals gaps that may need to fill through the research in the later stage. Section 2 contains the summaries of each ten articles. Sections 3 to 9 are the key findings from the literature that contribute to evaluating the feasibility of widespread RISC-V adoption in mobile phones.

2. Brief Literature Summary

[1] Survey on RISC-V System Architecture Research

Liu et al.’s article provides a comprehensive summary of RISC-V, including its properties and historical background, specification of basic and extension instruction set, a survey on hardware and emulator, the goal and

challenges of designing a RISC-V operating system (OS) and finally its prospect. This article enhances my background knowledge of RISC-V and provides valuable evidence from intrinsic properties, software ecosystems, and hardware ecosystems to answer my research question.

[2] RISC-V Instruction Set Architecture Extensions: A survey

Cui et al.'s article comprehensively surveys different official and custom RISC-V extensions and derived applications. As RISC-V is modular, combining different types of extensions can lead to various applications. This article provides knowledge mainly from the hardware perspective. It also explores some alternative potential applications of RISC-V on mobiles, such as graphics processing units (GPU) and 5G signal processing units other than CPUs.

[3] Performance Evaluation of Various RISC Processor Systems: A Case Study on ARM, MIPS and RISC-V

Liu et al.'s article provides a side-by-side benchmark comparison between ARM, RISC-V, and MIPS processors, which is closely relevant to my research because having performance advantages is an essential factor for customers choosing RISC-V-based mobile phones. However, there is a limitation where the benchmark is done through emulation instead of running on physical chips.

[4] A Survey of the RISC-V Architecture Software Support

Mezger et al.'s article provides the background knowledge of both hardware features and the software ecosystem of RISC-V to my research. The article first surveys RISC-V's current research progress and implementation examples on hardware, including processor core, Socs, and emulators. Then it analyses the software ecosystem, including OS and development tools. Finally, it demonstrates how RISC-V hardware's security, reliability, and low-power feature promotes a good software ecosystem.

[5] Building an Open-Source Linux Computing System On RISC-V

Ince et al.'s article discusses the processes and challenges of porting MILIS Linux to the RISC-V architecture. The paper concludes by highlighting the importance of open-source hardware and operating systems in creating a secure and independent computing environment. The findings of the article may become a reference for analysing the prospect and challenges of porting Linux-based Android on a RISC-V processor.

[6] Will RISC-V Revolutionize Computing?

Greengard's article first introduces RISC-V's properties: openness, modularity, non-proprietary, and low learning cost. From these properties, it further analyses the advantages of the widespread adoption of RISC-V, including high industrial and research engagement, security and cost advantage. However, the fragmentation, interoperability, and counter strategy taken by its competitor, such as ARM, also impedes its success. Overall, the author gives an optimistic view of the future of RISC-V. Although the article is from the general perspective of RISC-V, it is in the same direction as my research, where both focus on RISC-V's prospects.

[7] From low-power consumption to high-performance applications, what are the prospects for RISC-V's advancement

Li's article first surveys the current application of RISC-V chips in the IoT area. Then it analyses the advantages and challenges for RISC-V to target high-performance applications, which include immature software ecosystems, fragmentation issues, high security, and low cost. It also provides brief solutions to the challenges. Since mobile phone adoption lies within high-performance applications [2], the finding from this article highly relevant to my research.

[8] Current Status and Future Opportunities of Open-source Chip Ecosystem based on RISC-V

Zhong's articles first introduce RISC-V's simplicity, modularity, and openness characteristics. Then, talks about RISC-V development opportunities, including the relatively low threshold for chip designs and high industrial engagement because of its openness. The challenge of RISC-V adoption comes from the monopoly of ARM and x86, which have a much more mature ecosystem than RISC-V, and its fragmentation issue. The article concludes that RISC-V still has a long way to go into traditional fields such as servers, desktops, and mobile phones.

[9] A Survey on RISC-V Security: Hardware and Architecture

Lu's article covers the current research progress on RISC-V's hardware and architecture security. It also explores the solutions and technologies to address these challenges, such as security extensions and memory protection. Lu concludes with the advantages and challenges of RISC-V security, such as the flexibility of adding security extension and the lagging of security search of RISC-V compared to other architectures.

[10] Xuantie-910: A Commercial Multi-Core 12-Stage Pipeline Out-of-Order 64-bit High Performance RISC-V Processor with Vector Extension

Chen et al.'s article provides detailed specifications for the leading high-performance general-purpose RISC-V processor Xuantie-910. In addition, the article also undertakes rigorous benchmarks to compare Xuantie-910 with Arm's Cortex-A73, designed for mobile phones. As the first RISC-V processor successfully runs Android [2, 16] and its research outcome is also open-source [2, 16], the performance of Xuantie-910 is an important starting point and reference to estimate the future of RISC-V on mobile phones.

3. Problem of the Currently Dominant ISA

Liu et al. highlight the following three issues [1] within the current dominant ISA, ARM and x86. Cui et al. [2] and Li [7] also mention the lack of openness in their articles.

3.1 Lack of Openness

Both ARM and x86 are closed and proprietary [1]. Chip designers implementing these ISA must pay a high licence fee and cannot modify their ISA freely [1]. This raises the barrier for many companies to participate in chip design due to the lack of shared technologies, consequently leading to chip industry monopolies [7]. The closed nature also impedes community-driven innovation and improvement of their ISAs [1, 2].

3.2 Historical Burden

Due to their long-term development and iterations, both ARM and x86 must consider backward compatibility to support some currently outdated features. This can complicate the ISA designs and makes processors less efficient. As a new ISA designed from scratch, RISC-V eliminates the need to consider historical legacy problems and can focus more on innovation. [1]

3.3 Documentations are Numerous and Complicated

The documentation for ARM and x86 is numerous and complicated, increasing learning costs. For example, the official ARMv8-A specification document has 8528 pages for the first volume alone. In contrast, The RISC-V specification document consists of only two volumes with a total of 329 pages. [1]

4. RISC-V Intrinsic Properties

The literature has a consensus that RISC-V has the proprieties of openness and modularity. [1,2,3,4,6,7,8,9,10]. In addition, Liu et al. [1], Liu et al. [3], and Megaer et al. [4] highlight in their papers the simplicity of RISC-V.

4.1 Openness

RISC-V is open-source under the BSD License [5], which allows everyone to modify, republish and use it commercially [8]. The openness allows a wide range of people to participate in the RISC-V agile development [8] by sharing projects, ideas, and patches [5]. The openness also promotes transparency to allow a more thorough security analysis, which will be further discussed in Section 7 [6, 9]. The non-proprietary reduces the costs of designing chips [6].

4.2 Modularity

The RISC-V documentation defines four basic integer instruction sets, RV32I, RV32E, RV64I, RV64E, and RV128I, and a wide range of instruction set official extensions which provide extra functionality [2]. For example, the C extension provides instruction compression from 32-bit to 16-bit to reduce code size [2]. Researchers can also innovate new extensions to suit specific requirements [2]. Processors implementing RISC-V must include one of the basic instructions sets and none or multiple extensions [2]. Compared with the one-size-fits-all approach of ARM and x86, chip designers can only implement extensions that provide the features they need for simplicity [6]. This also allows RISC-V to become domain-specific processors, such as AI accelerators and GPUs [2]. The modularity also provides the potential to build HPC or general-purpose processors [2] with various extensions combined. For example, Xuantie-910 has implemented C (instruction compressions) and V (vector operations) extensions to become general-purpose processors for mobile phones, servers, and desktop processors.

4.3 Simplicity

Compared to ARM, RISC-V is more concise [10]. There are only 47 basic instructions [8], and all instructions can be divided into just six types (R, I, S, U, B, J) according to the structure. For example, R-type stands for register-register instructions, and S-type stands for store instructions. This simplifies compilers' encoding and decoding process [4], which reduces the complexity of development toolchain and processor execution costs and further facilitates software and hardware ecosystem development [10]. The reduced learning costs due to simplicity allow many universities, such as the University of Cambridge and Tsinghua University in Shenzhen, to use RISC-V chips in their teaching [6]. Li’s article [7] further points out that the future of the RISC-V industry depends on how many students have taken RISC-V courses before graduation.

4.4 Discussion

The three main properties summarised from the articles imply some potential advantages for the success of RISC-V. Based on its intrinsic properties only and compared with the current issues of ARM and x86, RISC-V has a promising future. However, the future of RISC-V may not imply the future of RISC-V on mobile phones. Therefore, further primary and secondary research is to explore how openness, modularity, and simplicity specifically contribute to the success of RISC-V on mobile phone processors and OS.

5. RISC-V Hardware Ecosystem

5.1 Performance of Leading RISC-V Processors

Processors' performance is one of the critical factors for customers to choose a phone. Therefore, RISC-V processors' performance highly affects the widespread RISC-V mobile phones. Liu et al. [10] have provided a side-by-side comparison between RISC-V, ARM, and MIPS processors. In their study, they first set up three containers to ensure a unified testing environment. Then, QEMU was installed in these three containers to emulate a RISC-V, ARM, and MIPS processor, respectively. Linux was running on the emulated processors, and UniBench and LMBench were used to measure their performance. The result shows that RISC-V has significantly strong string processing and floating-point computing capabilities over ARM and MIPS, especially for multi-cores, but much longer file copying delay, slower pipe throughput and slightly longer process switching and process creating than ARM. Through Liu et al.'s research, it can be found that RISC-V processors do not have significant overall advantages over ARM. Liu et al.'s research outcome have revels two limitations. The first is that the information on what precisely the processors are emulated is missing. Second, testing on emulators is less accurate on physical hardware [3].

Chen et al.'s study [10] also conducted a benchmark comparison between RISC-V Xuantie-910 and the 2016 flagship ARM Cortex-A73. Xuantie-910 is the first processor successfully running Android by T-head in 2020 [2, 16], and ARM Cortex-A73 is widely used in mobile phones' Soc, such as Kirin 960 [10]. Therefore, the result can somewhat represent the future of RISC-V on mobiles. As shown in Figure 1, the performance of Xuantie-910 and ARM Cortex-73 are generally at the same level. However, it should be noted that Xuantie-910 was released in 2019 [10], and there is a three-year technology gap between them. In addition, other factors, such as size, energy efficiency, and price, are not covered by the recent literature articles [3,10] but are essential for mobile phones.

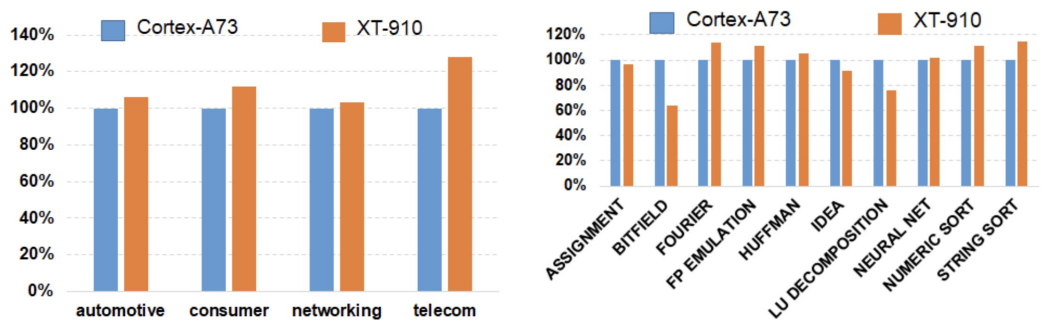

Figure 1: the performance comparison between Cortex-A73 and XT-910 [10]

5.2 Discussion

The two articles above reveal a research gap in a side-by-side comparison between physical general-purpose RISC-V and ARM processors for mobile phones with more comparison matrices. Therefore, gathering and evaluating third-party benchmark reports or obtaining the processors to do benchmarks to gather primary data is required for future research. This ensures a more rigorous answer to my research question.

5.3 Availability of RISC-V Processors for Mobile Phones

The processors potentially used in phones are high-performance and general-purpose processors. Liu et al.'s [1] study summarises 12 typical general-purpose RISC-V processors. For example, Rocket, freedom, and BOOM processors have more comprehensive instruction sets which can fit various OS and application scenarios [1]. SCR5, XuanTie-910, and RiscyOO have more advantages in performance. Nevertheless, Chen et al. [10] point out that throughout the performance spectrum, most RISC-V controllers belong to the microcontroller class, and the availability of 64-bit high-performance RISC-V processors is still limited. This observation is further supported by Cui et al. [2], who highlight the disparity between RISC-V x86 and ARM and x86 in the high-performance domain.

5.4 Academic and Industrial Activeness in RISC-V Extensions Research

As RISC-V is modular, having different extensions can significantly affect the application and performance of RISC-V processors [2]. Therefore, research on RISC-V custom extensions ensures a good hardware ecosystem. Both Liu et al. and Cui et al.’s survey research show high research activeness in different RISC-V extensions [1,2]. Liu et al. summarise in their article that the RISC-V instruction set architecture is currently in a vibrant development phase, with various instruction sets being proposed for different application environments [1]. For example, EdgeQ develops over 50 custom extensions aimed at enhancing the performance of 5G signal processing [2]. Elsabbagh et al. has proposed Vortex, a GPU using RISC-V with a peak performance of 25.6 GFlops [2]. Although there is no official extension for graphic computing [2], developing custom extensions makes RISC-V GPUs possible. However, it should be noted that 25.6 GFlops is far behind the performance of a phone's GPU. For example, the GPU, Adreno 730, in the current flagship phone Soc of Qualcomm 8, performs 2513 Gigaflops [12]. The above reveals the potential application of RISC-V in other components of mobile phones besides CPUs, even though having them applied to mobile phones will still have a long way to go. For general-purpose CPUs, the activeness of RISC-V extensions continues to enrich their security and functionality features [2].

6. RISC-V Software Ecosystem

The promotion of ISA highly depends on the construction of the software ecosystem [8]. In recent years, relying on its robust software ecosystem, Apple has enabled its ARM-based PCs to challenge traditional x86 PCs [8]. Emulators, OSs, compilers, development toolkits, and application software are the components of the software ecosystem of an ISA.

6.1 Current State of the Software Ecosystem

Mezger et al.’s [4], Li’s [7], and Zhong’s [8] article has given an overview of the RISC-V software ecosystem. Despite being relatively new in the market, compilers, state-of-the-art OSs, and development toolkits have been found in the software ecosystem [4]. Mezger et al. has explained how RISC-V's openness and simplicity properties (mentioned in Section 4) promote the software ecosystem [4]. The openness allows developers to build robust

software to satisfy various requirements [4]. The simplicity in architecture makes it easier for engineers to develop software to support RISC-V, compared to ARM and x86 with growing architectural complexity [4].

6.2 Emulators for RISC-V

Liu et al.'s [1] and Mezger et al.'s [4] studies have surveyed the currently available RISC-V emulators. By the publishment of Liu's study, there were 24 emulators for RISC-V serving various RISC-V research [1]. Among them, Spike and QEMU are the most repressive, as suggested by Liu [1] and Mezger et al. [4]. They both have a wide range of adaptability and can simulate both embedded and general-purpose processors [1], such as SiFive's HiFive Unleashed. QEMU is the emulator used by Liu et al.'s [5] comparison study of ARM and RISC-V performance, as discussed in Section 5.1. The above shows how emulators support RISC-V research.

6.3 OS for RISC-V

A unified OS is essential for RISC-V to target high-performance applications, as Zhong [8] discussed, and RISC-V has yet to achieve. Even so, Google has officially announced making its Android support RISC-V in 2023 [13], which is a good start for the RISC-V adoption in mobile phones. Chen et al. give a positive prospect to RISC-V OS [10]. As they mention, RISC-V gradually appears as the mainstream platform of Unix or Linux OS [10]. The maturity of development toolchains, such as GNU/GCC/GDB and LLVM, reduces software development costs and enhances software experiences [10]. However, Ince [5] also highlights the challenges when building a RISC-V Linux. The first is limited kernel support. Since RISC-V is still relatively new, ongoing work is still required related to the kernel and user space [10]. The second is toolchain compatibility. Currently, not all toolchains are compliable with RISC-V. The third one is bootloader configuration. The paper uses Berkley Bootloader (BBL) to boot the Linux Kernel. However, BBL has a limitation. Whenever the kernel is updated or modified, the BBL must be rebuilt. And the separation between BBL and the kernel is still under research. [5]

6.4 Discussion

The literature above has covered the software ecosystem of RISC-V from the perspective of OS, emulators, OSs, compilers, and development toolkits. However, the application software part is still missing from the literature. This is because the RISC-V OS for mobile phones is still in its early stage. After the release of Android for RISC-V, more information about the software ecosystem from the application software perspective will appear. Reviewing news articles will be a process later to see how well Android support RISC-V and how well companies engage in developing apps on the RISC-V platform.

7. RISC-V Security

Nowadays, phones store plenty of personal information, and thus the security of RISC-V is fundamental when adopted in mobile phones.

7.1 Security Overview

Lu's [9] study has given a comprehensive survey on research done for enhancing RISC-V security. Currently, physical memory protection, multiple privilege modes, and trusted execution environments are supported by RISC-V [9]. Ince [5] also talks about memory protection. The absence of speculative memory access in the RISC-V processor eliminates hardware vulnerabilities like the Meltdown-Spectre vulnerability [5]. The Meltdown-

Spectre vulnerabilities allow attackers to access sensitive information from a computer's memory that should be protected. It is affecting modern processors, such as ARM Cortex-A75 [14]. In addition, many security measures are proposed, such as cryptographic engines and side-channel prevention [9]. Although RISC-V has advanced security features over ARM, Lu [9] concludes that the security ecosystem for RISC-V is still immature. More security tools, libraries, and measures against attacks are still being developed. The second point is the limited availability of third-party secure hardware components supporting RISC-V architecture [5].

7.2 Security Advantages and Challenges Due to Openness

As stated by Lu [9], the openness of RISC-C allows the public to examine its architectural design so that there are more opportunities for improvement with innovative security approaches. This especially helps identify and alleviate vulnerabilities [9]. This argument is also mentioned in Ince's [5] and Greengard's [6] article. Greengard's article further explains that most processors today are like black boxes. Still, RISC-V allows users to understand more precisely what is happening on the chip and even create their security features [6]. Both Lu [9] and Greengard [6] agree that openness is also demonstrated by its support for customisable security features, which allow users to apply or create different security extensions [6]. However, the openness also makes it easier for attackers to explore and exploit vulnerabilities [9].

Li [7] also discuss security from another angle. With openness and shared technology, more companies can participate in chip design and production [7]. This ensures RISC-V chips are not in the hands of a few suppliers, increasing phone companies' supply chain security [7]. Having a constant chip supply is vital for phone markers.

7.3 Fragmentation Issue

The fragmentation issue comes with RISC-V's openness and modularity properties and affects its software, hardware, and security ecosystem. This issue is all mentioned by Greengard [6], Li [7], Zhong [9], and Lu [9].

The modularity of RISC-V gives hardware designers the freedom and flexibility to apply different instruction extensions to meet their needs [8]. This increases variance in a chip implementation and makes it harder for chips to standardise [8]. The difference in instruction sets and extensions impedes adopting a unified operating system because the compilers and toolkits may have to adapt to each RISC-V variation [7].

The diversity of RISC-V implementation by different companies also makes their security features various [9], leading to inconsistencies in security standards and practices.

To address this issue, corporation between hardware designers is needed [7], which includes technologies and information sharing so that more standardised and advanced chips can be designed and compilers and toolkits are unified [7].

8. RISC-V External Opportunities and Challenges

The external influences are crucial in determining whether RISC-V can succeed in the mobile phone area. This is because for RISC-V to be adopted widely, RISC-V needs to be strong enough to challenge ARM's dominance in the mobile phone field. In addition to RISC-V's internal properties and ecosystem, external competition with ARM and x86 is inevitable.

8.1 The Slowdown of Semiconductor Advances

In recent years, the physical limit of transistor technology has become closer. Moore's Law no longer holds, and the advance of semiconductors slows down [6]. However, this provides an opportunity for new ISA like RISC-V and the chips industry to catch up with the ARM and x86.

8.2 ARM's Dominance in The Mobile Phone Field

ARM is dominant in the mobile market, with robust software ecosystems with iOS, Android, comprehensive application software, and many patents [8]. The considerable R&D investment by leading enterprises like Apple continuously deepened its monopoly position [8]. Greengard [6] predicts that RISC-V will require enormous resources to rival proprietary ISA like ARM. Even with strong OS support for RISC-V, most apps today are designed for ARM-based phones, and the transition from RISC-V to ARM is also challenging [6].

Also, ARM has set up strategies against RISC-V. For example, it made the instruction set for its Cortex-M processors customisable in 2019 [6]. Customizability is considered one of RISC-V's critical advantages and attractive features to win ARM.

8.3 National and Industrial Enthusiasm

All Liu et al. [1], Mezger et al. [4], Greengard [6], Zhong [8], and Lu [9] agree with the high national industrial enthusiasm for RISC-V development. The RISC-V Foundation has attracted over 1,000 members from over 50 countries worldwide [8], which includes international giants such as Google, Intel, Qualcomm, and Alibaba [15]. The giant phone designer and manufacturer Samsung has made an announcement stating its adoption of RISC-V cores in its 5G smartphones [6]. The leading processor designer Qualcomm also announced to apply RISC-V into GPUs and solid-state drives (SSD) of mobile phones [6]. European Processor Initiative (EPI) is considering RISC-V as its primary solution for its embedded HPC platform.

9. SWOT Analysis

Strengths (Internal)	Weaknesses (Internal)
(1) Open-Source & Non-Proprietary: No high license fees; allows for commercial use, modification, and republication under the BSD License.	**(1) Fragmentation Issue:** Modularity allows for various implementations, making it difficult to standardise and hindering a unified OS.
(2) Modularity & Customisability: Designers can implement only necessary extensions, reducing complexity and allowing for domain-specific accelerators (AI/GPU).	**(2) Hardware Immaturity:** Limited availability of 64-bit high-performance general-purpose processors compared to the microcontroller class.
(3) Simplicity: Fewer instructions (47 basic) and a smaller specification document (~329 pages vs. 8000+ for ARM) reduce learning and execution costs.	**(3) Immature Software Ecosystem:** While basic tools exist, kernel support is limited and the application software layer for mobiles is in its early stages.
(4) Security Advantages: Openness allows for public transparency and verification; lacks speculative memory access vulnerabilities like Meltdown-Spectre.	**(4) Performance Gap:** Early high-performance chips like Xuantie-910 are roughly at the level of years-old ARM cores (Cortex-A73).

Opportunities (External)	Threats (External)
(1) National & Industrial Enthusiasm: Over 1,000 foundation members, including giants like Google, Samsung, and Qualcomm.	**(1) ARM's Market Dominance:** ARM holds a monopoly with a mature ecosystem (iOS/Android), extensive patents, and massive R&D investment.
(2) Official Android Support: Google's 2023 announcement to support RISC-V provides a critical software foundation for mobile adoption.	**(2) Competitive Response:** ARM has begun offering customisable instructions for its own cores to counter RISC-V's flexibility.
(3) Educational Pipeline: Growing use of RISC-V in university courses (e.g., Cambridge, Tsinghua) ensures a future workforce skilled in the architecture.	**(3) Supply Chain Barriers:** Limited availability of third-party secure hardware components and specialised mobile-grade GPUs.
(4) Slowdown of Moore's Law: The semiconductor advance slowdown allows new ISAs to catch up to incumbents like x86 and ARM.	**(4) Transition Costs:** Moving existing ARM-based apps to RISC-V is resource-intensive and technically challenging.

10. Conclusion

10.1 Overall Perspectives from the Literature

All Liu et al. [1], Cui et al. [2], Ince et al. [5], and Greengard [6] have estimated that RISC-V processors have a bright future. It is predicted that by 2025, RISC-C processors will occupy 6% of the processor market [6].

However, all of the estimations refer to the overall processor, which is not limited to phone processors, embedded processors, domain-specific processors, and many more. Zhong [8] argues that RISC-V processors will take a long time to enter traditional fields like desktops, servers, and mobile phones. Therefore, the future of RISC-V on mobile phones still needs a stronger conclusion.

10.2 Conclusion of the Literature Review

The literature articles have covered RISC-V's intrinsic properties, software ecosystem, hardware ecosystem, security, and other external opportunities and challenges. The three intrinsic properties, openness, modularity, and simplicity, also significantly affect the latter areas. The key findings that may impact the future of RISC-V architecture on mobile phones have been summarised in this literature review article. A few pieces of evidence were found to explicitly refer to the RISC-V adoption on mobiles, such as the performance comparison of the RISC-V processor XuanTie-910 capable of running Android and the announcement of Samsung using RISC-V cores in phones. And most sources are from a more general perspective, such as the fragmentation issue within RISC-V hardware and the opportunity to catch up with the slowdown of semiconductor technology, even though they are still highly relevant to the success of the mobile application of RISC-V.

This research aims to gather enough resources to make an objective prediction on the prospect of RISC-V in the mobile phone area. This can fill the research gap in exploring the connection between RISC-V and mobile phones. The literature review has found many articles helpful in the prediction, but they are mostly general and cannot answer my research question more rigorously. Therefore, the next stage is to focus on more specific resources about RISC-V and mobile phones and not be limited to literature articles, such as news articles, industrial reports, and summits, surveys.

In addition, some important evidence that may significantly contribute to the research of my topic is missing in the literature articles. They include the performance comparison between current and physical RISC-V processes for mobile phones and the survey on industrial willingness to develop RISC-V-based phone apps when the RISC-V mobile phone platform, such as Android, is established. These points can be discovered through primary research in the future.

Throughout the literature review, debates can be found in some areas. For example, its open architecture brings both advantages and challenges to security. Therefore, conducting further research in this domain is valuable to provide deeper insights and understanding.

Overall, this literature review summarises the existing knowledge about the future of RISC-V mobile phones and identifies the needs and possible research directions for my research topic.

11. Bibliography

11.1 Journal Articles and Conference Proceedings

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