Proyecto Final - Circuitos Analogicos 2024-II

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Full Adder - Truth Table

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder Truth Table

Full Adder - Boolean Algebra

$$S = \overline{A}\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\overline{C_{in}} + ABC_{cin}$$

$$C_{out} = \overline{A}BC_{in} + A\overline{B}C_{in} + AB\overline{C_{in}} + ABC_{in}$$

Full Adder - Implementation

Takes 108 transistors.

$$S = \overline{A}\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\overline{C_{in}} + ABC_{cin}$$

Takes only 18 transistors (9 transistors by **XOR**).

$$\begin{aligned}
S &= \overline{A}\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\overline{C_{in}} + ABC_{in} && (1)\\
&= C_{in}\left[\overline{A}\overline{B} + AB\right] + A\overline{B}\overline{C_{in}} + \overline{A}B\overline{C_{in}} && (2)\\
&= C_{in}\left[(\overline{A} + B)(A + \overline{B})\right] + \overline{C_{in}}(A\overline{B} + \overline{A}B) && (3)\\
&= C_{in}\left[\overline{A\overline{B}}\,\overline{\overline{A}B}\right] + \overline{C_{in}}(A\overline{B} + \overline{A}B) && (4)\\
&= C_{in}\overline{(A\overline{B} + \overline{A}B)} + \overline{C_{in}}(A\overline{B} + \overline{A}B) && (5)\\
&= C_{in} \oplus \left[A\overline{B} + \overline{A}B\right] && (6)\\
&= C_{in} \oplus (A \oplus B) && (7)
\end{aligned}$$

Full Adder - Implementation

Initial expression extracted from Truth Table.

$$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$$

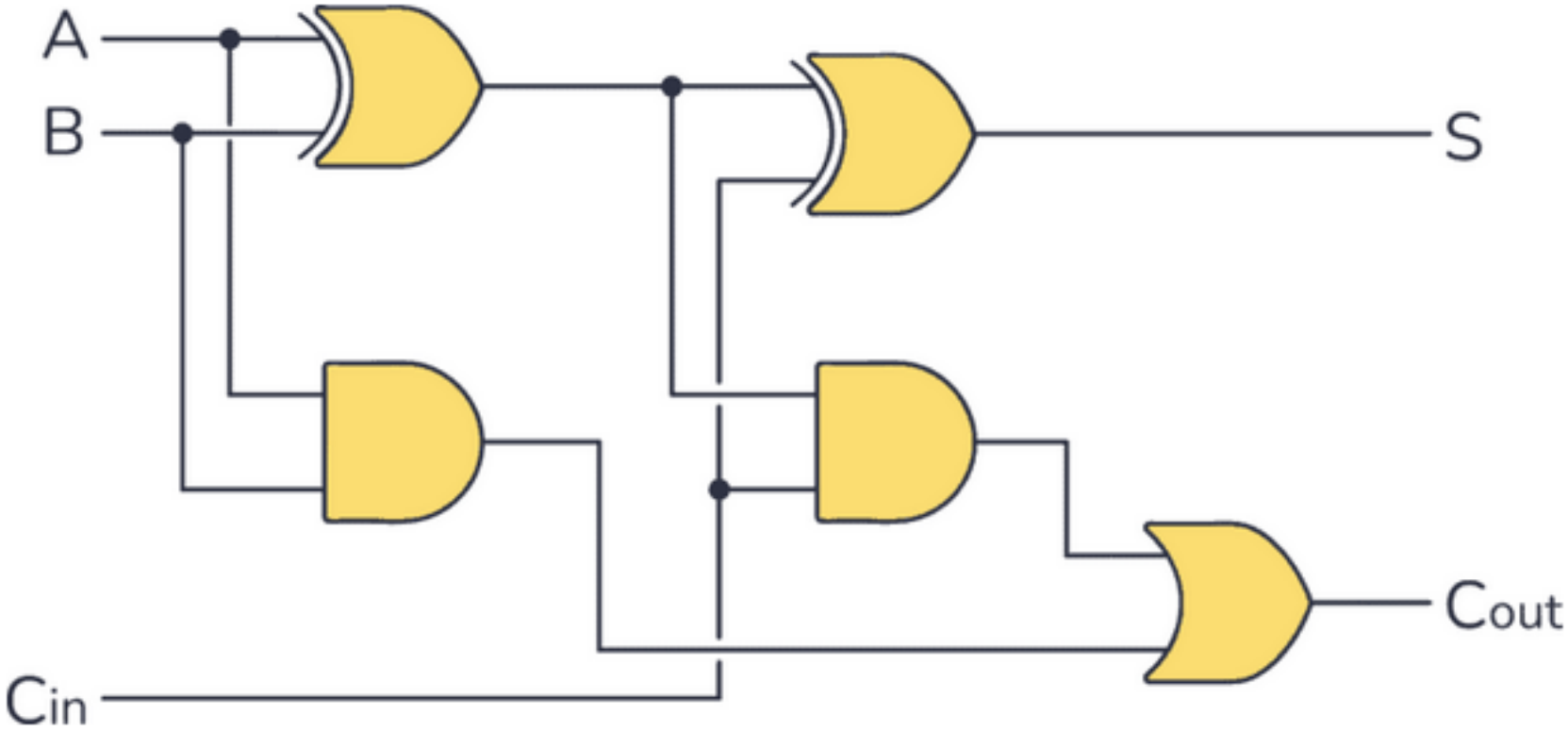
Reducer with *Karnaugh Map*[2].

$$C_{out} = AB + BC_{in} + AC_{in}$$

$$\begin{aligned} C_{out} &= \bar{A}BC_{in} + A\bar{B}C_{in} + AB\overline{C_{in}} + ABC_{in} && (8)\\ &= C_{in}(\bar{A}B + A\bar{B}) + AB(C_{in} + \overline{C_{in}}) && (9)\\ &= C_{in}(\bar{A}B + A\bar{B}) + AB && (10)\\ &= AB + C_{in}(A \oplus B) && (11) \end{aligned}$$

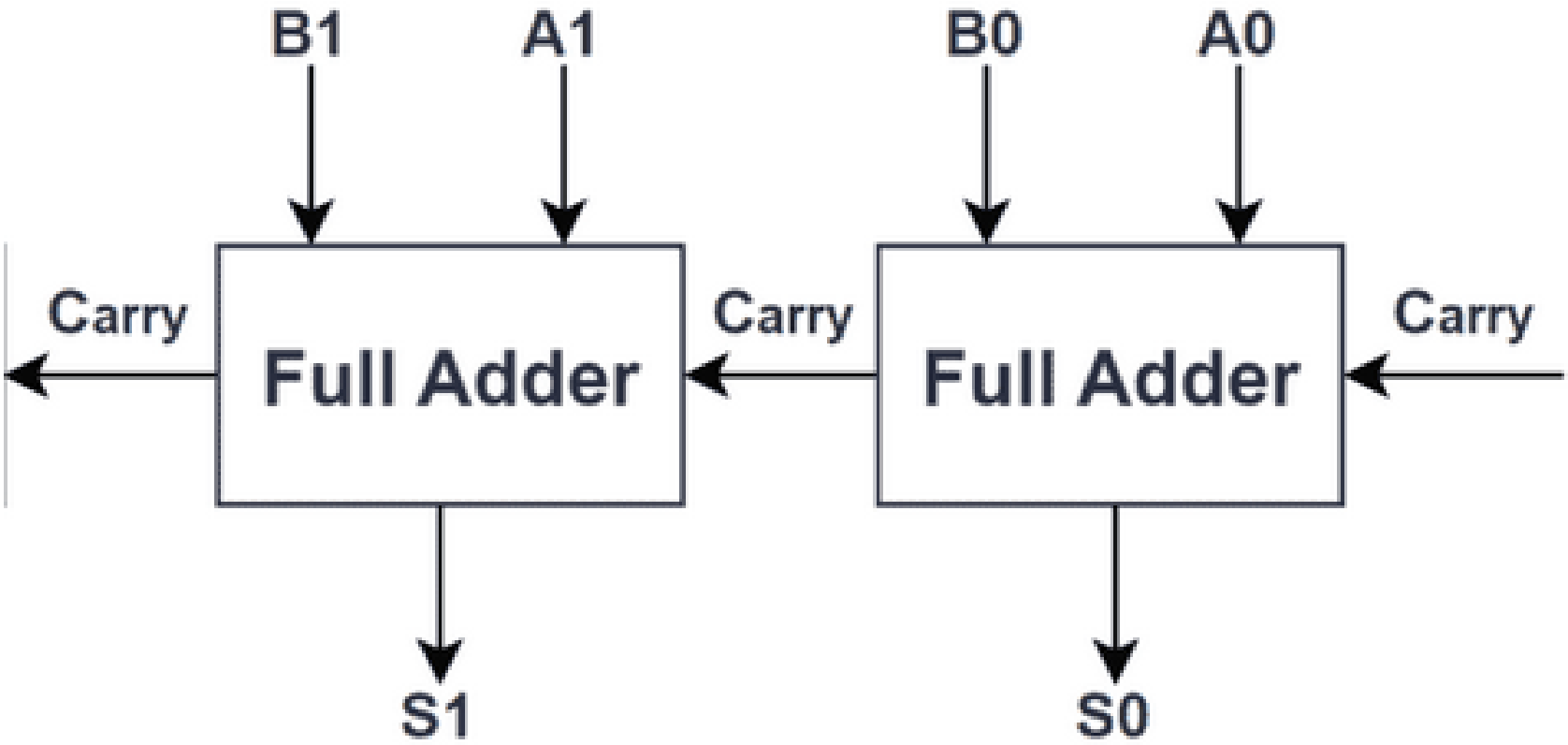
In this expression we need 2 **AND** gate, 1 **OR** gate and 1 **XOR** (that we can **reuse** from S expression).**XOR**).

Full Adder - Logical Gates Circuit



A Full Adder Circuit

Two Bit Adder



MOSFET - Inversion Layer

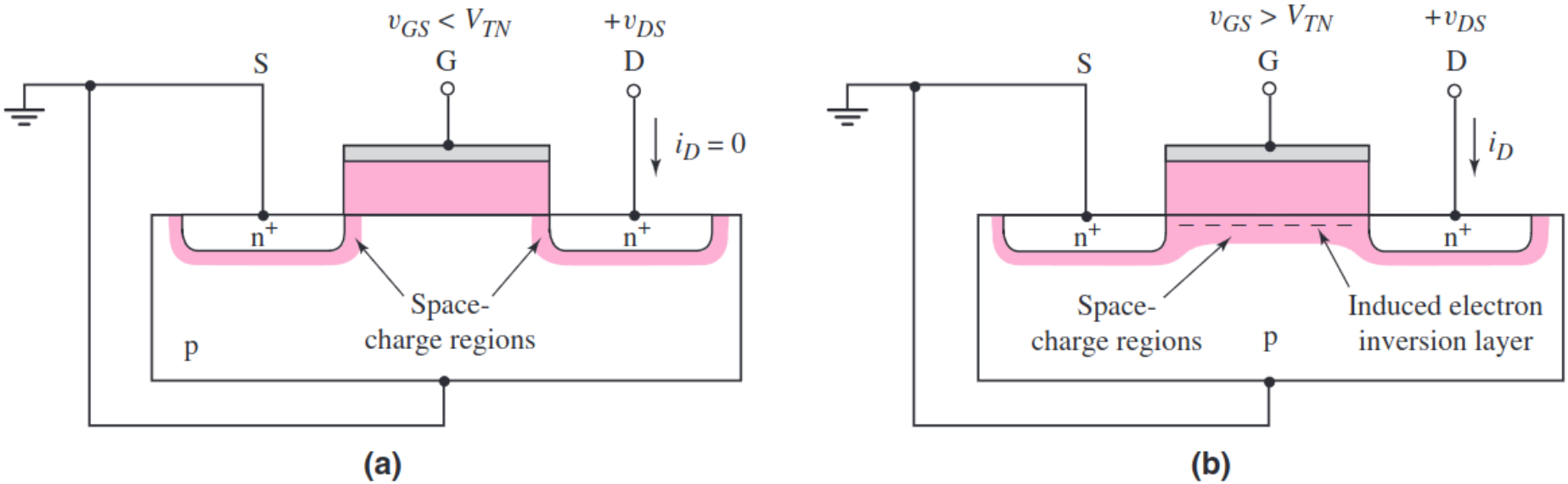


Figure 3.7 The n-channel enhancement-mode MOSFET (a) with an applied gate voltage $v_{GS} < V_{TN}$, and (b) with an applied gate voltage $v_{GS} > V_{TN}$

MOSFET - Characteristic Curves

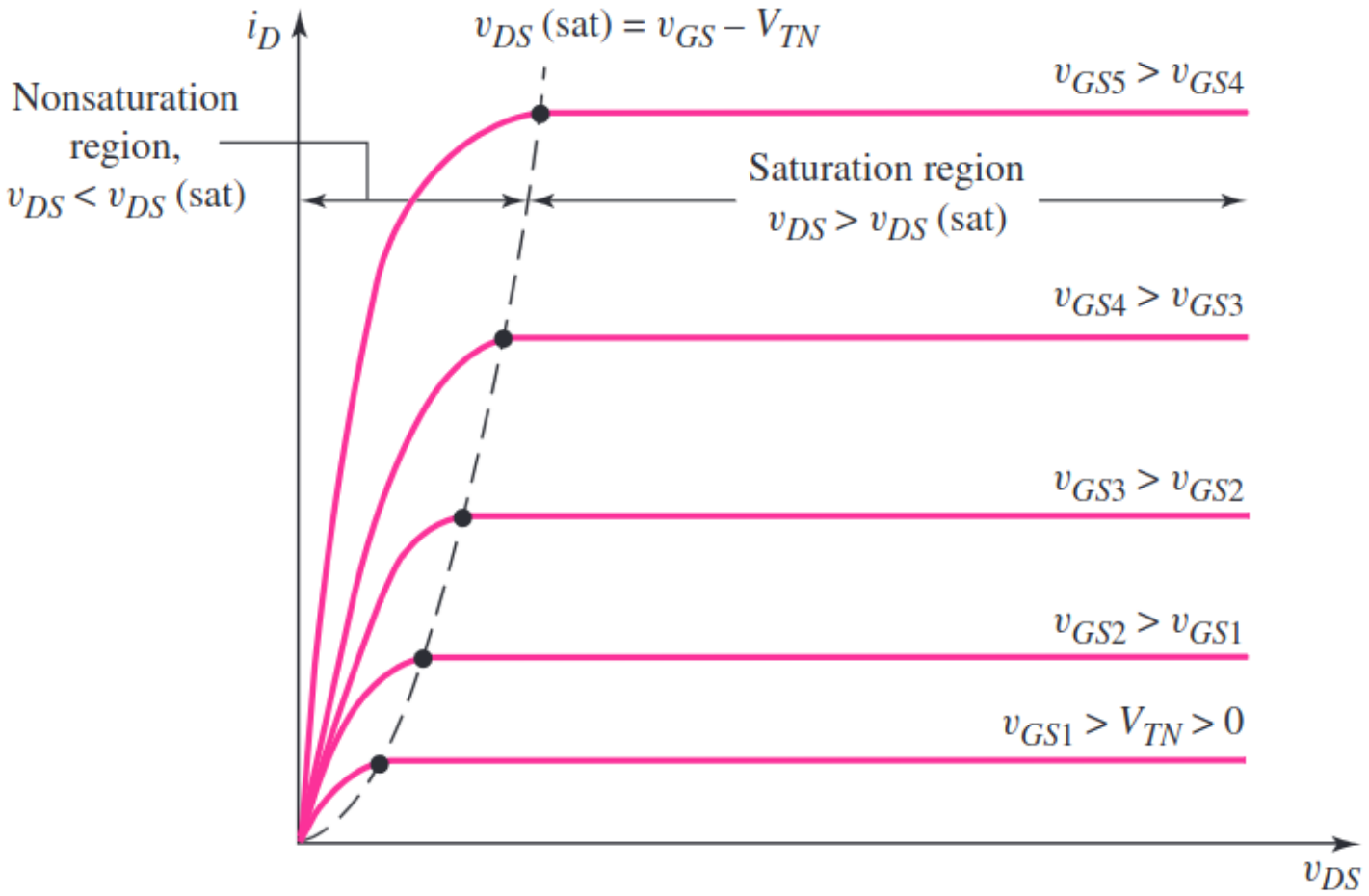


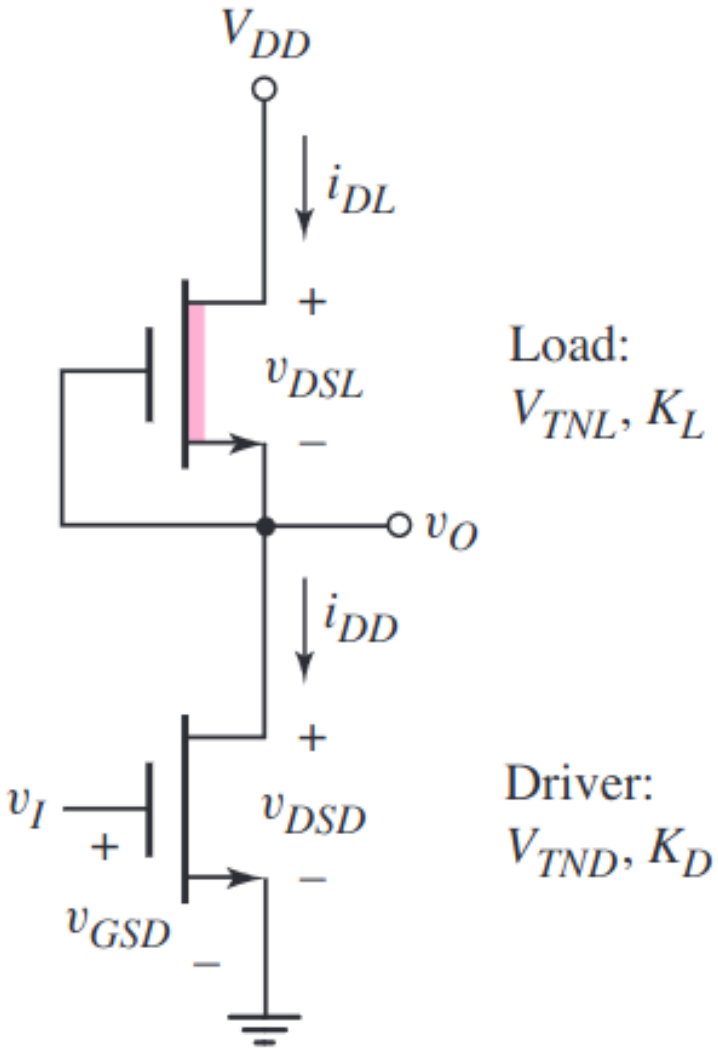
Figure 3.10 Family of i_D versus v_{DS} curves for an n-channel enhancement-mode MOSFET.

MOSFET - Equations

Table 3.1 Summary of the MOSFET current–voltage relationships

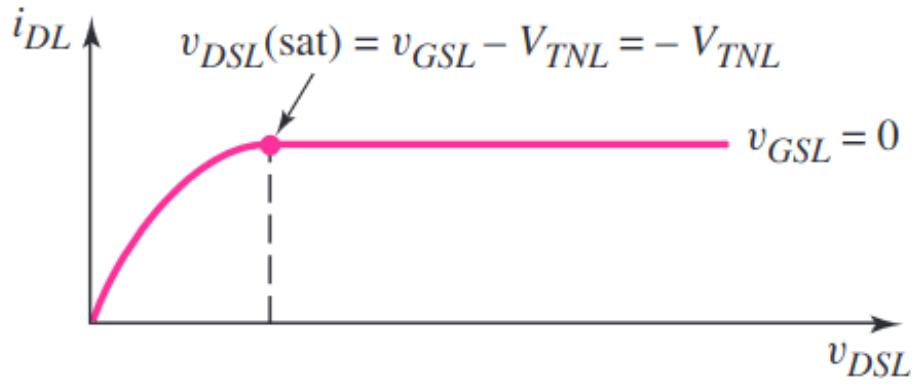
NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

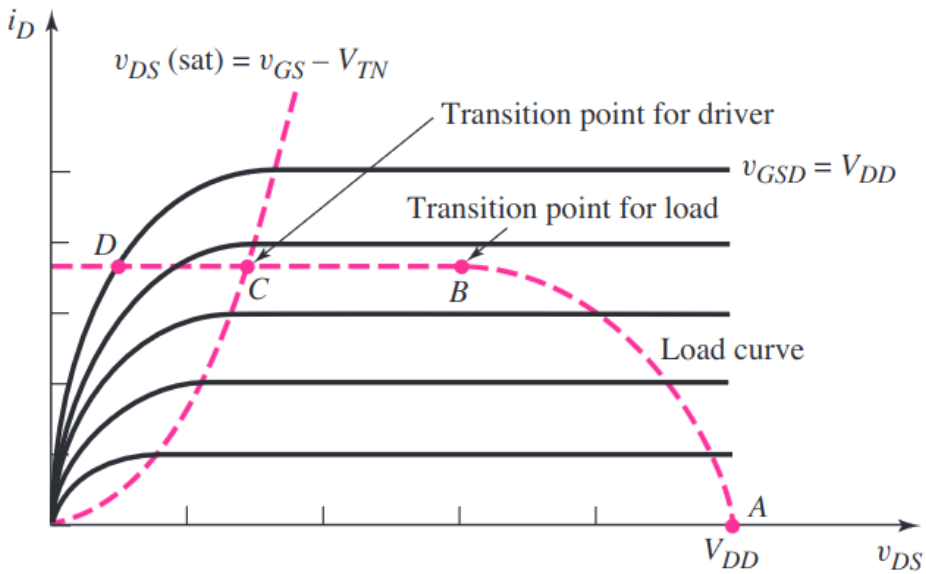
Logic gates - MOSFET Inverter



Load:
V_{TNL}, K_L

Driver:
V_{TND}, K_D





Logic gates - MOSFET Inverter - Transition Points

LOAD

$$v_{DSL} = V_{DD} - v_o = v_{GSL} - V_{TNL} = -V_{TNL}$$

Therefore, one transition point (LOAD) is at:

$$v_o = V_{DD} + V_{TNL}$$

DRIVER

$$v_{DSD} = v_o = V_{GSD} - V_{TND} = v_i - V_{TND}$$

Therefore, the other transition point (DRIVER) is at:

$$v_o = v_i - V_{TND}$$

Logic gates - MOSFET Inverter - Operation

- **load** nonsaturation and **driver** saturation (Q-point on A and B)

$$K_D[-V_{TND}]^2 = K_L[2(v_i - V_{TND})v_o - v_o^2]$$

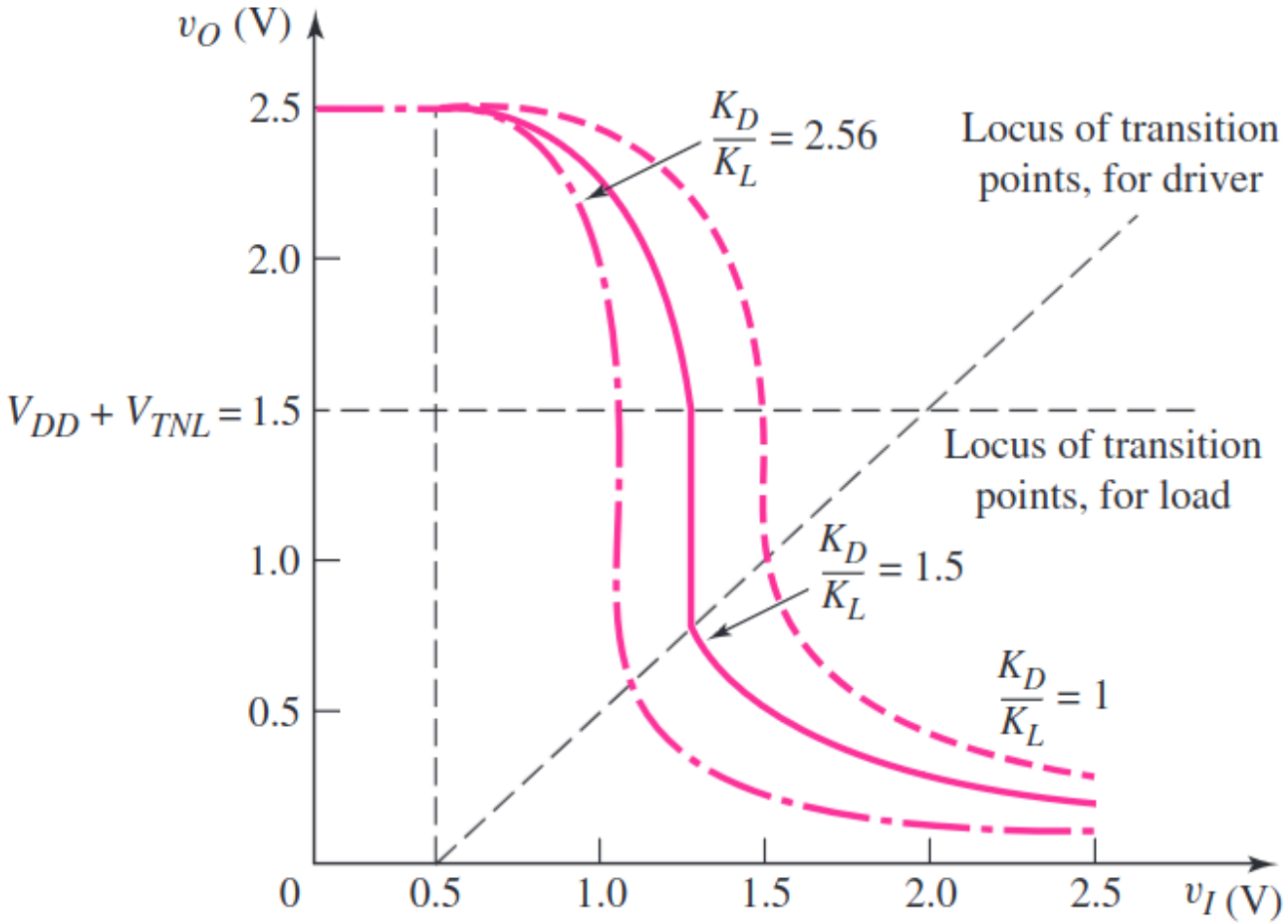
- **load** and **driver** on saturation (Q-point on B and C)

$$K_D[v_i - V_{TND}]^2 = K_L[(V_{DD} - v_o) - V_{TNL}]^2$$

- **load** saturation and **driver** nonsaturation (Q-point on C and D)

$$K_D[v_i - V_{TND}]^2 = K_L[2(-V_{TND})(V_{DD} - v_o) - (V_{DD} - v_o)^2]$$

Logic gates - MOSFETS - Inverter



Logic gates - MOSFETS - NOR

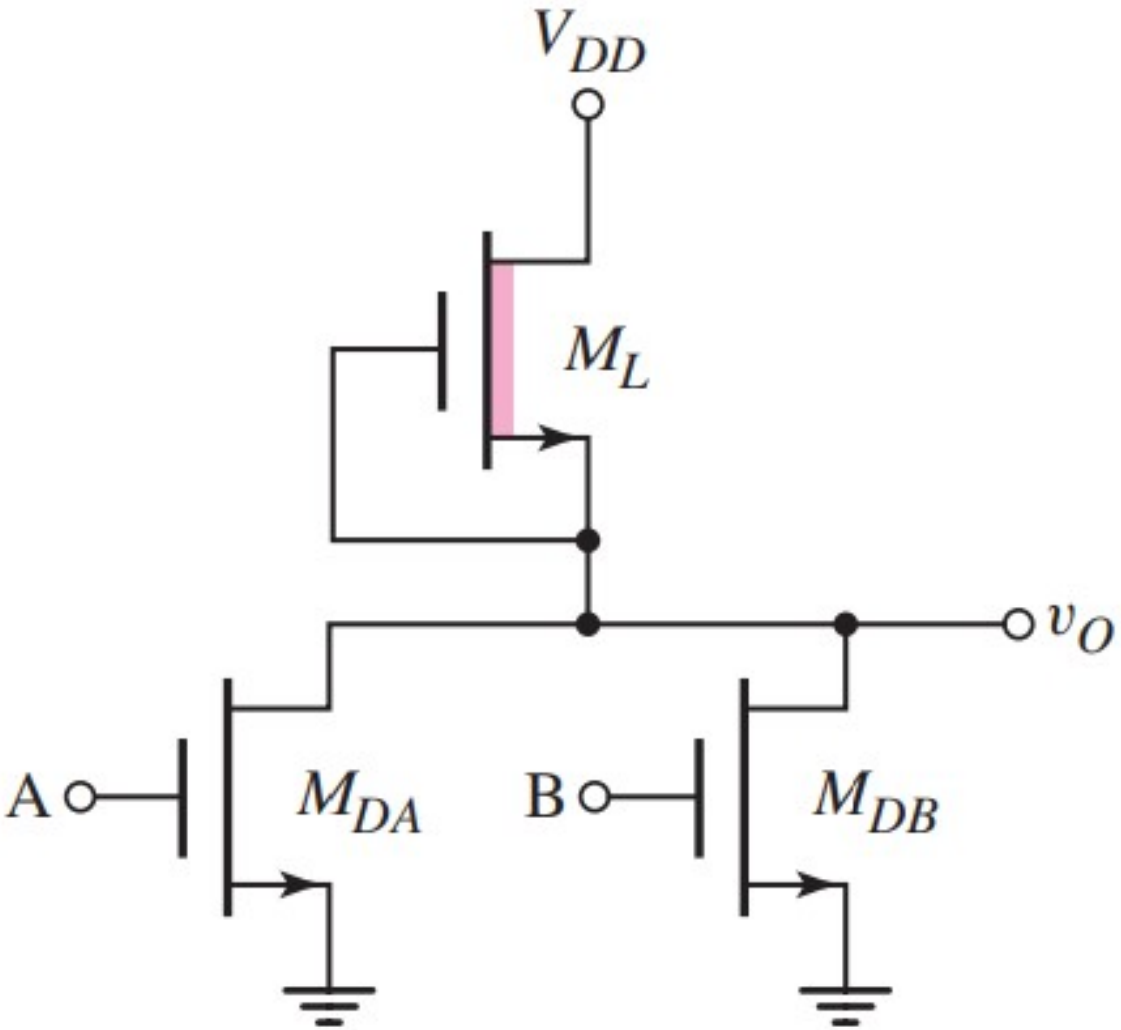


Tabla de verdad

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Logic gates - MOSFETS - NAND

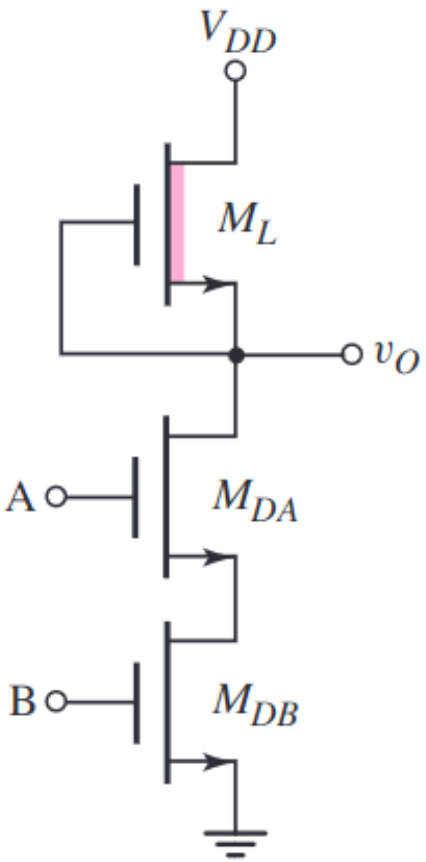


Tabla de verdad

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Logic gates - MOSFETS - XOR

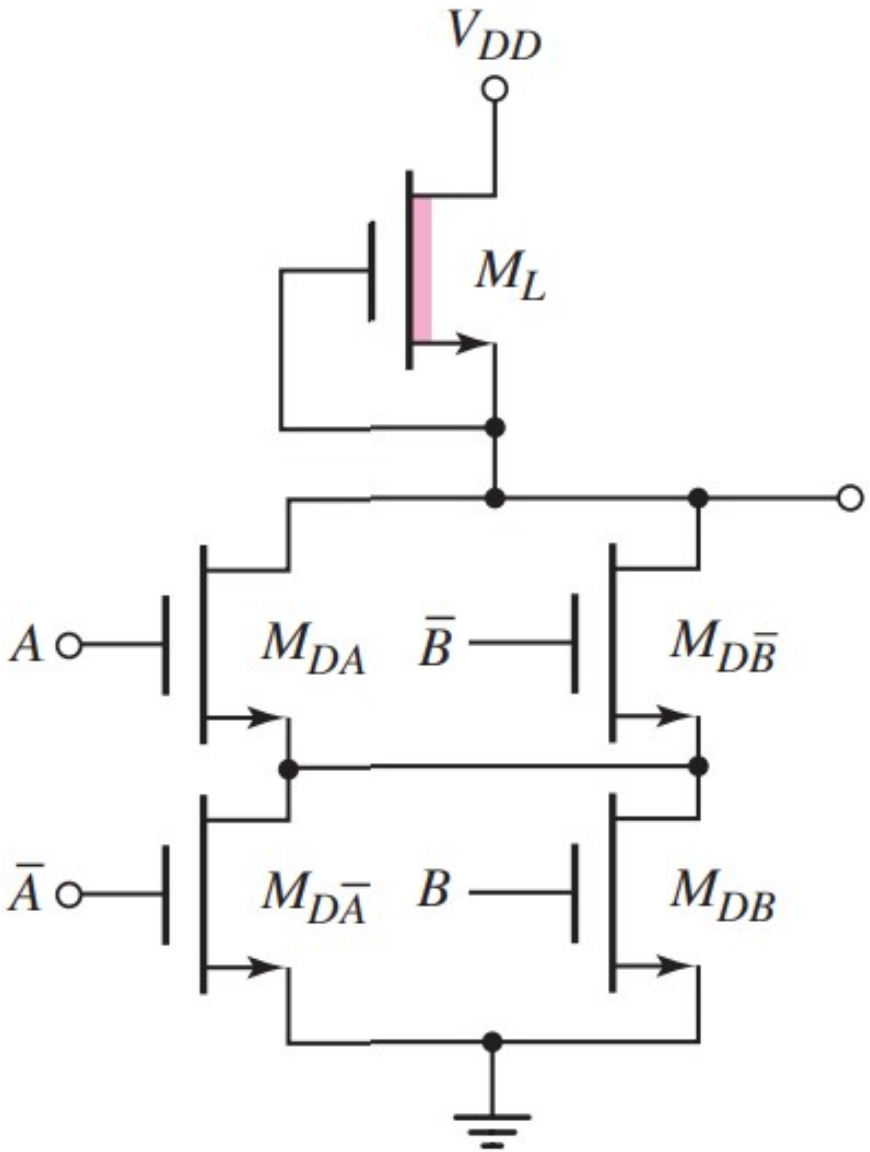
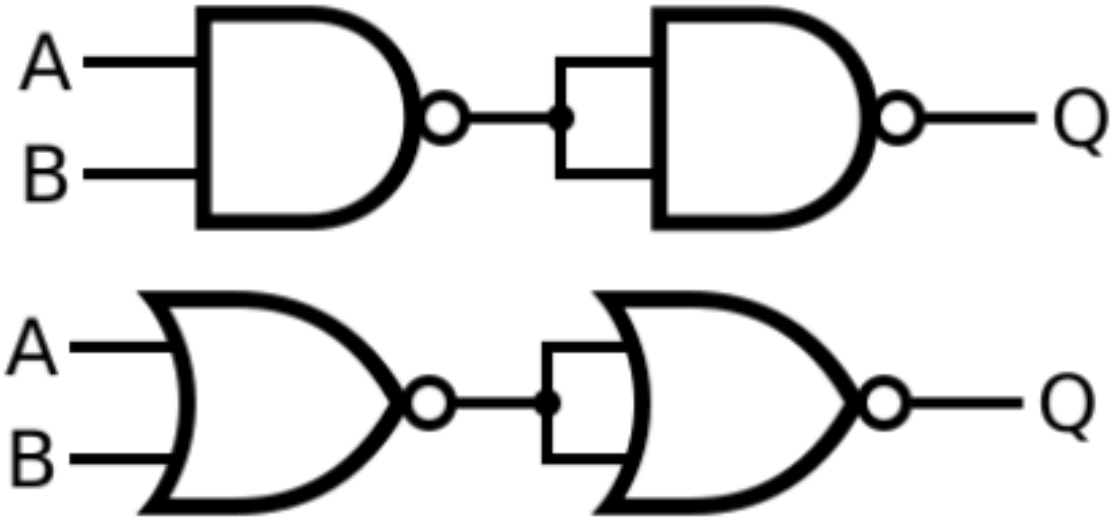


Tabla de verdad

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

Logic gates - MOSFETS - AND and OR



Inversor

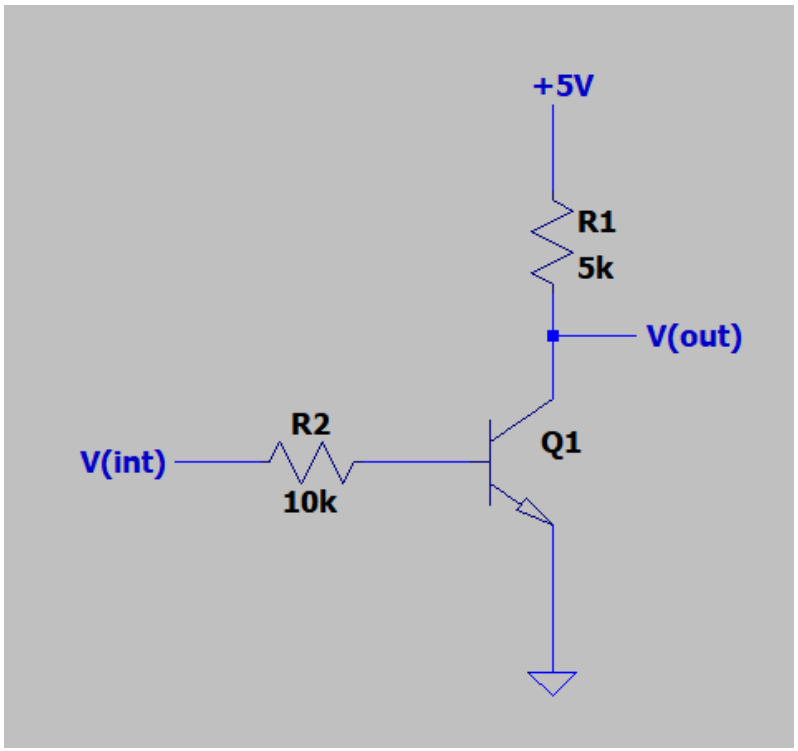


Tabla de verdad

A	$\overline{A}$
0	1
1	0

Puerto OR

Circuito OR

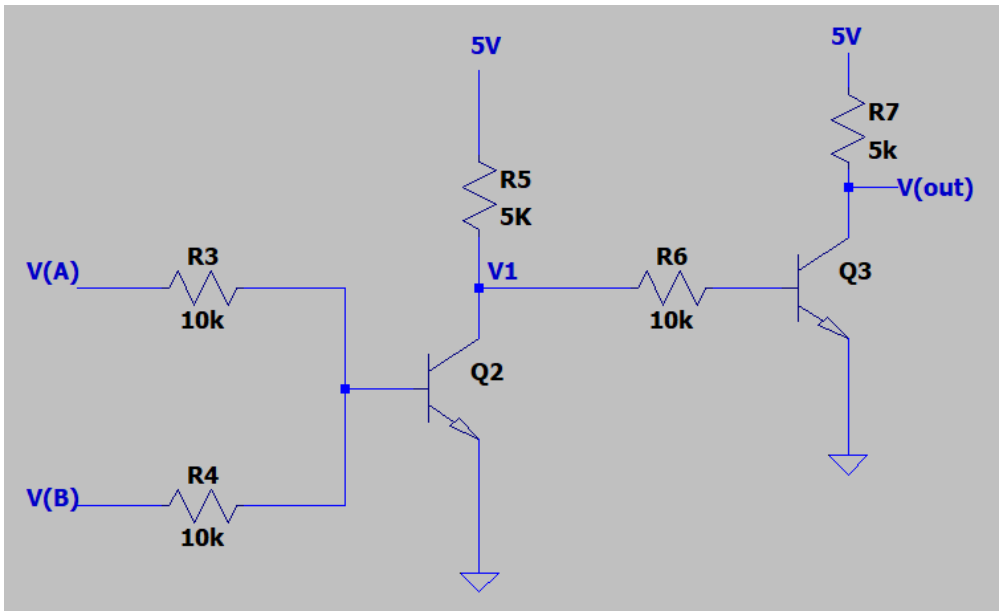
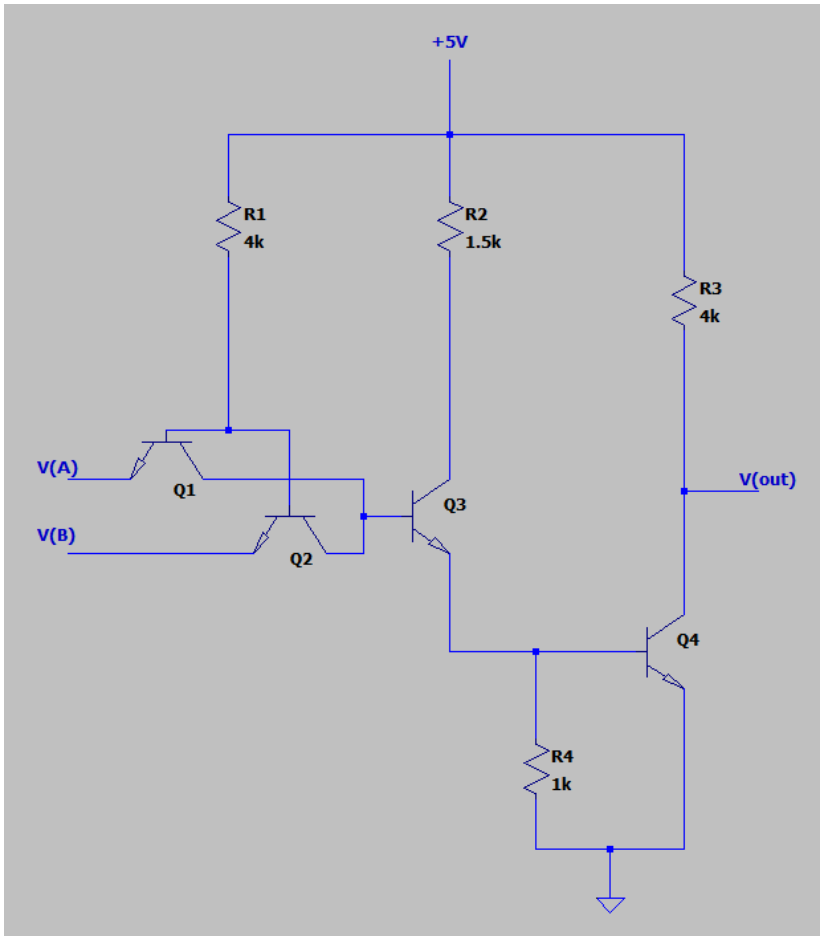


Tabla de verdad

A	B	$A + B$
0	0	0
1	0	1
0	1	1
1	1	1

Puerto AND

Circuito NAND



Circuito equivalente del AND

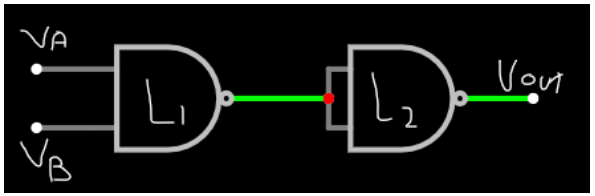
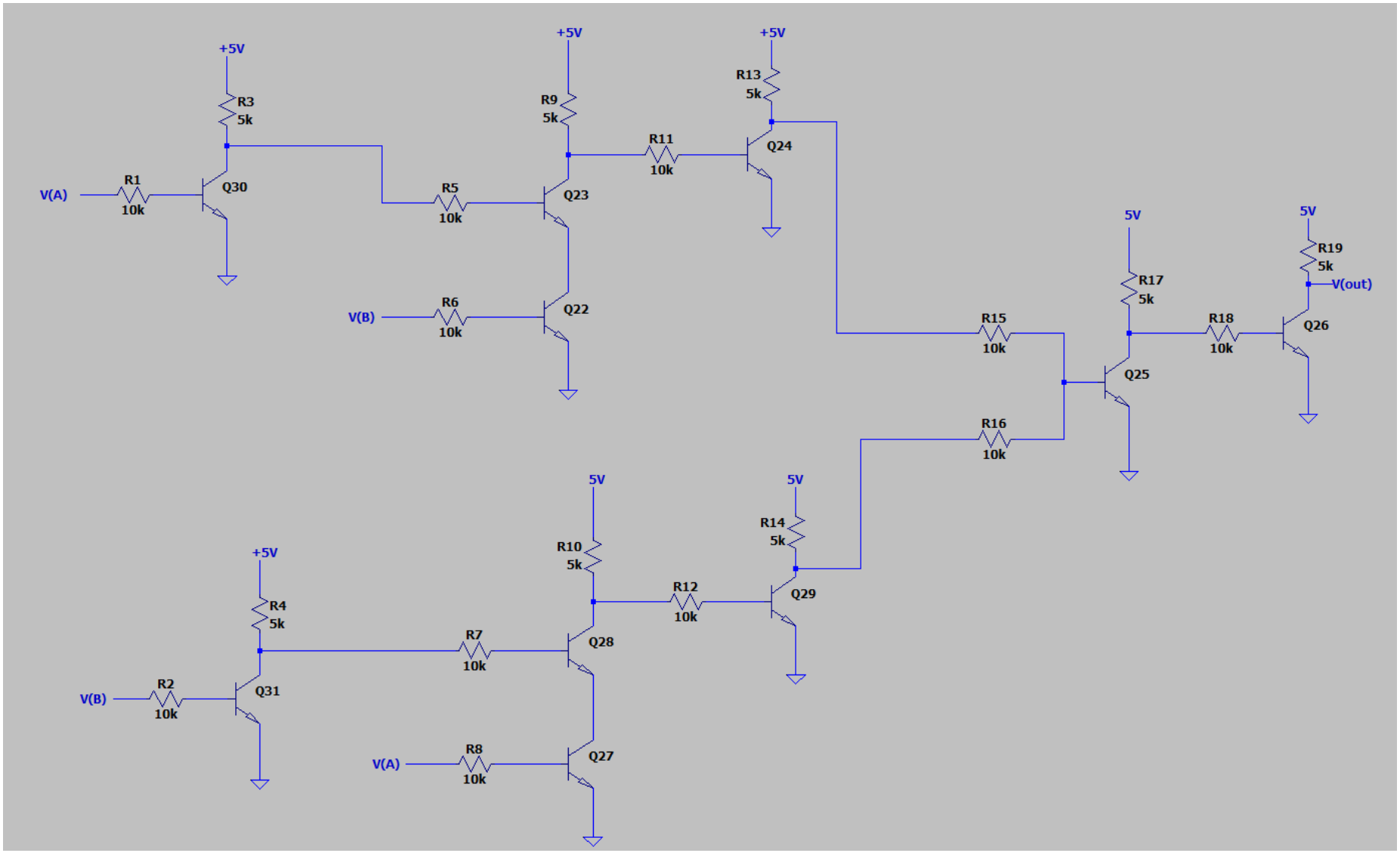


Tabla de verdad

A	B	$A \cdot B$
0	0	0
1	0	0
0	1	0
1	1	1

Puerto XOR


+5V
R3
5k
R1
10k
V(A)
Q30
R5
10k
+5V
R9
5k
Q23
R11
10k
+5V
R13
5k
Q24
V(B)
R6
10k
Q22
R15
10k
5V
R17
5k
R18
10k
5V
R19
5k
V(out)
Q26
Q25
R16
10k
5V
R10
5k
5V
R14
5k
+5V
R4
5k
R12
10k
Q29
R7
10k
Q28
V(B)
R2
10k
Q31
V(A)
R8
10k
Q27

Puerto XOR

Tabla de verdad

A	B	$A \oplus B$
0	0	0
1	0	1
0	1	1
1	1	0

Observaciones

- Al utilizar interruptores de un solo sentido en cada pin de entrada, si el interruptor estaba abierto, el voltaje obtenia cualquier valor. Esto se corrigió usando de dos vías, esto permitía definir correctamente el 0 y 1.
- Dado que no se pudo obtener un n-channel depletion mode, se reemplazó por una resistencia de menor valor posible para no afectar el 1 lógico; y evitar dañar la fuente de alimentación.

Conclusiones

- Ambos *Full adder* presentaron un correcto funcionamiento, se creó *2 bits adder* usando MOSFET y BJT.

References

Images and circuits were extracted from [3][4][1].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