UNIVERSIDAD NACIONAL DE INGENIERÍA

FACULTAD DE CIENCIAS

Proyecto Final: Full Adder

Circuitos Electrónicos Analógicos CF3E1A

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Ciclo 2024-1

1 Fundamento teórico

1.1 Mosfet

1.1.1 MOS Capacitor

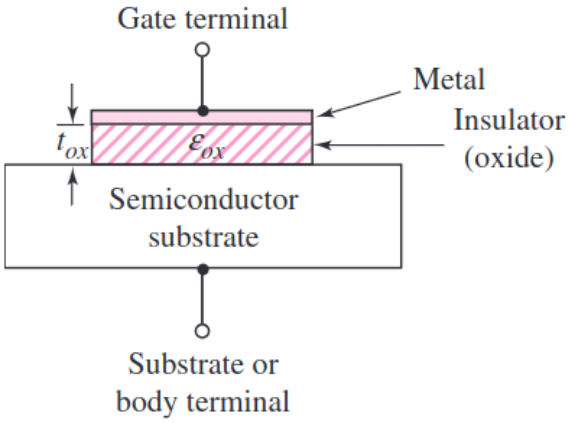

Figure 3.1 The basic MOS capacitor structure

Figure 1: MOS Capacitor

1.1.2 Inducted inversion layer

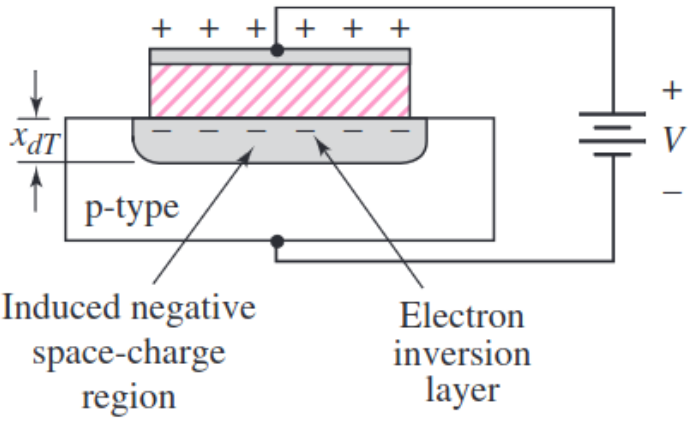

Figure 2: Inducted Inversion Layer

The current in a MOSFET is the result of the flow of charge in the inversion layer, also called the channel region, adjacent to the oxide–semiconductor interface.

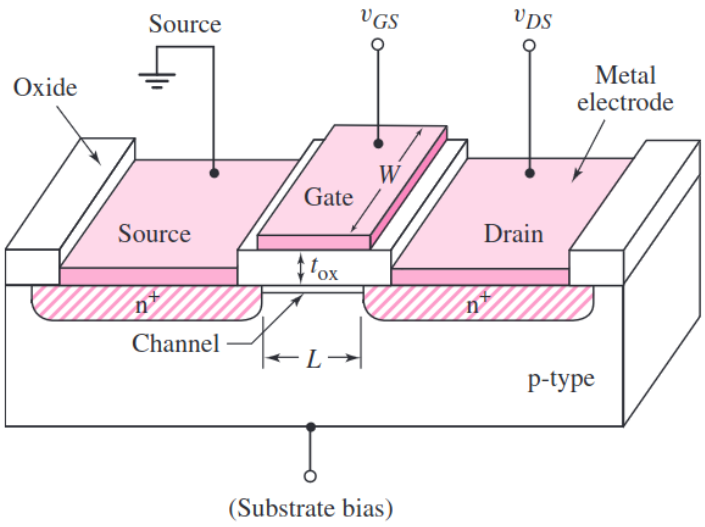

Figure 3: Mosfet Structure

2 Full Adder

2.1 Truth Table

We want to build a circuit that given the bits A, B and a *carrier* (C_{in}) computes $SUM = A + B$ (in table S is the less significant bit of SUM and C_{out} the more significant one) (Figure 4)

2.2 Boolean Algebra

From the truth table we can derive (**SOP**: Sum of Products). The following expression for S.

$$S = \overline{A}\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\overline{C_{in}} + ABC_{cin}$$

Using **Karnaugh Map**[1] (Figure 5) to reduce the expression of S.

We can notice that this expression is the more simplified one. But this is the more cost-efficient way of implement this circuit. Let's count the number of transistors that should be used to build it (taking as reference the implementation with **NMOS** technology - Circuits 11, 17, 15, 16 - Extracted from [3][2]).

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder Truth Table

Figure 4: Full Adder - Truth Table

$\overline{A}\overline{B}C_{in}$ 2 **inverters** (2 transistors by inverter), 2 **AND** gates (2 **NAND** gates, where we need 3 transitors by *NAND* gate), 2 **OR** gates (2 **NOR** gates, where we need 3 transistors by *NOR* gate)

```
transistors = 0

x = 2*2 + 2*2*3 + 2*2*3
transistors += x

x = 28
transistors = 28
```

$\overline{A}B\overline{C_{in}}$ 2 **inverters** (2 transistors by inverter), 2 **AND** gates (2 **NAND** gates, where we need 3 transitors by *NAND* gate), 2 **OR** gates (2 **NOR** gates, where we need 3 transistors by *NOR* gate)

```
transistors = 28

x = 2*2 + 2*2*3 + 2*2*3
transistors += x

x = 28
transistors = 56
```

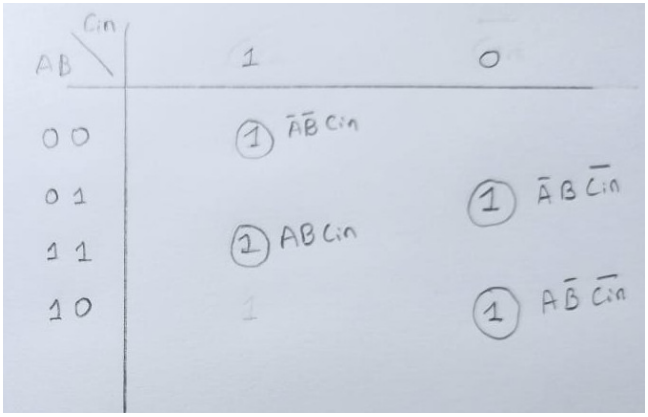

Figure 5: Karnaugh Map - S expression

$A\overline{B}\overline{C_{in}}$ 2 **inverters** (2 transistors by inverter), 2 **AND** gates (2 **NAND** gates, where we need 3 transitors by *NAND* gate), 2 **OR** gates (2 **NOR** gates, where we need 3 transistors by *NOR* gate)

```
transistors = 56

x = 2*2 + 2*2*3 + 2*2*3
transistors += x

x = 28
transistors = 84
```

ABC_{cin} 2 **AND** gates (2 **NAND** gates, where we need 3 transitors by *NAND* gate), 2 **OR** gates (2 **NOR** gates, where we need 3 transistors by *NOR* gate)

```
transistors = 84

x = 2*2*3 + 2*2*3
transistors += x

x = 24
transistors = 108
```

If well this expression is the more reduced one, it is not practical for implementation. Let's try to find a more compact expression that reduce the number of transistors.

$$
\begin{aligned}
S &= \overline{A}\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\overline{C_{in}} + ABC_{in} && (1)\\
&= C_{in}\left[\overline{A}\overline{B} + AB\right] + A\overline{B}\overline{C_{in}} + \overline{A}B\overline{C_{in}} && (2)\\
&= C_{in}\left[(\overline{A} + B)(A + \overline{B})\right] + \overline{C_{in}}(A\overline{B} + \overline{A}B) && (3)\\
&= C_{in}\left[\overline{A\overline{B}}\,\overline{\overline{A}B}\right] + \overline{C_{in}}(A\overline{B} + \overline{A}B) && (4)\\
&= C_{in}\overline{(A\overline{B} + \overline{A}B)} + \overline{C_{in}}(A\overline{B} + \overline{A}B) && (5)\\
&= C_{in} \oplus \left[A\overline{B} + \overline{A}B\right] && (6)\\
&= C_{in} \oplus (A \oplus B) && (7)
\end{aligned}
$$

Now, let's count the number of transistor used to implement this expression.

$A \oplus B$ 2 **inverters** (2 transistors by inverter) and 5 transistors by **XOR** gate.

```
transistors = 0

x = 2*2 + 5
# we are going to use 'x' transistors on A XOR B
# and other 'x' transistors on C_in XOR (A XOR B)
transistors += 2*x

x = 9
transistors = 18
```

Similarly, let's find the more suitable expression for C_{out}. From the truth table, we have this initial expression:

$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + ABC_{in} + ABC_{in}$

Let's use **Karnaugh Map** to reduce the below expression.

From *Karnaugh Map* we have the following reduced expression:

$$C_{out} = AB + BC_{in} + AC_{in}$$

To implement this expression we need 3 **AND** gates and 2 **OR** gates.

Let's try to find a more optimal expression to implement C_{out}

$$
\begin{aligned}
C_{out} &= \overline{A}BC_{in} + A\overline{B}C_{in} + AB\overline{C_{in}} + ABC_{in} && (8)\\
&= C_{in}(\overline{A}B + A\overline{B}) + AB(C_{in} + \overline{C_{in}}) && (9)\\
&= C_{in}(\overline{A}B + A\overline{B}) + AB && (10)\\
&= AB + C_{in}(A \oplus B) && (11)
\end{aligned}
$$

In this expression we need 2 **AND** gate, 1 **OR** gate and 1 **XOR** (that we can **reuse** from S expression).

Therefore we only need 2 **AND** gate, 1 **OR** gate (1 less **AND** gate and 1 less **OR** gate that the expression extracted from *Karnaugh Map*).

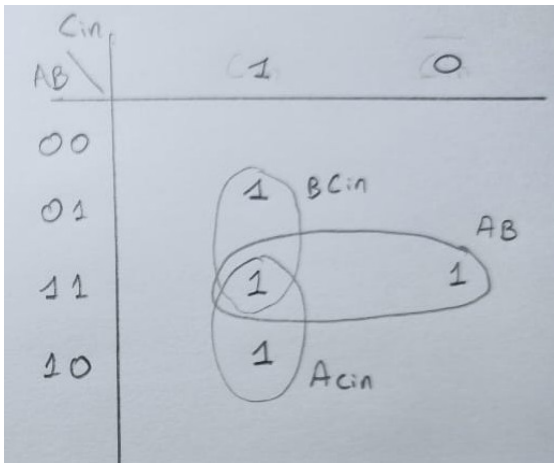

Figure 6: Karnaugh Map - C_{out} expression

2.3 Logical Gates Circuit

From the derived expressions our *full-adder* circuit (in term of logical gates) is show in the following diagram (Figure 7):

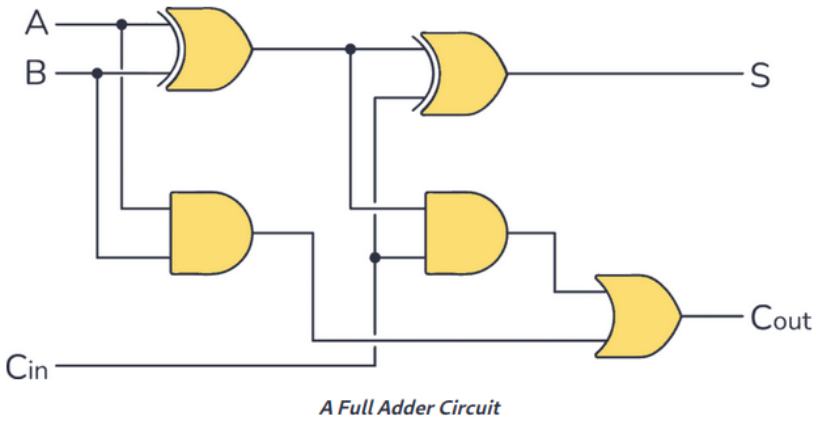

Figure 7: Full Adder - Logical Gates Circuit

2.4 Two Bits Adder

How can I add more than *one bit*?

Well, just chain together several *Full Adders* and make the first **carry = 0**. For example a 2-bits adder looks like this (Figure 8):

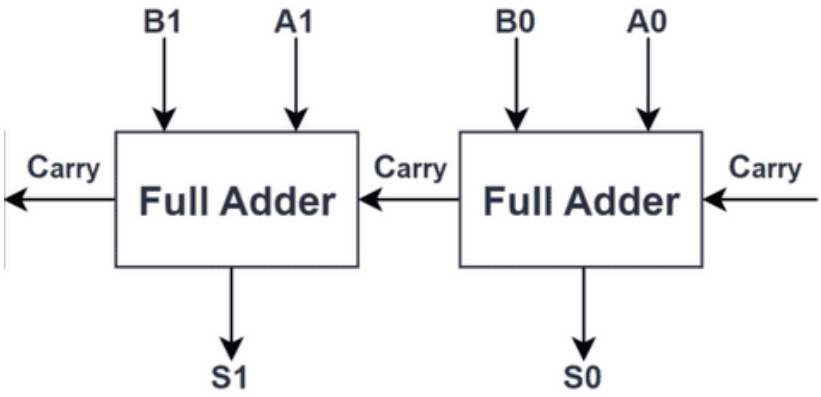

Figure 8: Full Adder - Logical Gates Circuit

3 How does a Logical Gate is build?

They are build from *fundamental* gates like **NOR** or **NAND** that are build using transistors (MOSFTER or BJT) or directly using transistors like the *fundamental* ones.

- **AND** Logical Gate (based on **NAND** gates) (Figure 9)

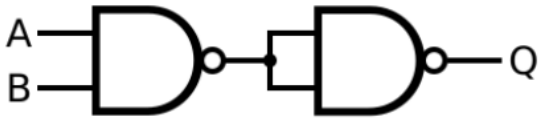

Figure 9: **AND** from **NAND** gates

- **OR** Gate (based on **NOR** gates) (Figure 10)

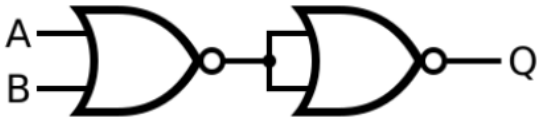

Figure 10: **OR** from **NOR** gates

4 Logic gates - MOSFETS

4.1 Inverter

Since **XOR** gate needs inverted signals. We are going to build **inverter** gates. In specific we are going to build an *NMOS Inverter with Depletion Load*, show in Figure 11:

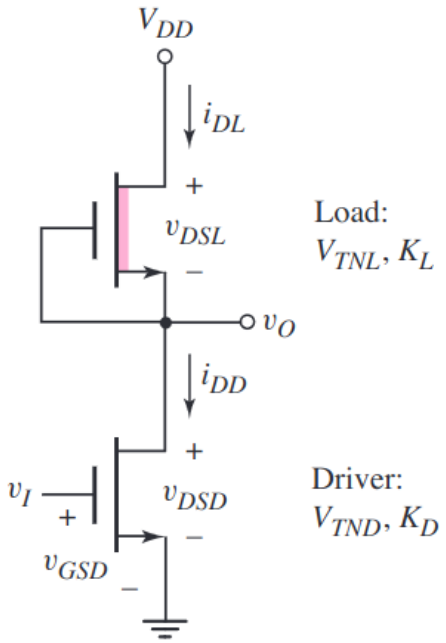

Figure 11: **Inverter** gate NMOS

4.1.1 Analysis

When the inverter input is less than the driver threshold voltage, the driver is cut off and the drain currents are zero. From Figure 12, we see that for $i_D = 0$, the V_{DSL} must be zero. Therefore $v_o = V_{DD}$ for $v_i \leq V_{TND}$.

Before start analyzing, when $v_i > V_{TND}$. We need to know where the transition points (driver and load) are to know in which region each MOSFET is operating.

LOAD

$$v_{DSL} = V_{DD} - v_o = v_{GSL} - V_{TNL} = -V_{TNL}$$

Therefore, one transition point (LOAD) is at:

$$v_o = V_{DD} + V_{TNL}$$

DRIVER

$$v_{DSD} = v_o = V_{GSD} - V_{TND} = v_i - V_{TND}$$

Therefore, the other transition point (DRIVER) is at:

$$v_o = v_i - V_{TND}$$

Given that $v_o = V_{DSD}$ and $v_i \leq V_{DD}$, then the transition point of the load is further to the right than driver transition point (As show in Figure 12)

Now if the input voltage becomes just greater than the driver threshold voltage V_{TND}, let's say:

$$v_i = V_{TND} + \delta$$

Then the channel of the enhancement-mode mosfet (driver) is subtly open and therefore is on saturation mode. And the current on the channel is:

$$i_{DD} = K_D[V_{GS} - V_{TND}]^2 = K_D[(V_{TND} + \delta) - V_{TND}] = K_D\delta^2$$

Let's suppose that **load** is on saturation mode. Then, since $i_{DD} = i_{DL}$.

$$\begin{aligned} i_{DL} &= K_L[v_{GSL} - V_{TNL}]^2 && (12)\\ &= K_L(-V_{TNL})^2 && (13)\\ &= K_L V_{TNL}^2 && (14) \end{aligned}$$

Which is a contradiction, since i_{DL} is variable and $K_L V_{TNL}^2$ is an static value.

Therefore the **load** is on nonsaturation mode.

Given that $i_{DD} = i_{DL}$, Then we have the following relation:

$$K_D[v_{GSD} - V_{TND}]^2 = K_L[2(v_{GSL} - V_{TND})v_{DSL} - v_{DSL}^2] \qquad (15)$$

Given that $v_i = v_{GSD}$ and $v_o = V_{DD} - v_{DSL}$. Then, replacing these expression on eq.15. We have the following one:

$$K_D[v_i - V_{TND}]^2 = K_L[2(-V_{TND})(V_{DD} - v_o) - (V_{DD} - v_o)^2]$$

This expression is true only when **driver** is on saturation mode and **load** is on non-saturation mode (Q-point lies between points A and B on Figure 12 - first nonlinear portion of graph on Figure 14).

When Q-point lies between points B and C. The **load** and **driver** are now on saturation mode. Therefore since $i_{DD} = i_{DL}$. We have the following relation:

$$K_D[v_{GSD} - V_{TND}]^2 = K_L[v_{GSL} - V_{TNL}]^2 \qquad (16)$$

Given that $v_i = v_{GSD}$ and $v_{GSL} = V_{DD} - v_o$. Then eq.16 is reduced to the following expression (linear portion of graph on Figure 14):

$$K_D[v_i - V_{TND}]^2 = K_L[(V_{DD} - v_o) - V_{TNL}]^2$$

When Q-point lies between points D and C. The **load** is still on nonsaturation mode but the **driver** is now on saturation mode. Therefore since $i_{DD} = i_{DL}$. We have the following relation:

$$K_L[v_{GSL} - V_{TNL}]^2 = K_D[2(v_{GSD} - V_{TND})v_{DSD} - v_{DSD}^2] \tag{17}$$

Given that $v_i = v_{GSD}$, $v_{GSL} = 0$ and $V_{DSD} = v_o$. Then eq.17 is reduced to the following expression (last non-linear portion of graph on Figure14):

$$K_D[-V_{TND}]^2 = K_L[2(v_i - V_{TND})v_o - v_o^2]$$

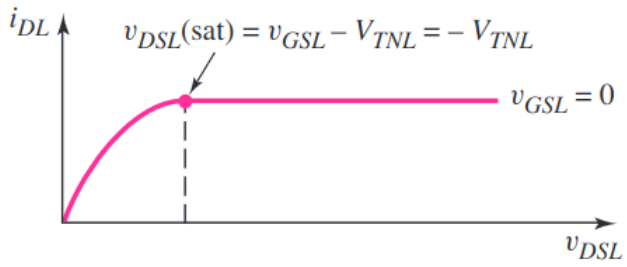

Figure 12: current–voltage characteristic of depletion load

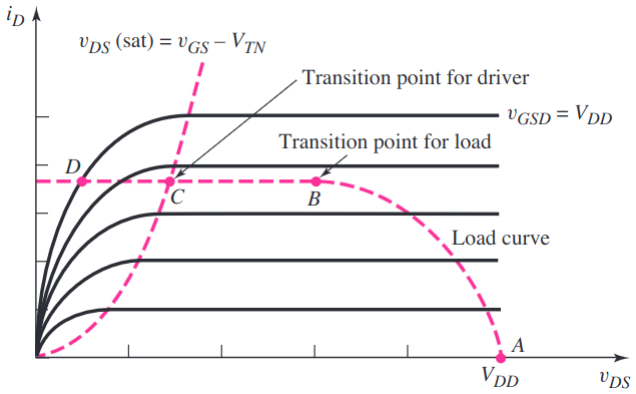

Figure 13: driver transistor characteristics and load curve

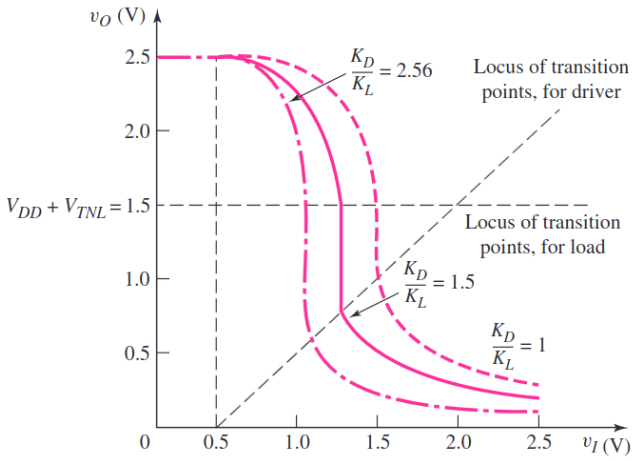

Figure 14: Voltage transfer characteristics of an NMOS inverter with depletion load

4.2 NOR Gate

This circuit (Figure 17) have 2 driver transistor in parallel with a depletion-mode driver.

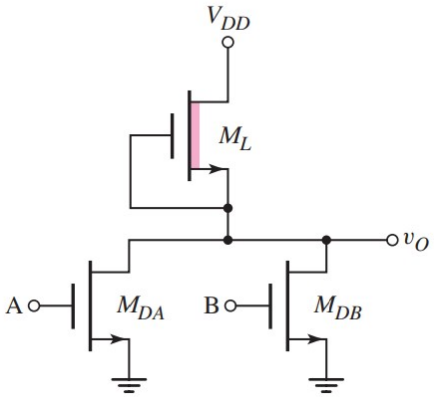

Figure 15: **NOR** gate - NMOS

When **A** and **B** are on cutoff $i_{DA} = i_{DB} = 0$. Therefore $i_{DL} = 0$, $V_{DSL} = 0$ and $v_o = V_{DD} - V_{DSL} = V_{DD}$ (0 NOR 0 = 1)

When only one driver transistor is on cutoff and the other is on. We have a configuration similar to the **inverter**. Therefore $v_o \approx 0V$ (in other words: 0 NOR 1 = 0 and 1 NOR 0 = 0)

When both **A** and **B** are on. We have $i_{DL} = i_{DA} + i_{DB}$.

$$K_L[v_{GSL}-V_{TNL}]^2 = K_A[2(v_{GSA}-V_{TNA})v_{DSA}-v_{DSA}^2]+K_B[2(v_{GSB}-V_{TNB})v_{DSB}-v_{DSB}^2] \quad (18)$$

Given that: $v_{GSL} = 0$, $v_{DSA} = v_{DSB} = v_o$ and $V_{GSA} = V_{GSB} = V_{DD}$. Solving eq.18. We have v_o slow (logical 0). Therefore 1 NOR 1 = 0.

4.3 NAND Gate

This circuit (Figure 16) have 2 driver transistor in series with a depletion-mode driver.

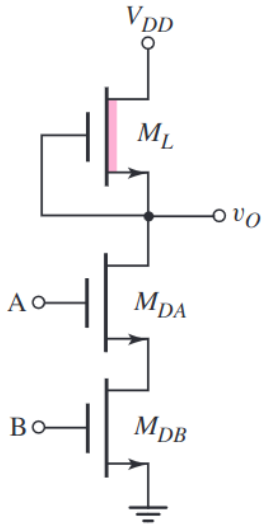

Figure 16: **NAND** gate - NMOS

When only one driver transistor or both are on cutoff. $i_{DA} = i_{DB} = 0$. Therefore $i_{DL} = 0$, $V_{DSL} = 0$ and $v_o = V_{DD} - V_{DSL} = V_{DD}$ (in other words: 0 NAND 1 = 1 and 1 NAND 0 = 1 and 0 NAND 0 = 1)

When both drivers are on. We have a configuration similar to the **inverter**. Therefore $v_o = 0$ (in other words: 1 NAND 1 = 0)

4.4 XOR Gate

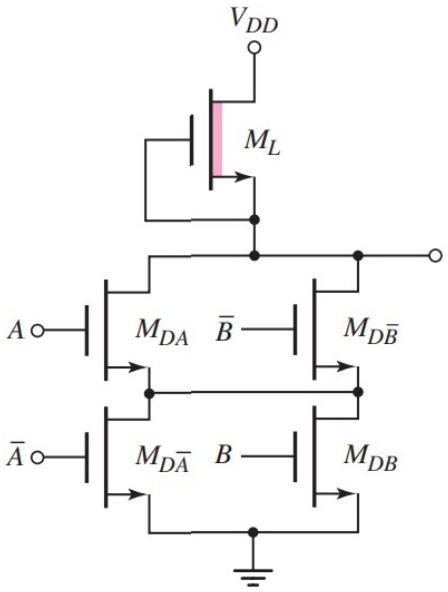

Figure 17: **XOR** gate - NMOS

5 Circuitos Lógicos con BJT

5.1 Inversor

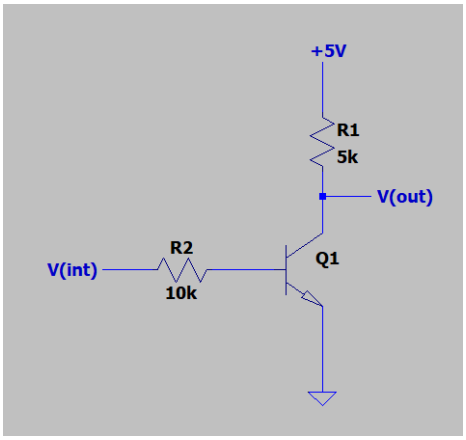

Figure 18:

En la figura 18 el voltaje de entrada puede ser 0 o 1 lógico. En el caso de ser $0V$ (0 lógico), los el transistor Q1 se encontrará en cerrada de colector-emisor y

en corte. Por ende, la resistencia se encuentra en cortocircuito siendo el voltaje de salida $5V$ (1 lógico). Para cuando el voltaje de entrada es $5V$, La permitirá que se abra el canal; además, entrando en saturación. Este funcionaría como un circuito cerrado, y el voltaje de salida es igual a $0V$.

A	$\overline{A}$
1	0
0	1

Table 1: Tabla de valores del inversor

5.2 OR

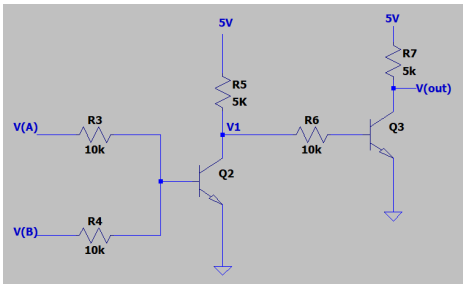

Figure 19:

En el montaje de la figura 19 se tiene la compuerta lógica *or*. Para su funcionamiento: si el voltaje en A y B es $0V$, el transistor Q2 estará en corte, la resistencia $R5$ esta en cortocircuito y V_1 es $5V$, en la parte del circuito con $Q3$ funciona como inversor, entonces el voltaje de salida es la negación de V_1; si $V_A = 5V$ y $V_B = 0V$, o viceversa, el transistor Q2 estará abierto su canal colector-emisor, entoces $V_1 \approx 0V$, entonces $V_{out} = 5V$; y si $V_A = 5V$ y $V_B = 5V$, entonces $V_1 \approx 0V$ y $V_{out} = 5V$.

A	B	$A + B$
0	0	0
1	0	1
0	1	1
1	1	1

Table 2: Tabla de valores

5.3 AND

El circuito AND tiene como equivanlencia el circuito de la figura 20. El montaje

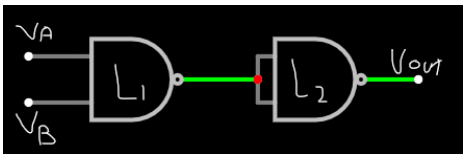

Figure 20: Equivalencia del circuito lógico AND

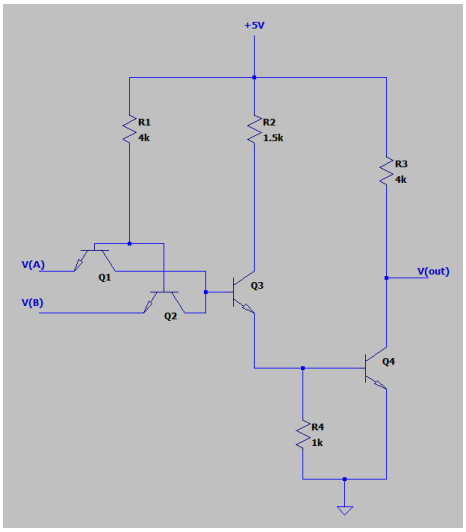

Figure 21:

del circuito NAND se muestra en la figura 21. Analizando el circuito NAND; si $V_A = V_B = 0V$, entonces la corriente avanza hacia la resistencia R1, entonces los trancistores Q3 y Q4 se encuentran en corte, entonces R3 se encuentra en cortocircuito, y el $V_{out} = 5V$; si $V_A = 5V$ y $V_B = 0V$, o viceversa, el voltaje de la base del transistor Q1 y Q2 es fijado a $0.7V$, esto se debe al $0V$ de una de sus entradas, por ende Q3 y Q4 están en corto, igual que el primer caso, $V_{out} = 5V$; y si $V_A = V_B = 5V$, Los transistores Q1 y Q2 enviará la corriente a Q3, abriento su colector-emisor y este a su vez de Q4, entonces $V_{out} \approx 0V$.

A	B	$\overline{A \cdot B}$
0	0	1
1	0	1
0	1	1
1	1	0

Table 3: Tabla de valores del NAND

A	B	$A \cdot B$
0	0	0
1	0	0
0	1	0
1	1	1

Table 4: Tabla de valores del AND

5.4 XOR

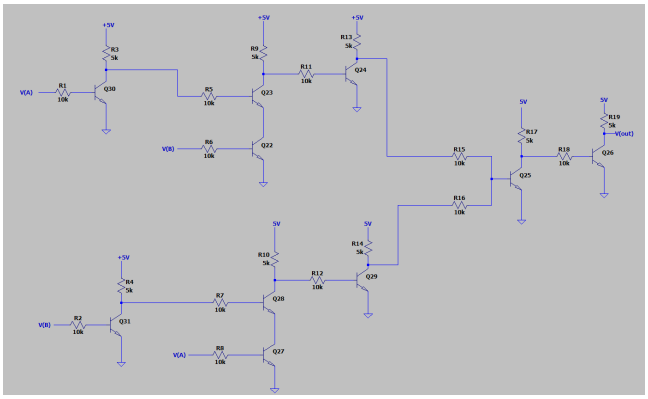

Figure 22:

El operrador XOR tiene su representación en el álgebra de Boole como $(\overline{A} \cdot B) + (A \cdot \overline{B})$. El circuito XOR de la figura 22 es una combianción de los anteriores operadores ya mencionados.

A	B	$(\overline{A} \cdot B) + (A \cdot \overline{B})$
0	0	0
1	0	1
0	1	1
1	1	0

Table 5: Tabla de valores de XOR

6 Observaciones

Al momento de probar en cada compuerta con interruptores de una vía, si el interruptor estaba abierto, no registraba un correcto valor de cero lógico. Esto se solucionó con un cambio de tipo de dos vías, definiendo para cada puerto los valores de $5V$ y $0V$. Con esta modificación se pudo arreglar este problema que se presentó.

7 Conclusiones

Los dos full adder presentaron un correcto funcionamiento, usando las tablas de posibilidades que presenta, se comprobó que los cumple en su totalidad. Además, ambos full adder presentan un cero lógico ligeramente disto al teórico. Como lo hemos explicado, el nuestro 0 lógico es $0V$(punto a tierra), este cambio es aproxximadamente de 32mV para el full adder de BJT y 9mV para el full adder de MOSFET. Pero es una variación mínima a si que podemos considerarlo como un 0 lógico.

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