**Gunjan Atul Lunkad** **Male**
**glunkad26@gmail.com** **DOB: 26/01/2001**
http://www.linkedin.com/in/gl-gunjan-lunkad **+91 7620980424**
http://github.com/glunkad

| Examination | Specialization | University / Board | Year | CPI |
|---|---|---|---|---|
| Graduation | Electronics & Telecommunication | PCCOE | 2023 | 8.24/10 |
| Intermediate | - | HSC | 2019 | 69.8/100 |
| Matriculation | - | SSC | 2017 | 87.6/100 |

## INTERNSHIP

- Computer Architecture, Multi-core Architecture, Embedded Systems, Signal Processing

## Technical Proficiency

**Operating Systems** : Windows, Linux
**Programming Languages** : C, Python, C++, VHDL, Verilog
**Hardware Platforms** : 8051, 8086, ATMEL AVR, Altera EPM3064, MaxV 5M1270 CPLDs
**Softwares/Tools** : Sniper, McPAT, PinPoints, MATLAB, TortoiseHg, Visual Studio, LaTeX

## Key Academic Projects

- **M.Tech Thesis - Scheduling Heterogeneous Multi-cores: Using Performance Variation Across Phases**
  (Guide : Prof. Virendra Singh, IIT Bombay) **[Jul '13 - Jul '14]**
  - **Abstract**: In the multicore era apart from the challenge of increasing processor's performance, computer architects must also focus on designing energy efficient multicore processor so that processor's power consumption doesn't exceed its power budget. A dynamic scheduler was proposed which analysed the performance variation of an application at runtime to utilize time-varying execution behaviour of the application and schedules the application on the most suitable idle core among all the cores available in heterogeneous multi-core architecture. The work compared a static scheduler with the dynamic scheduler. It was shown that the dynamic scheduler is more power efficient than static scheduler with an average perf/watt benefit of 26% on the analysed benchmarks.

- **R&D Project - Opportunities and Challenges in Multicore Architecture**
  (Guide : Prof. Virendra Singh, IIT Bombay) **[Jan '13 - Jun '13]**
  - **Abstract** Migration from single-core to many-core era has provided us with various opportunities & challenges. Reviewed literature related to different core configurations like homogeneous, heterogeneous & morphcores and analysed the challenges in designing a computer architecture in constrained power budget.

## Relevant Technical Projects

- **Implementation of Cache Replacement Policies** **[Mar '13 - Apr '13]**
  - Implemented LLC Cache Replacement Policies like LRU, LFU, SRRIP, DRRIP, ABRip.

- **Design of 2 way Out of Order (OoO) Superscalar ARM 7 Processor** **[Mar '13 - Apr '13]**
  - Studied ARM ISA & developed the required control words and designed necessary processor architecture.
  - Implemented using Verilog, major hardware blocks like Branch Predictor, Instruction Decoder, Reservation Station, 5 Stage Pipeline, ROB etc. required for out of order execution of instruction.

- **Interrupt Controller of Microprocessor 8085** **[Apr '12]**
  - Hardware and software interrupts were implemented using VHDL.
  - Synchronisation, timing constraints, & handshaking with other internal modules were taken care of.

- **Data Processor of Microprocessor 8085** **[Mar '12]**
  - All data movement and ALU operation instruction were implemented using Verilog.
  - Handshaking with Bus Interface Unit was also implemented for memory read/write operations.

## Work Experience

- **Senior Software Engineer, Huawei Technologies India Pvt. Ltd., Bangalore** **[Jun '08 - Jul '11]**
  - **Development of MDBLite: Database to store messages in mobile phones**.
    Being part of the platform team, developed APIs to provide services to the application (GUI) team. Responsible for development of APIs, their functionality testing, release activities and later maintenance of the project. C language was used on BREW platform for the development of interfaces.
  - **Development of RSS Reader for Smartphones.**
    Understood the already developed module and customized it to support new feature requirements for the smartphones. Responsible in increasing the speed of the app by changing the database structure which was used to store the content of the RSS feeds in the SQLite DB. Added new feature to update the RSS feeds automatically as per user setting.
  - **Development of GUI for Conversation and Panchang App for Smartphone**.
    Developed Graphical User Interface for Conversation (SMS app) and Panchang (Vedic Astrology app)
- **Research Assistant, Wadhwani Electronics Lab, IIT Bombay** **[Jul '11 - Jul '14]**
  (Guide : Prof. Mahesh B. Patil, IIT Bombay)
  - Working as a Teaching Assistant for conducting undergraduate lab courses.
  - Conducted workshops on Modern Digital Design at BVM Engineering College, Vallabh Vidyanagar, Anand, Gujarat as part of e-Prayog, "Virtual Labs", IIT Bombay, an MHRD initiative.

## Relevant Courses

- Processor Design
- Advanced Computer Archiecture
- Advanced Topics in Computer Architecture
- Embedded Systems Design
- Embedded Systems
- VLSI Design Lab

## Scholastic Achievements

- Recipient of **Research Assistant Scholarship** at Indian Institute of Technology Bombay by Ministry of Human Resource Development, Government of India
- **Dean's Appreciation Letter** from Faculty Coordinator, Student Mentor Program; Dean, Student Affairs and Dean, Academic Program, IIT Bombay for remarkable efforts on student mentoring of post graduate students as the overall coordinator of Institute Student Companion Program, IIT Bombay.

## Positions of Responsibility

**Overall-Coordinator, Institute Student Companion Programme (ISCP)** **[May '13 - April '14]**

- Leading the ISCP team in creating an environment for smooth transition of PG freshers to the new college.
- Selected a team of 140 mentors to guide, help and motivate PG freshers in pursuit of their academic and non-academic goals. Working with the team in organising Orientation Programs, Workshops and session for freshers.
- Around 80% freshers found that the allotted mentors and programs done by ISCP were very helpful.

## Extra Curricular activities

- Part of the team of 937 students which was awarded **Guinness World Record** and **Limca Book of Record** for solving 3 x 3 x 3 Rubik Cube puzzle with most students at a time. [Mar '12]
- Secured **First** position in E-Modelling and Kritika (circuit designing contest) in APEX'06, POWERFEST'07 (National Level Techical Fest) at NIT Kurukshetra. [Nov '06, Feb '07]

## Hobbies and Interests

- Watching Documentaries, Reading Fiction and Non-Fiction books, Trekking, Solving Rubik Cube

*Updated on 26th Dec 2016*