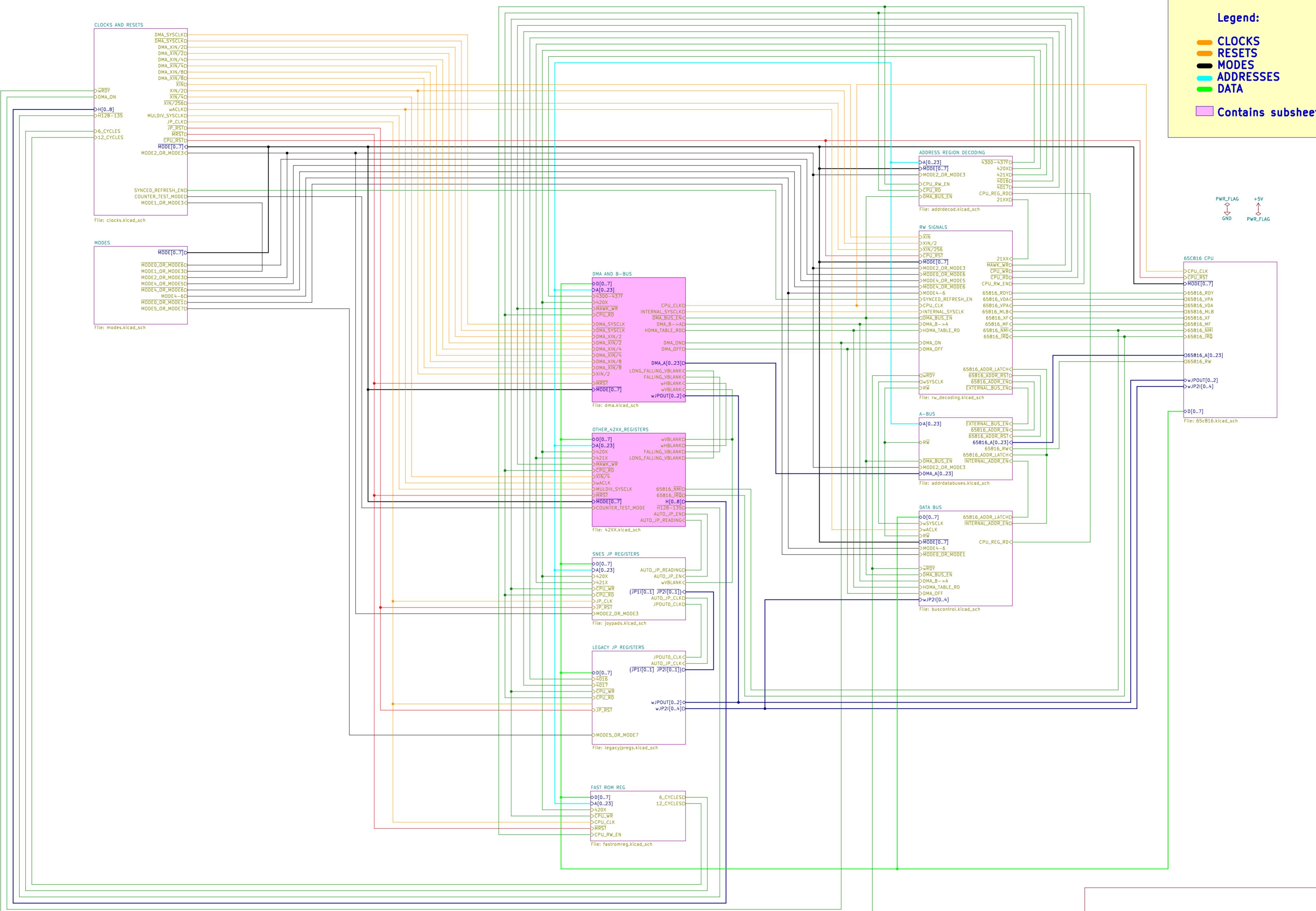


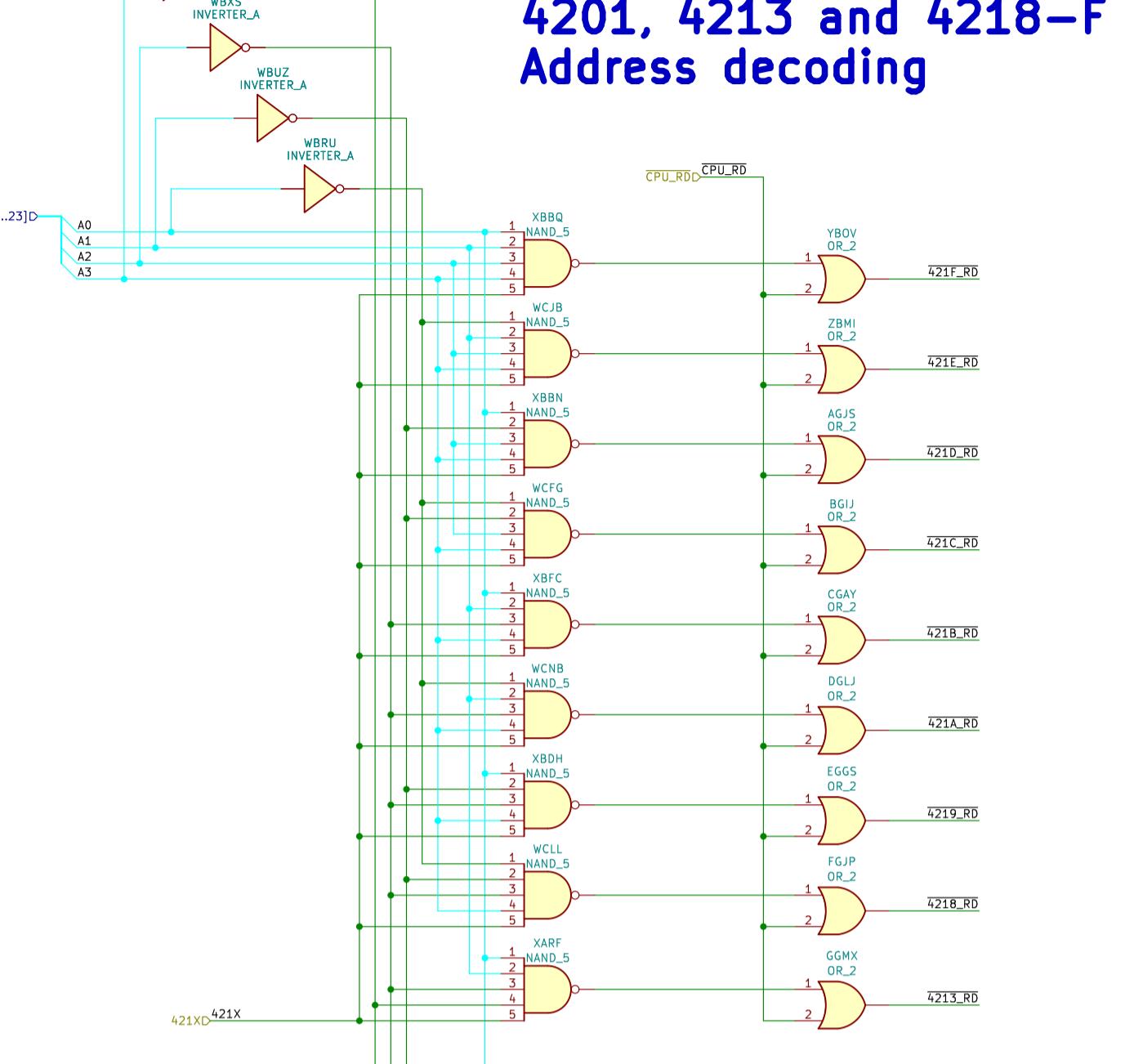
Legend:

- CLOCKS
- RESETS
- MODES
- ADDRESSES
- DATA
- Contains subsheets

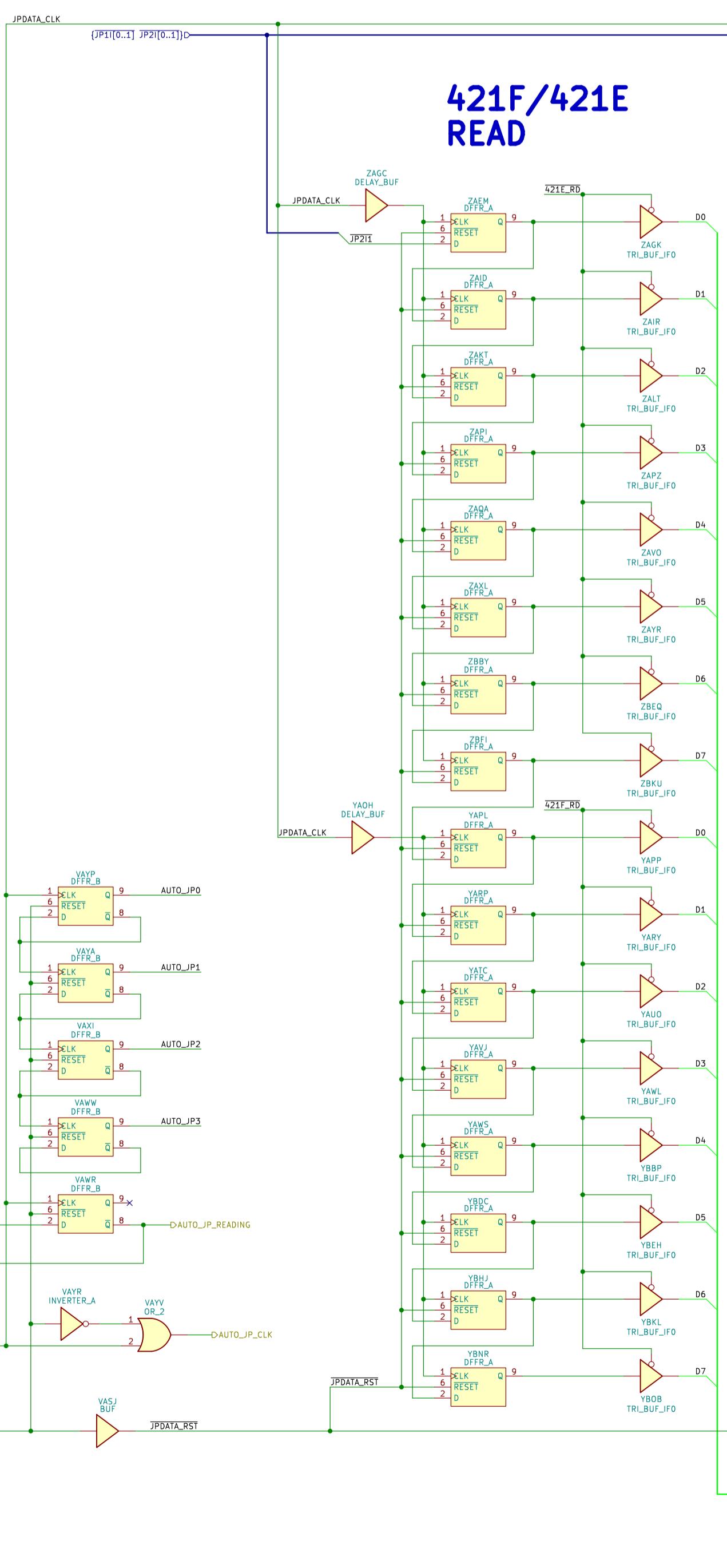
PWR_FLAG
GND
+5V



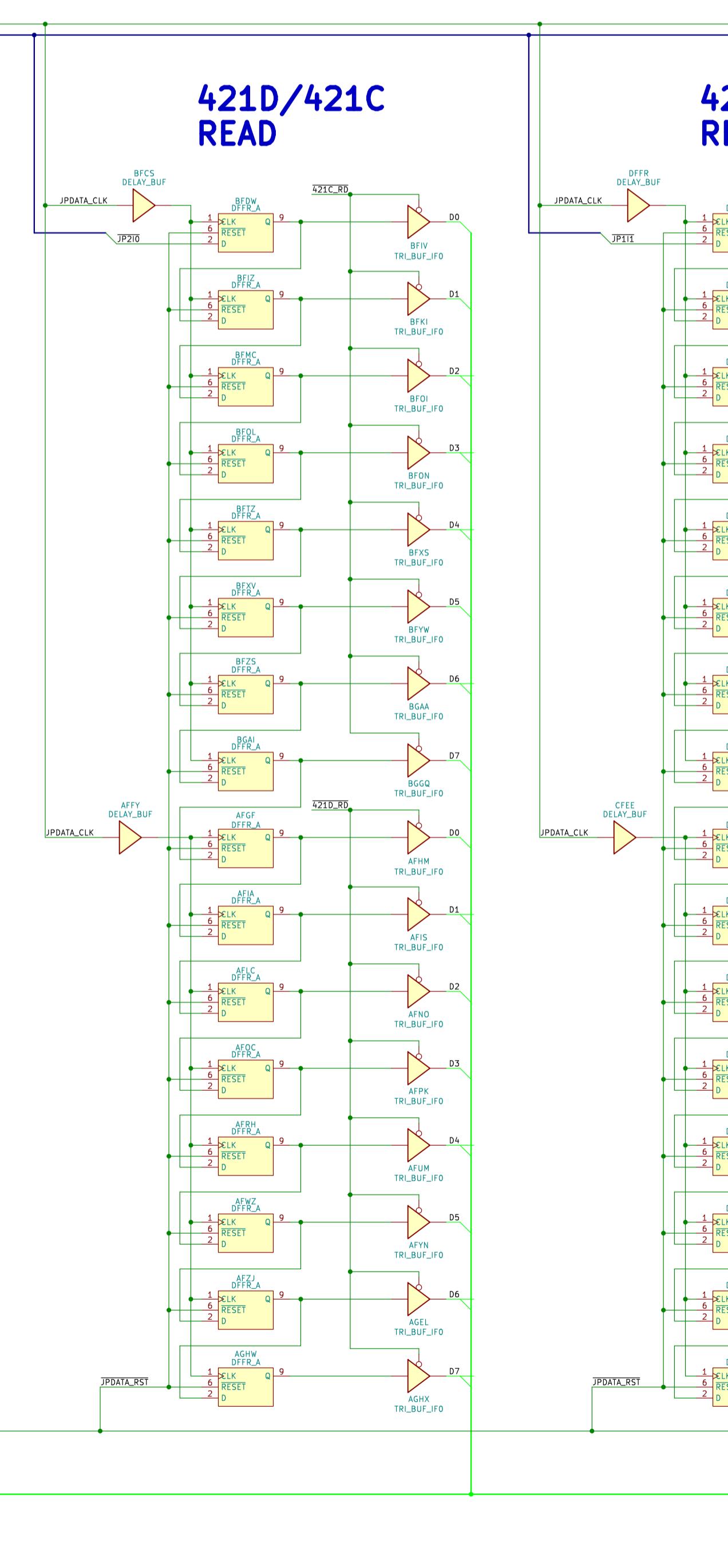
4201, 4213 and 4218-F Address decoding



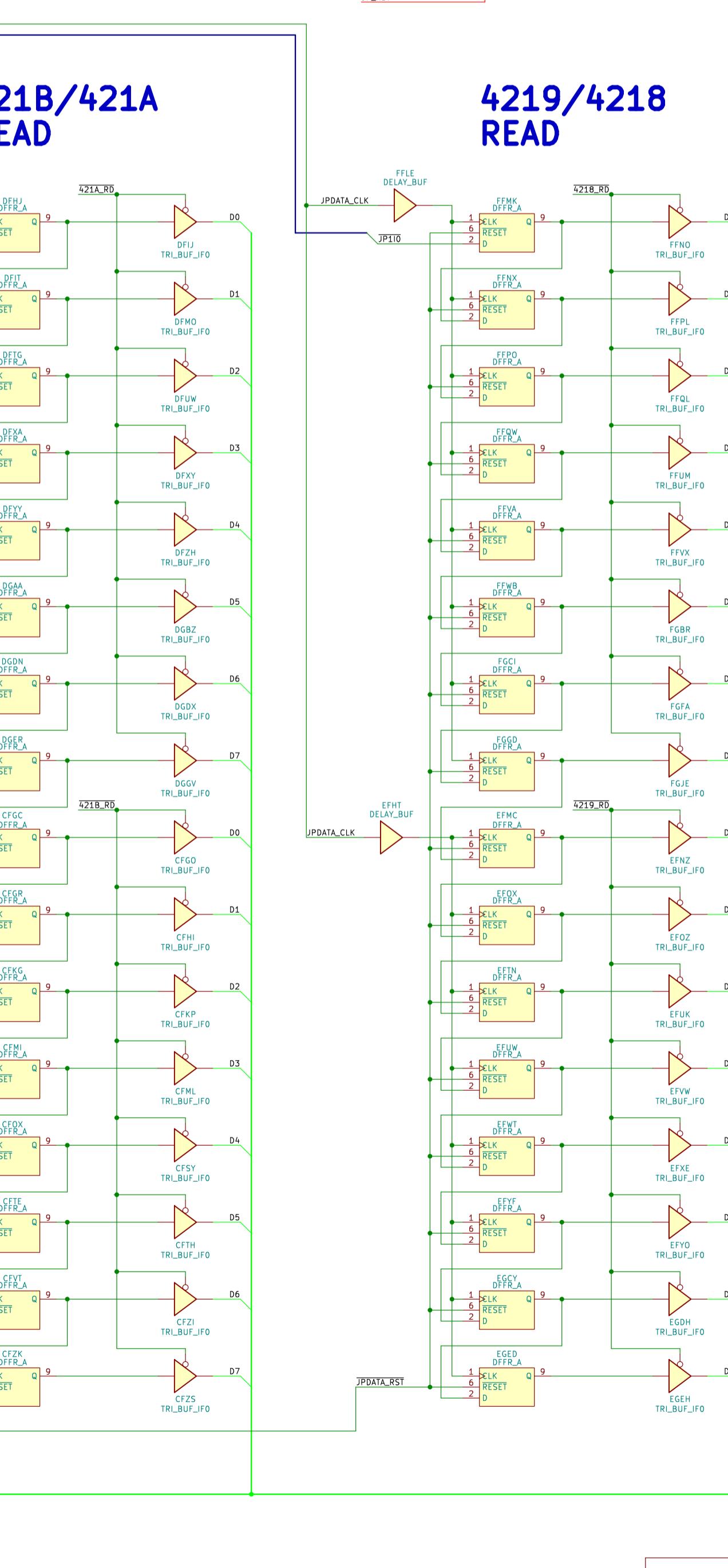
421F/421E READ



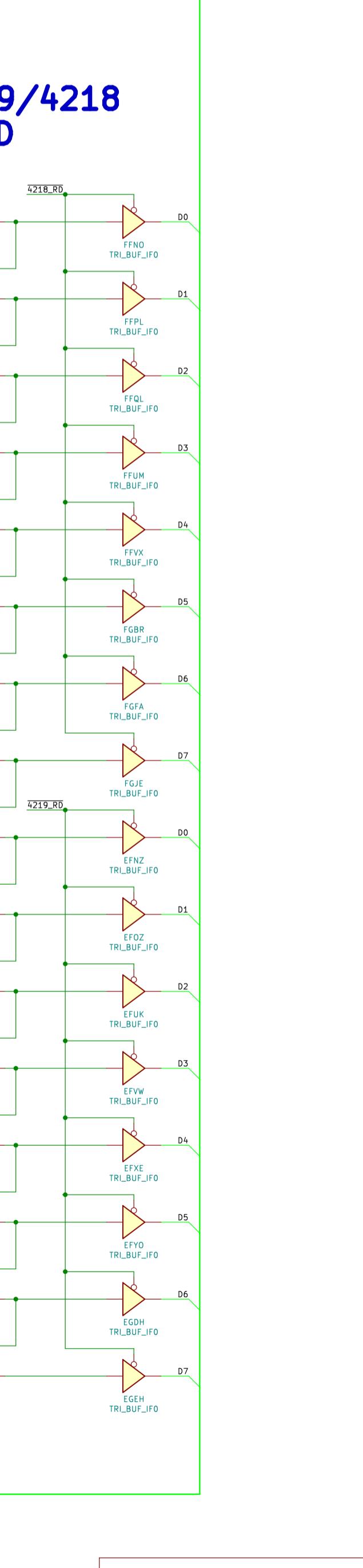
421D/421C READ

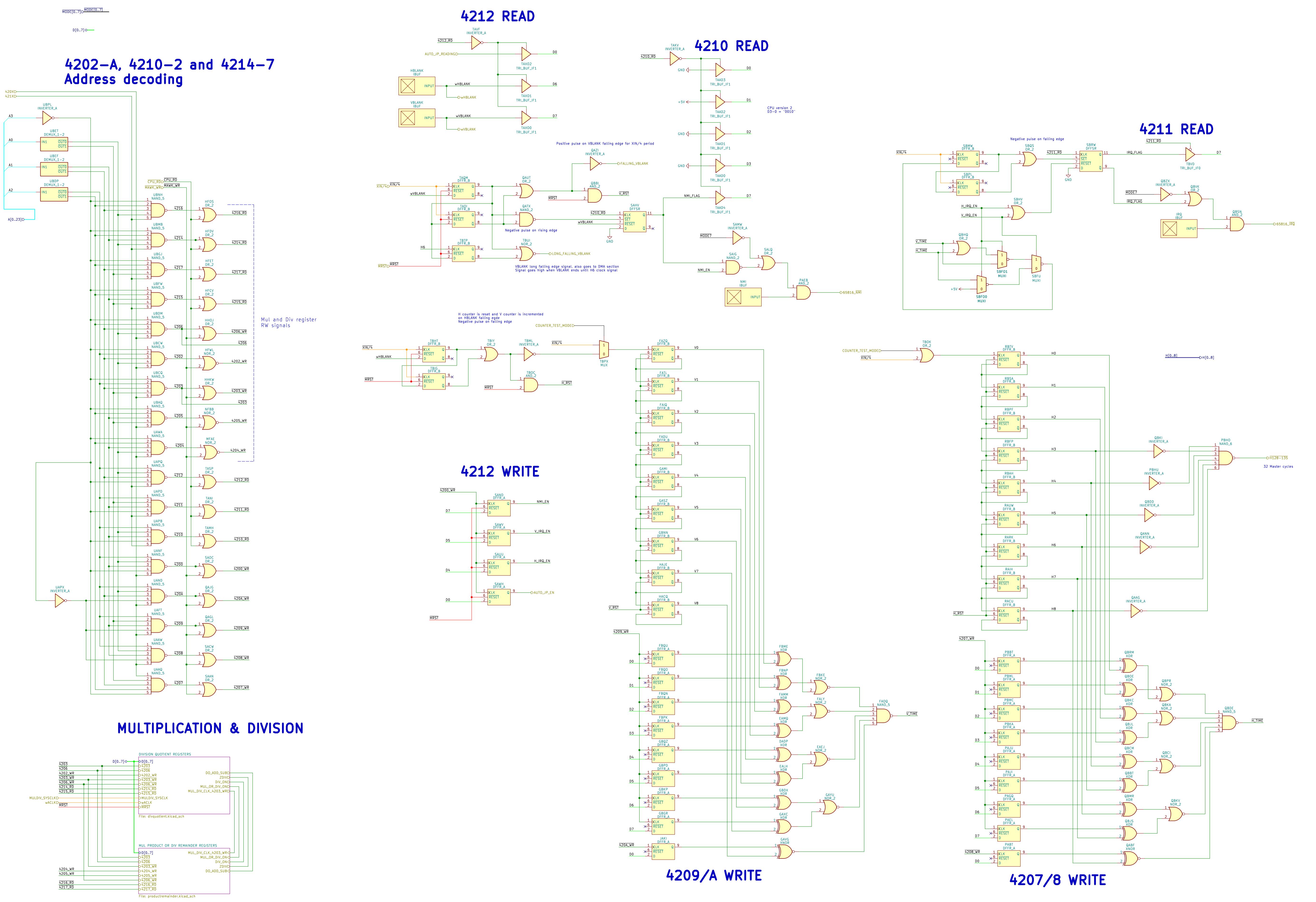


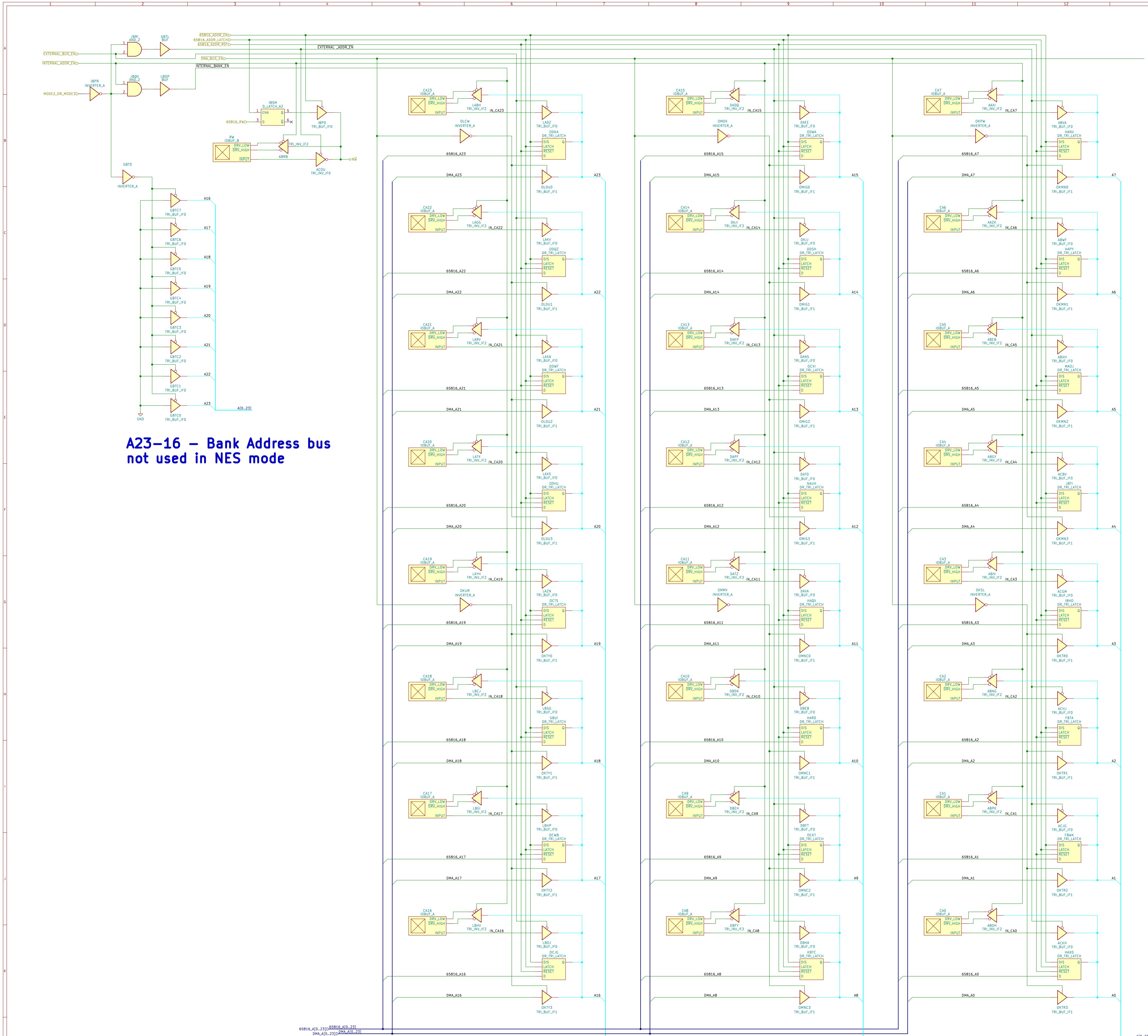
421B/421A READ



4219/4218 READ

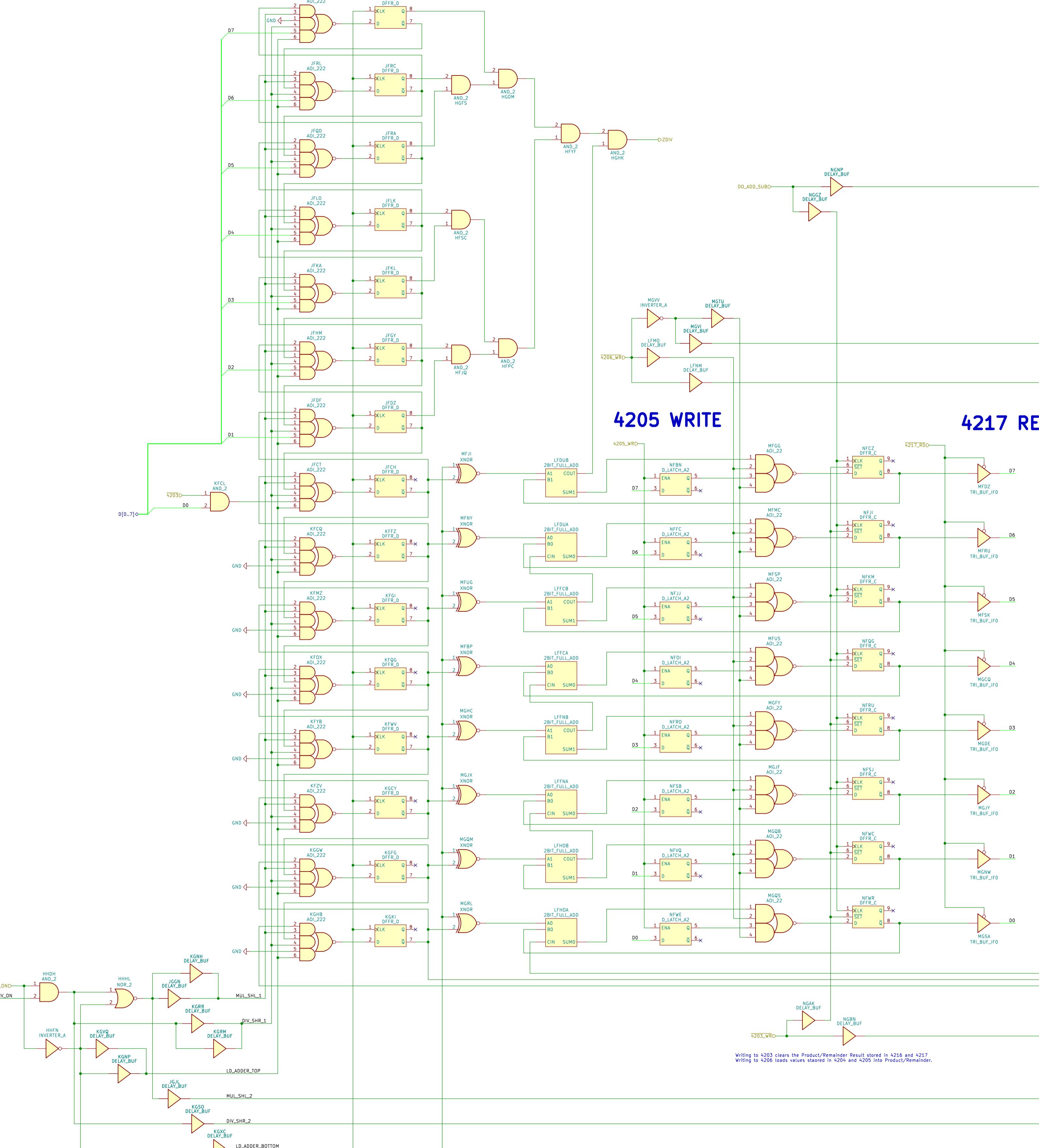




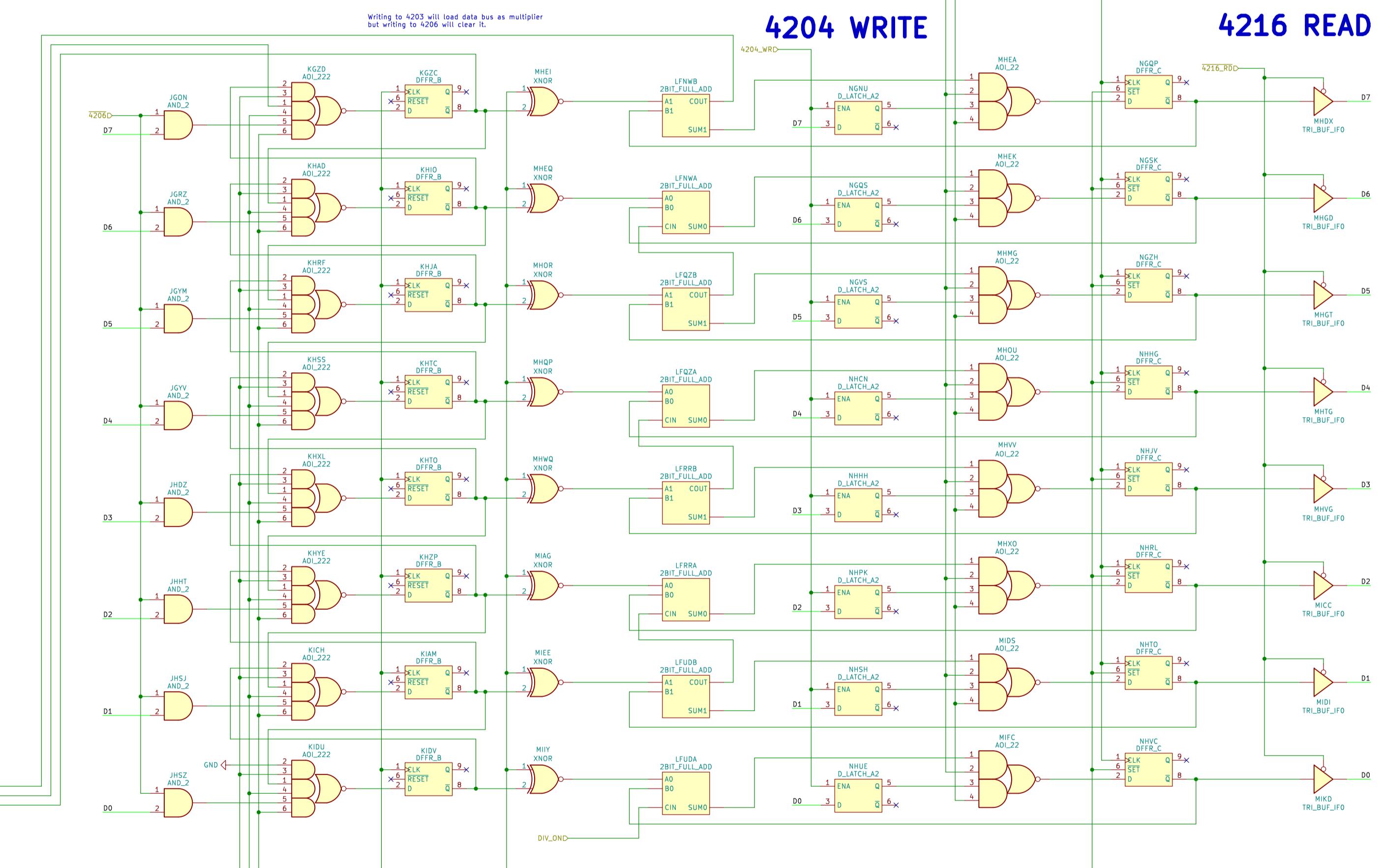


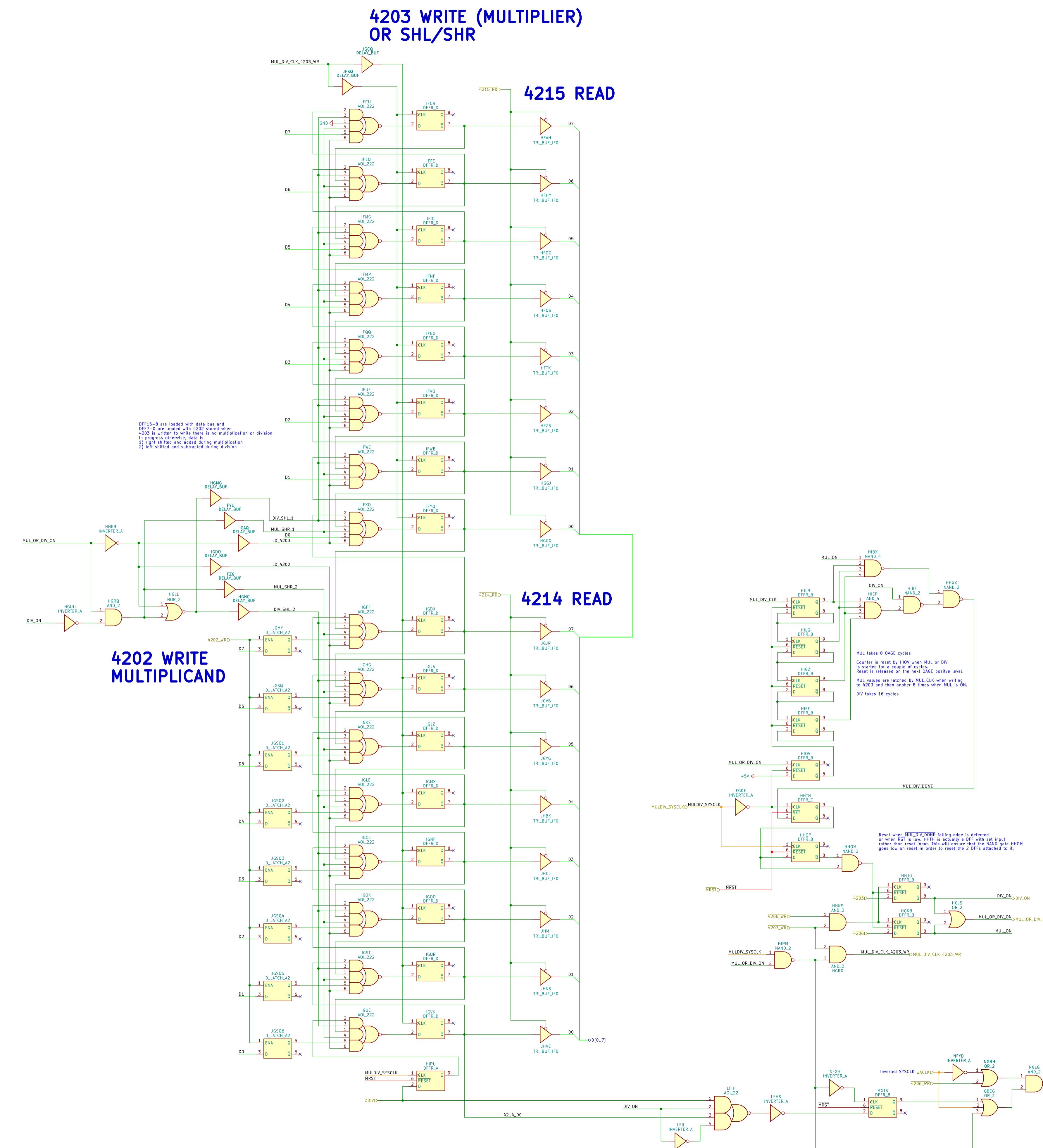
A-BUS

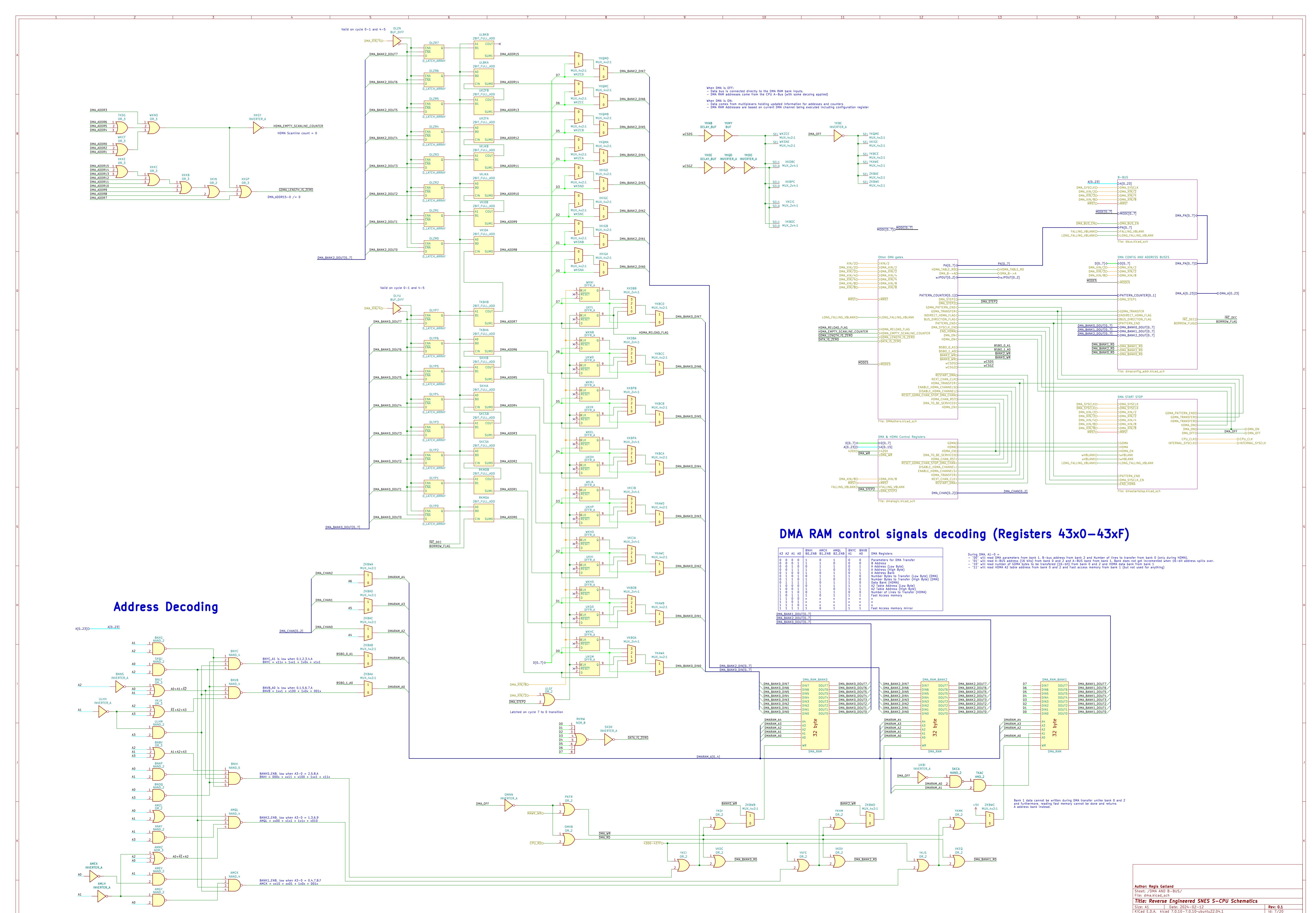
4203 WRITE (MULTIPLIER) OR 4206 WRITE OR SHL/SHR

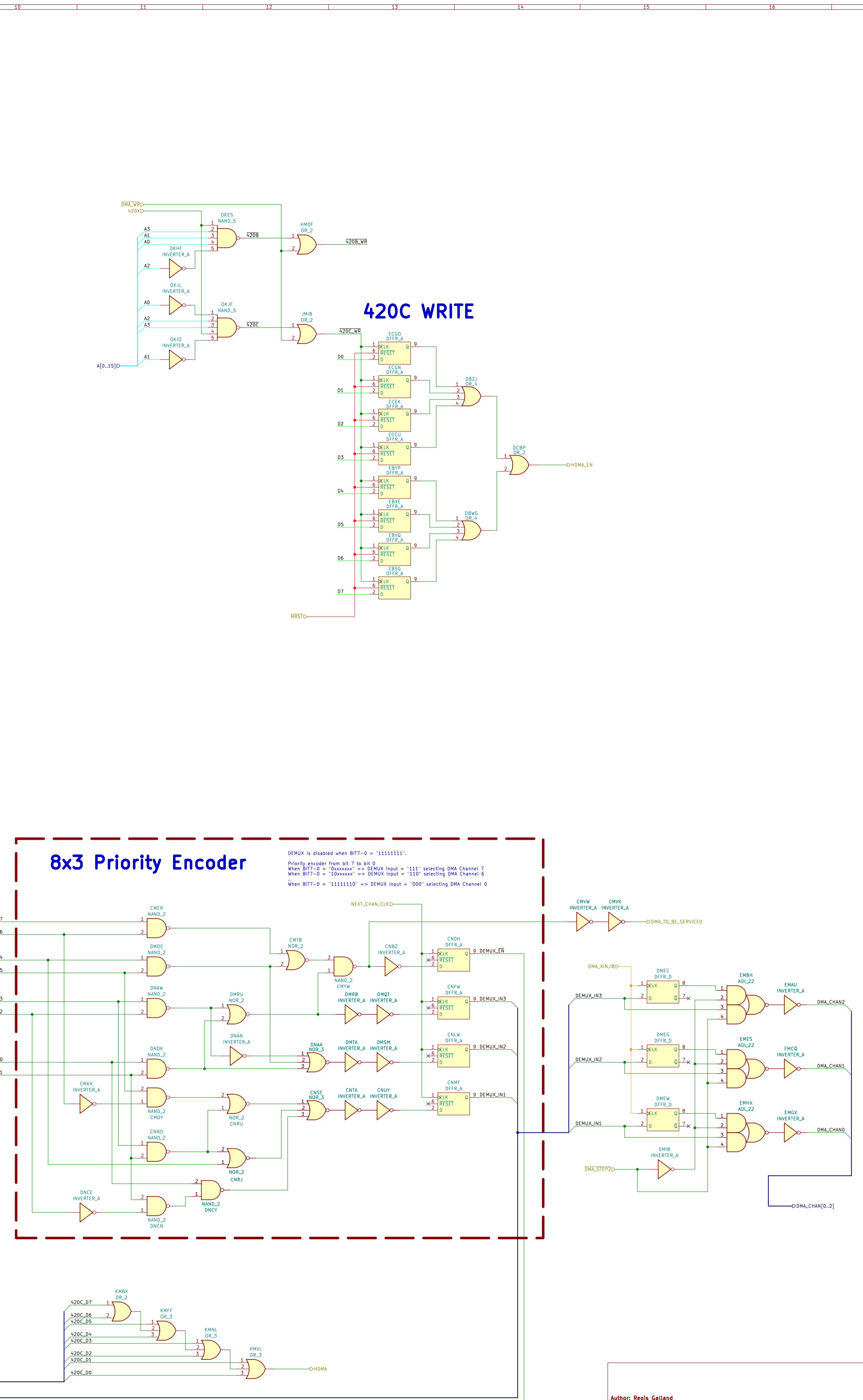
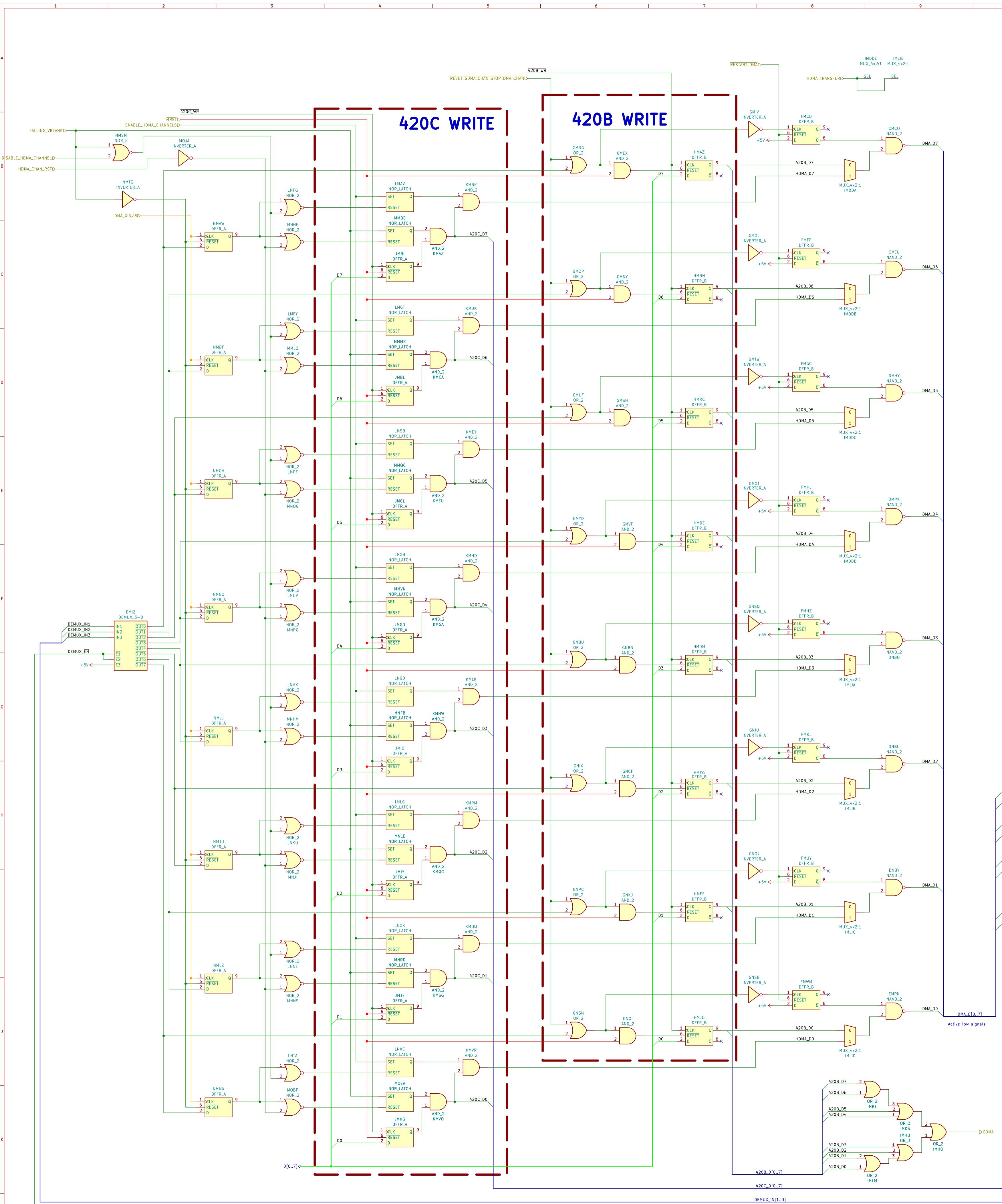


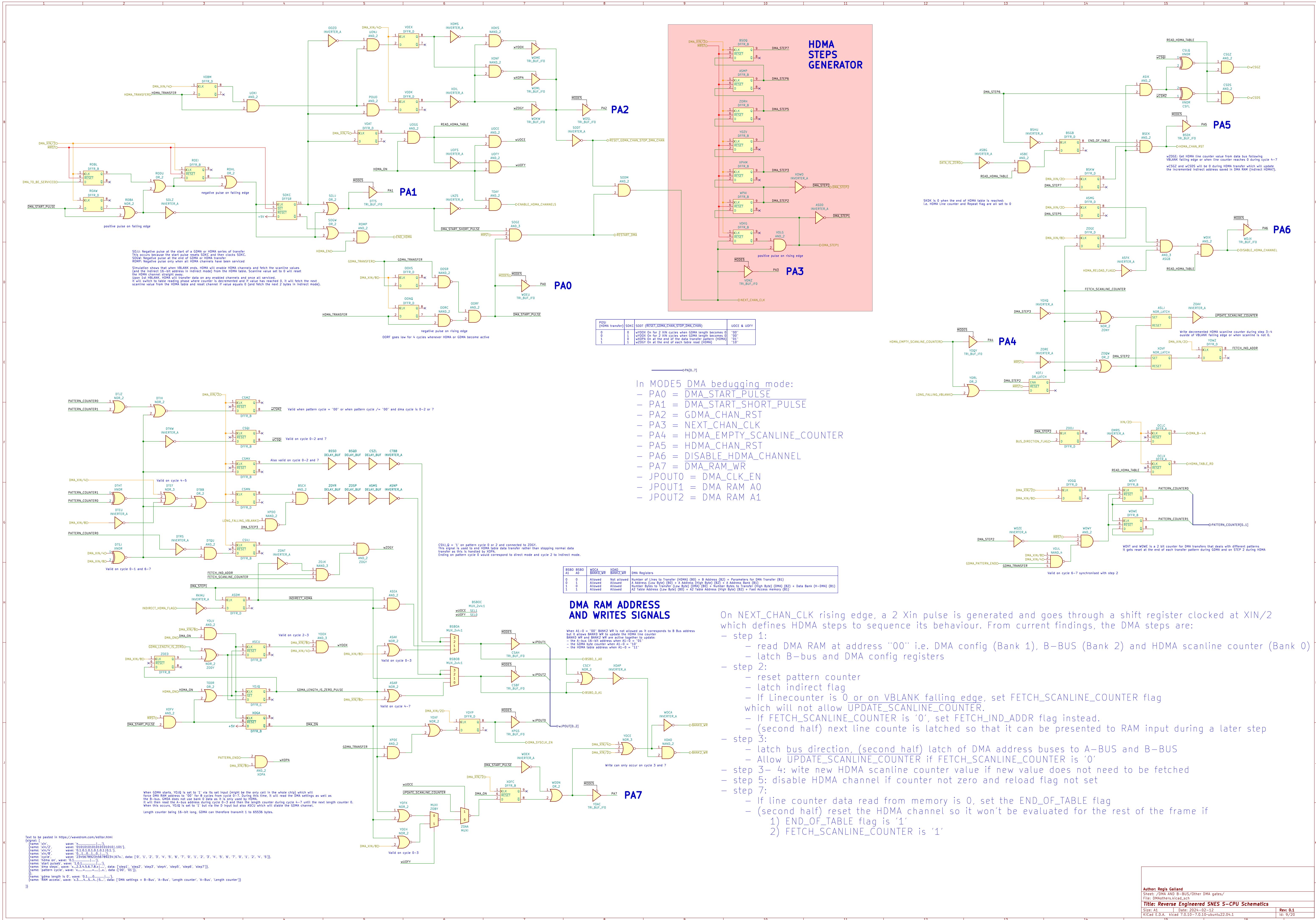
4217 READ









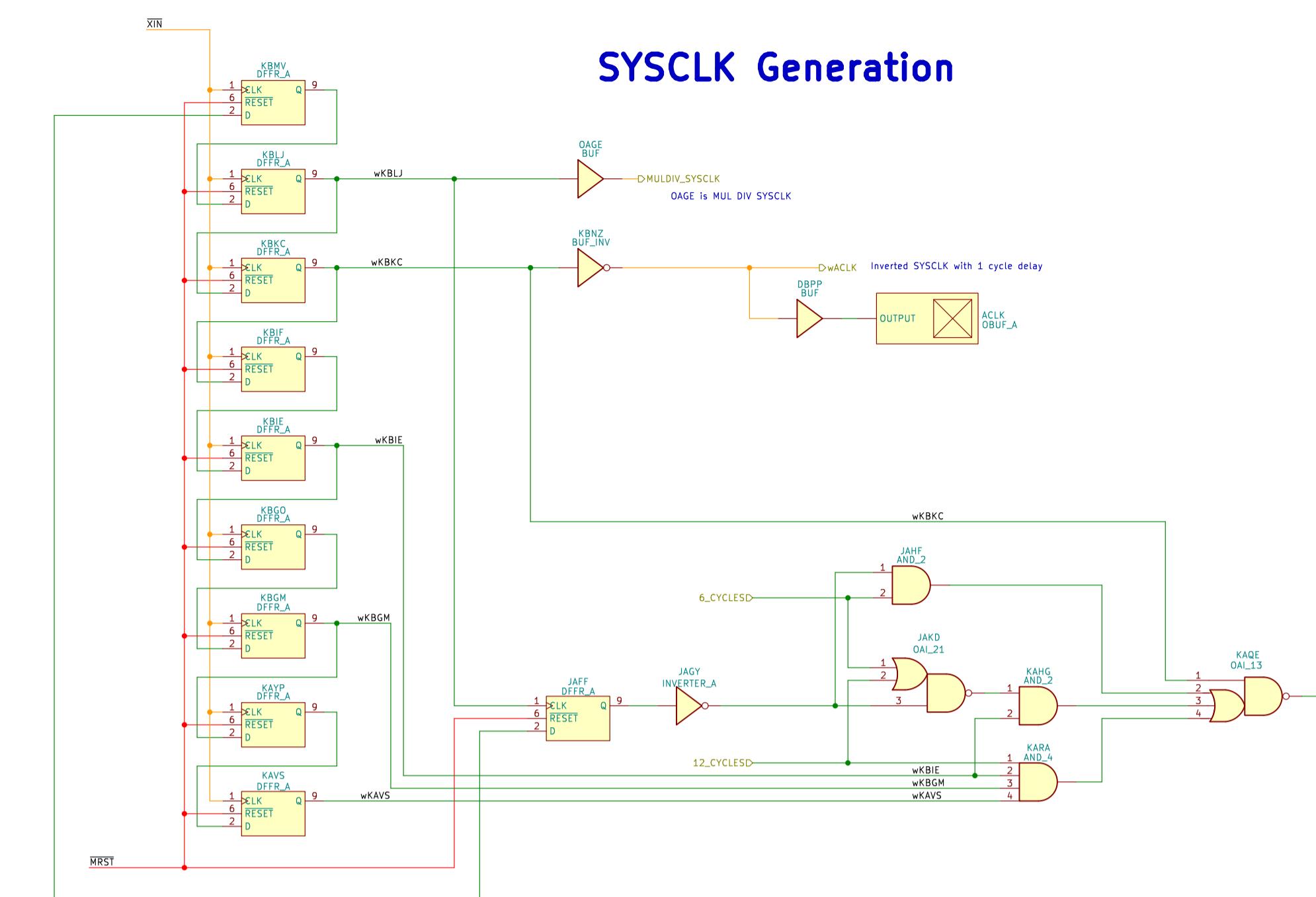


In MODE5 DMA debugging mode:

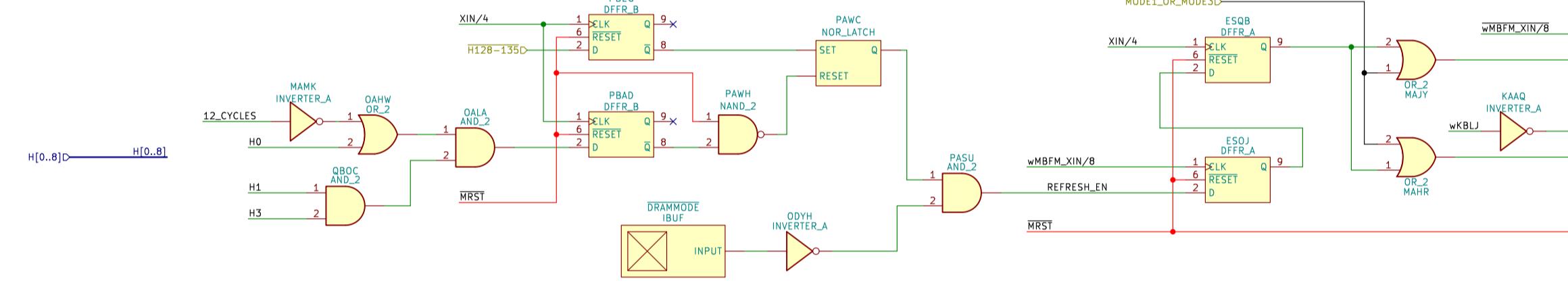
- PA0 = DMA_START_PULSE
- PA1 = DMA_START_SHORT_PULSE
- PA2 = GDMA_CHAN_RST
- PA3 = NEXT_CHAN_CLK
- PA4 = HDMA_EMPTY_SCANLINE_COUNTER
- PA5 = HDMA_CHAN_RST
- PA6 = DISABLE_HDMA_CHANNEL
- PA7 = DMA_RAM_WR
- JPOUT0 = DMA_CLK_EN
- JPOUT1 = DMA RAM AO
- JPOUT2 = DMA RAM A1

On NEXT_CHAN_CLK rising edge, a 2 Xin pulse is generated and goes through a shift register clocked at XIN/2 which defines HDMA steps to sequence its behaviour. From current findings, the DMA steps are:

- step 1:
 - read DMA RAM at address "00" i.e. DMA config (Bank 1), B-BUS (Bank 2) and HDMA scanline counter (Bank 0)
 - latch B-bus and DMA config registers
- step 2:
 - reset pattern counter
 - latch indirect flag
 - If Linecounter is 0 or on VBLANK falling edge, set FETCH_SCANLINE_COUNTER flag which will not allow UPDATE_SCANLINE_COUNTER.
 - If FETCH_SCANLINE_COUNTER is '0', set FETCH_IND_ADDR flag instead.
 - (second half) next line counte is latched so that it can be presented to RAM input during a later step
- step 3:
 - latch bus direction, (second half) latch of DMA address buses to A-BUS and B-BUS
 - Allow UPDATE_SCANLINE_COUNTER if FETCH_SCANLINE_COUNTER is '0'
- step 3 - 4: wite new HDMA scanline counter value if new value does not need to be fetched
- step 5: disable HDMA channel if counter not zero and reload flag not set
- step 7:
 - If line counter data read from memory is 0, set the END_OF_TABLE flag
 - (second half) reset the HDMA channel so it won't be evaluated for the rest of the frame if
 - 1) END_OF_TABLE flag is '1'
 - 2) FETCH_SCANLINE_COUNTER is '1'



DRAM refresh is enabled by setting it on for 32 master cycles from H=128 to H=135. DRAM refresh is disabled whenever H[3..0] = "1xx" when accessing memory. It means that DRAM refresh comes on at H128 ('010000000') and gets disabled at H135 ('010001010') and SYSCLK signal is feed to DRAM refresh pin during 10H cycles of 40 Master cycles.



SYSCLK and SYSCLK signals used in the DMA region

System clocks
 $2 \times XIN/2$

$1 \times XIN/2$

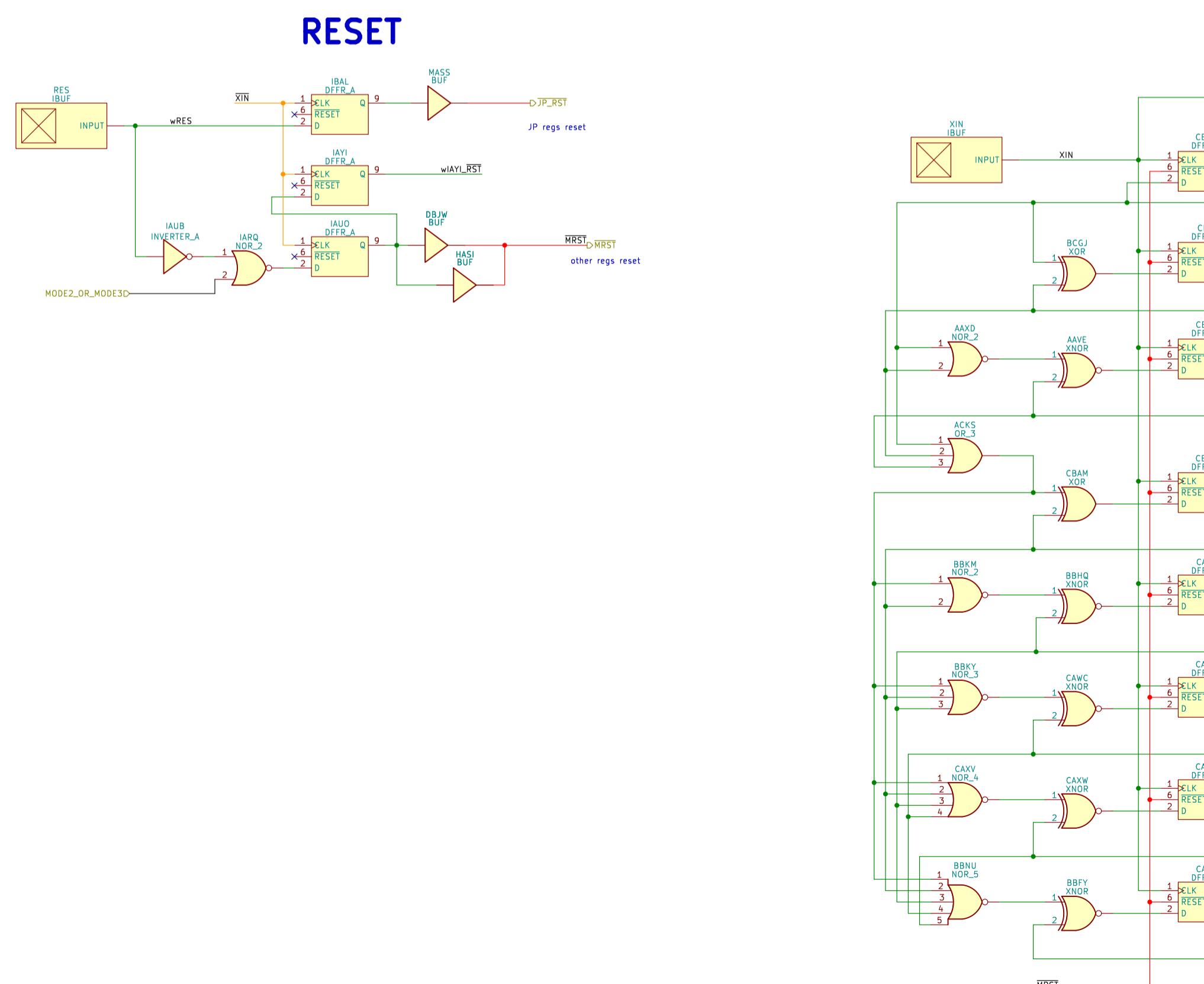
$2 \times XIN/4$

$2 \times XIN/4$

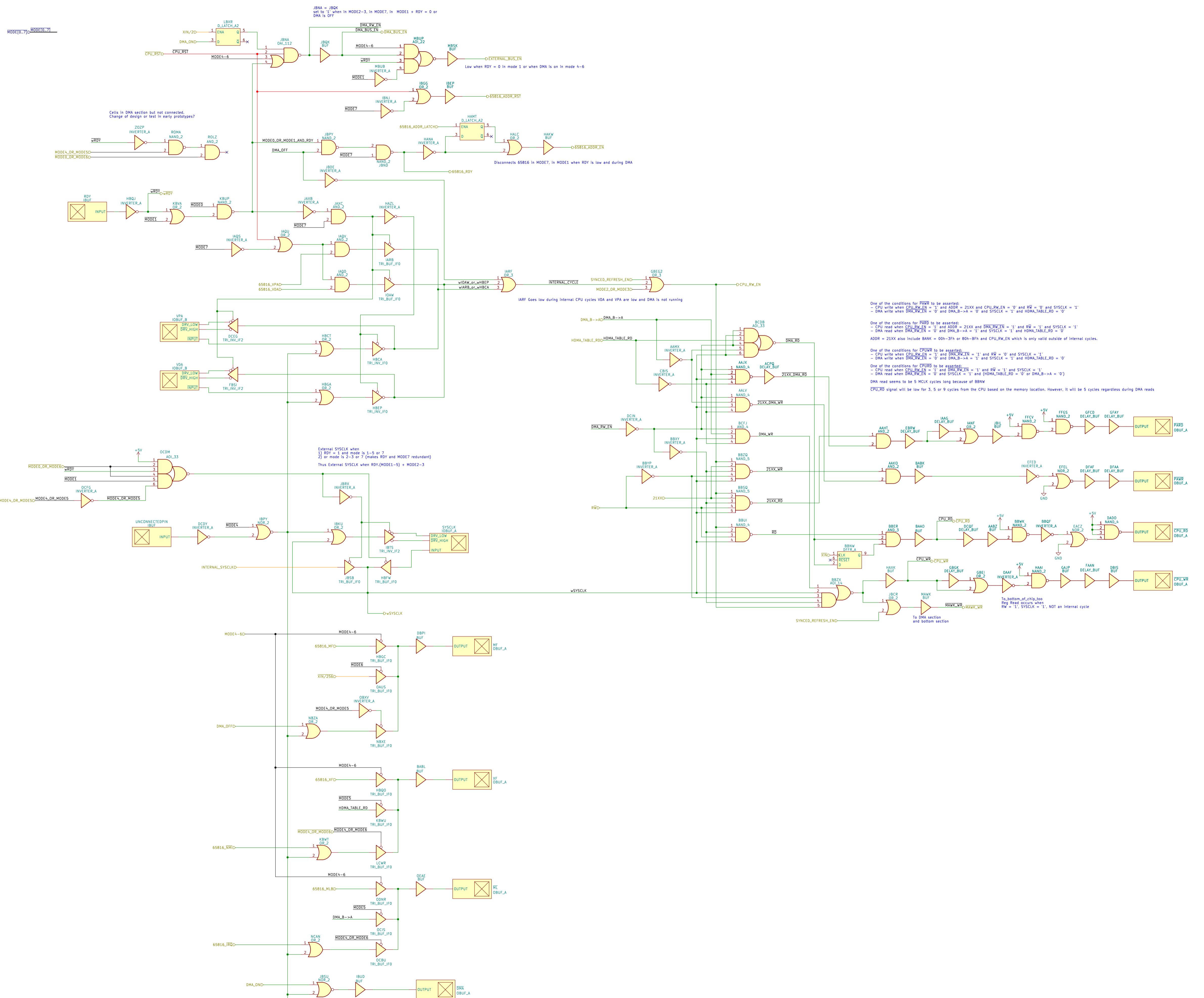
$1 \times XIN/8$

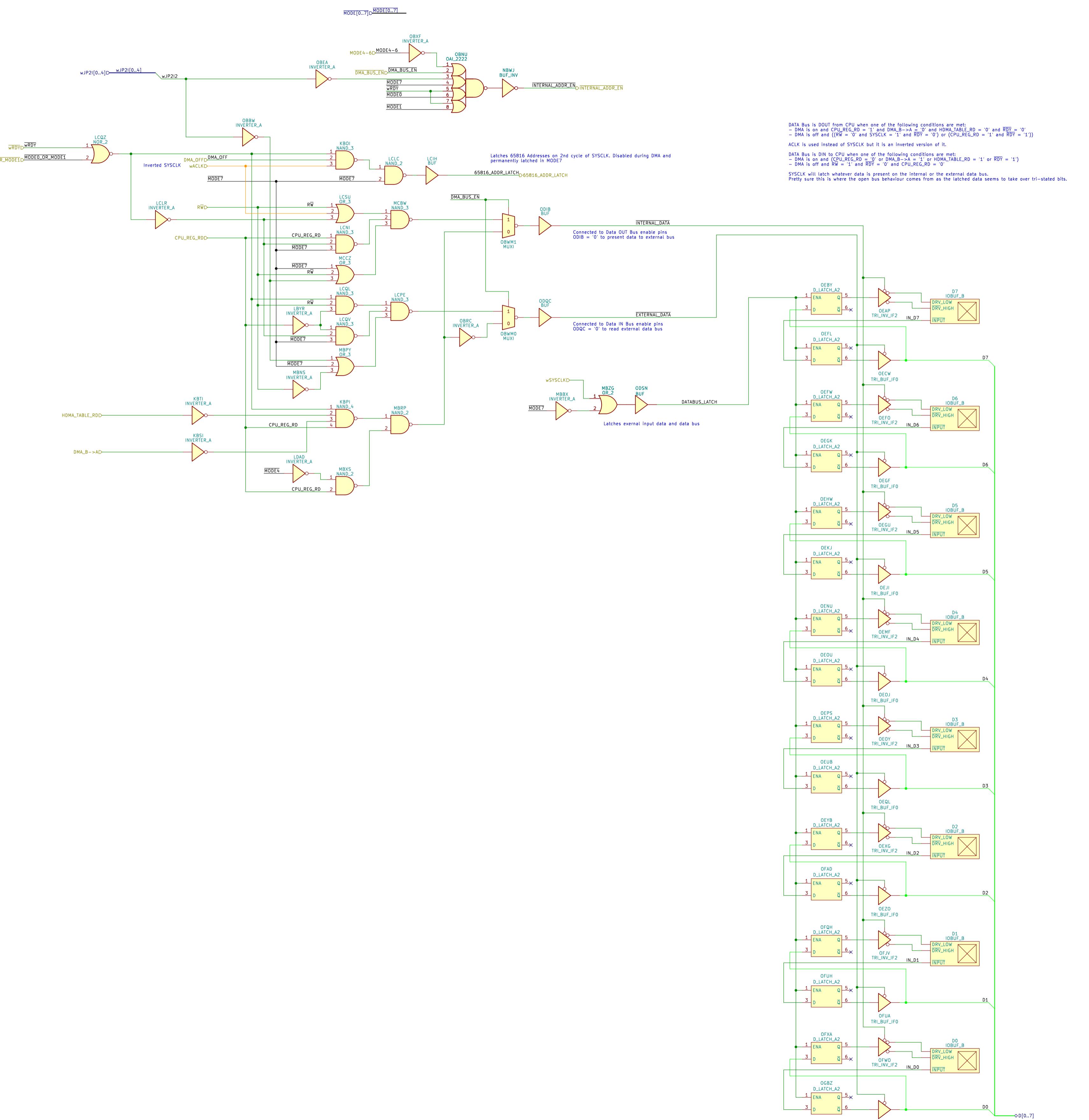
$1 \times XIN/8$

$1 \times XIN/256$

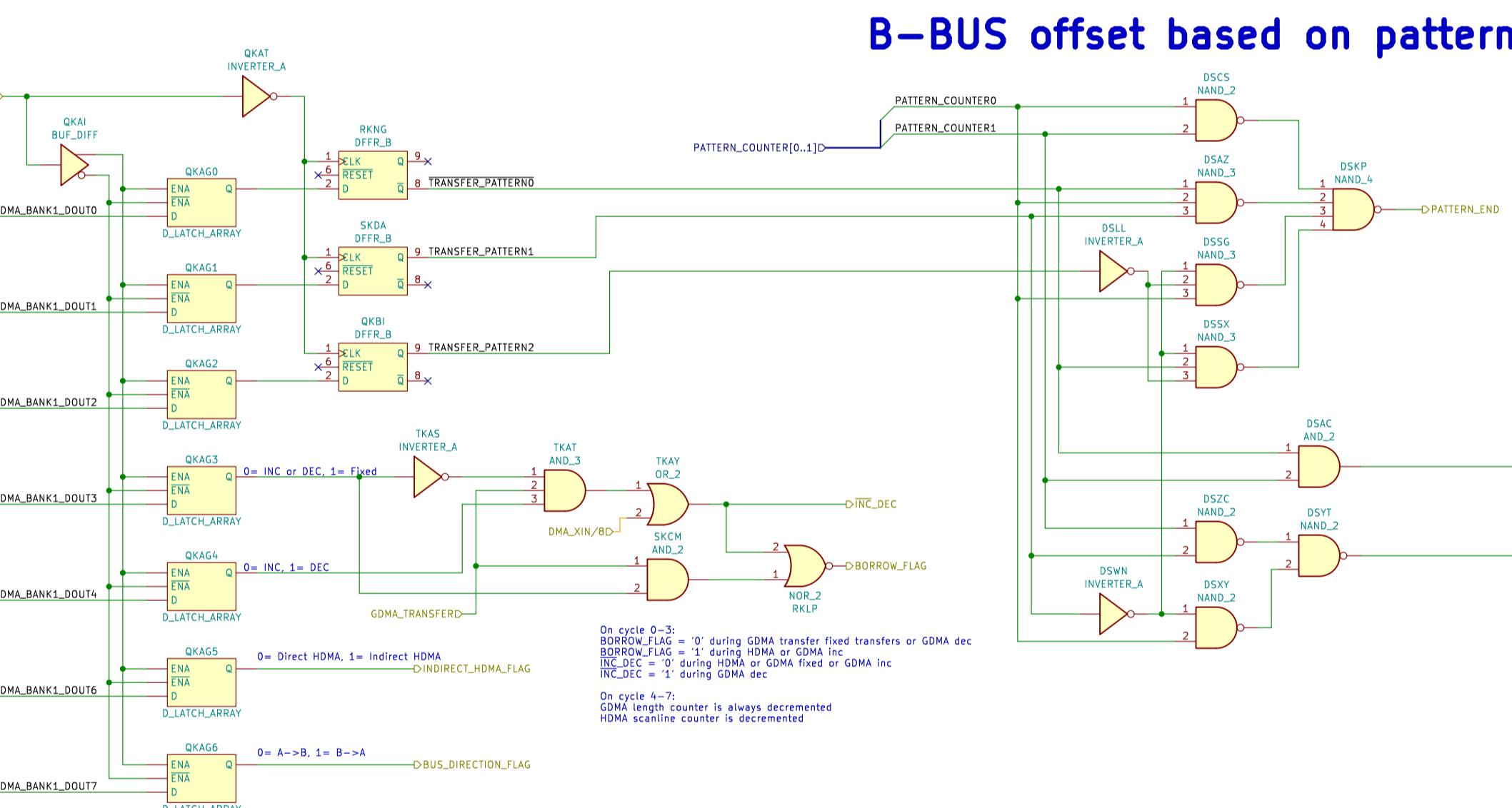


Normal clock is XIN/256 which will take 3 scanning lines to fill in jp shift registers.
In MODE6, XIN/4 clock is used instead when RDT = 0.

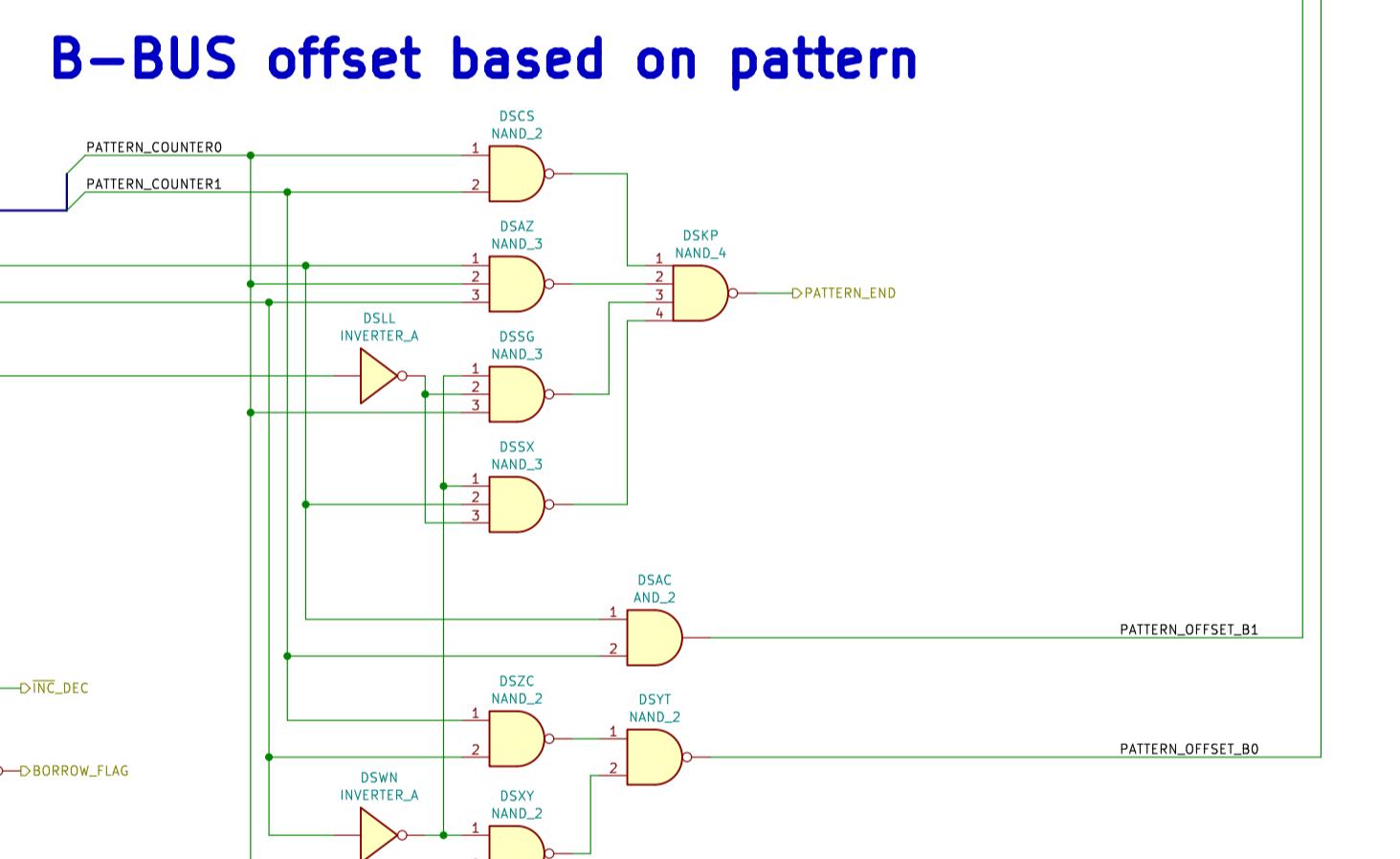




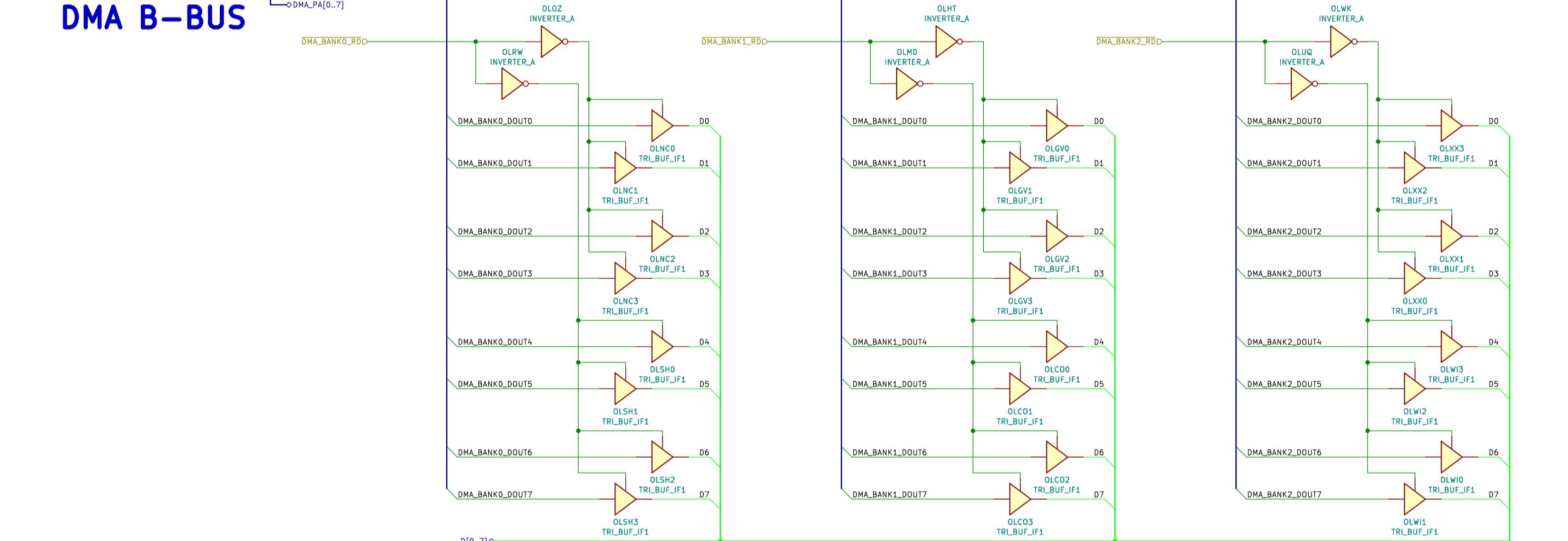
DMA Configuration



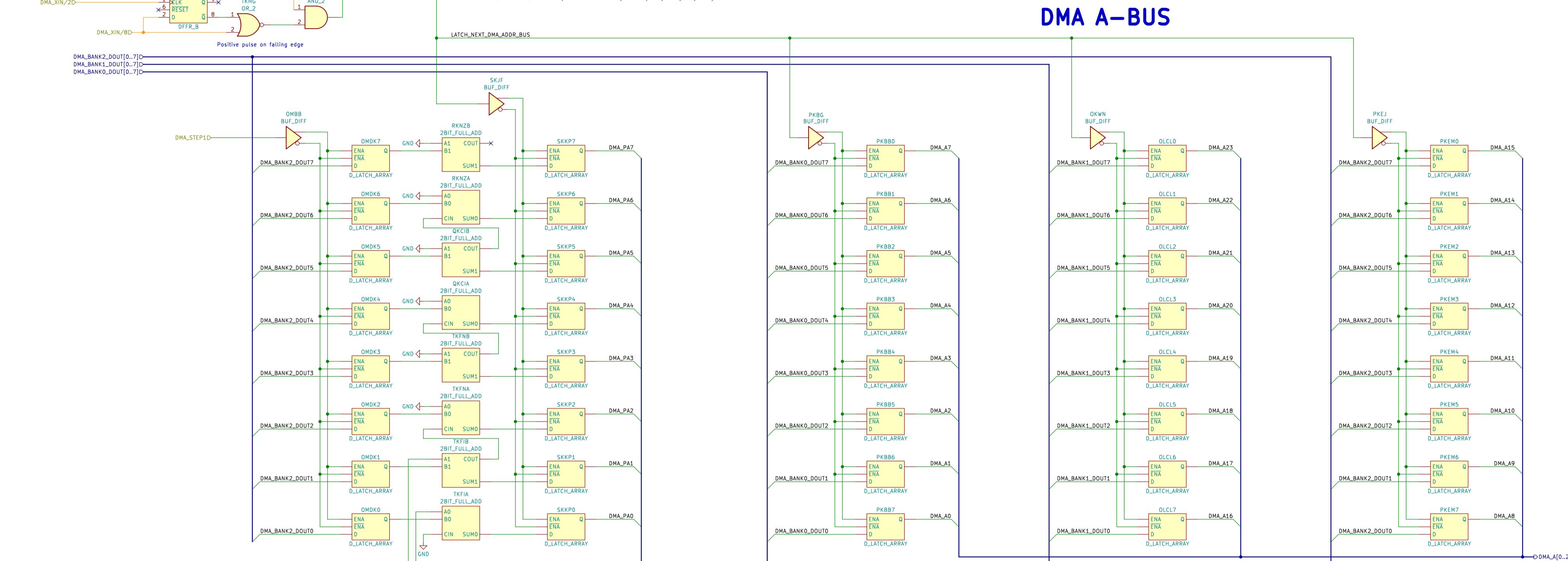
B-BUS offset based on pattern



DMA B-BUS

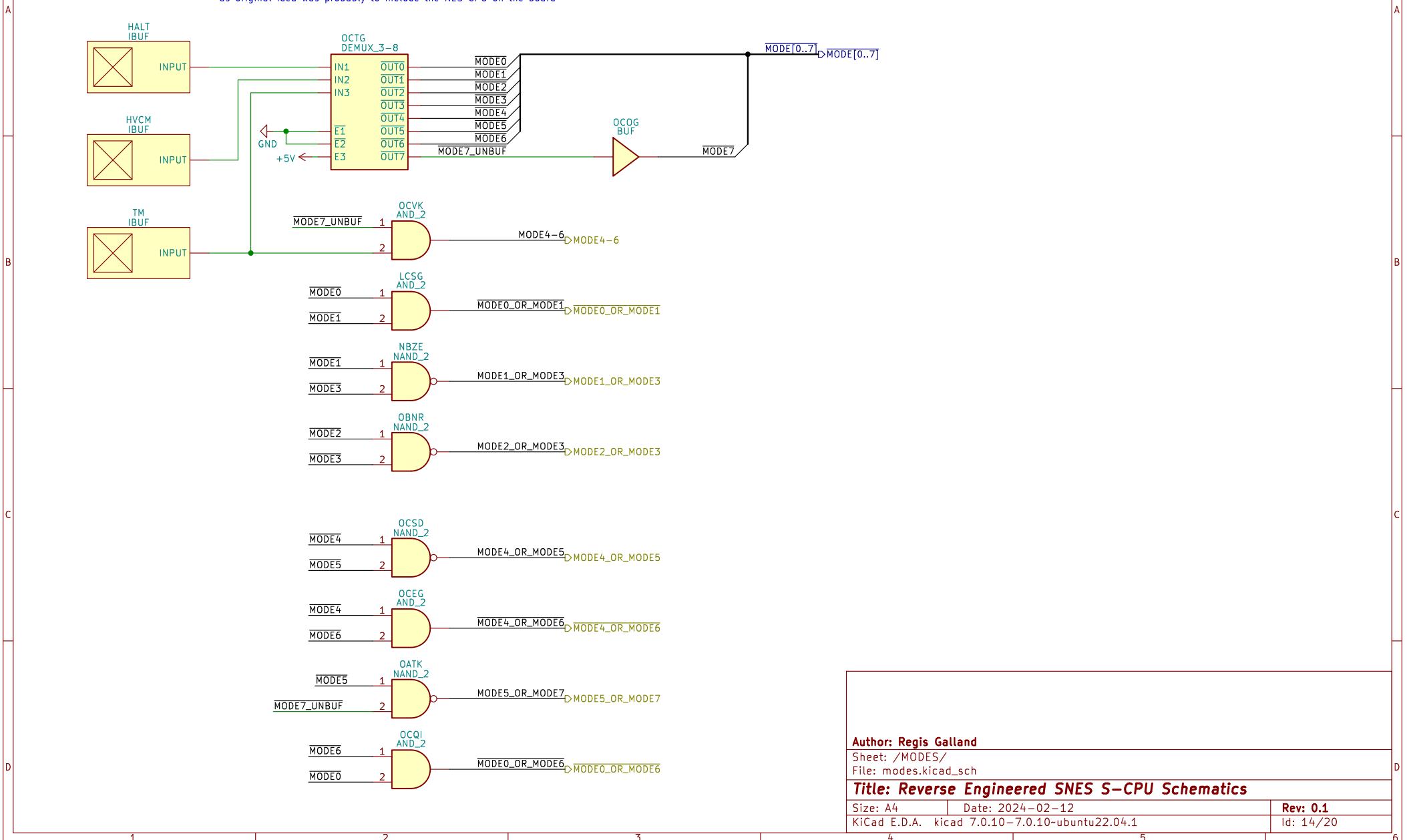


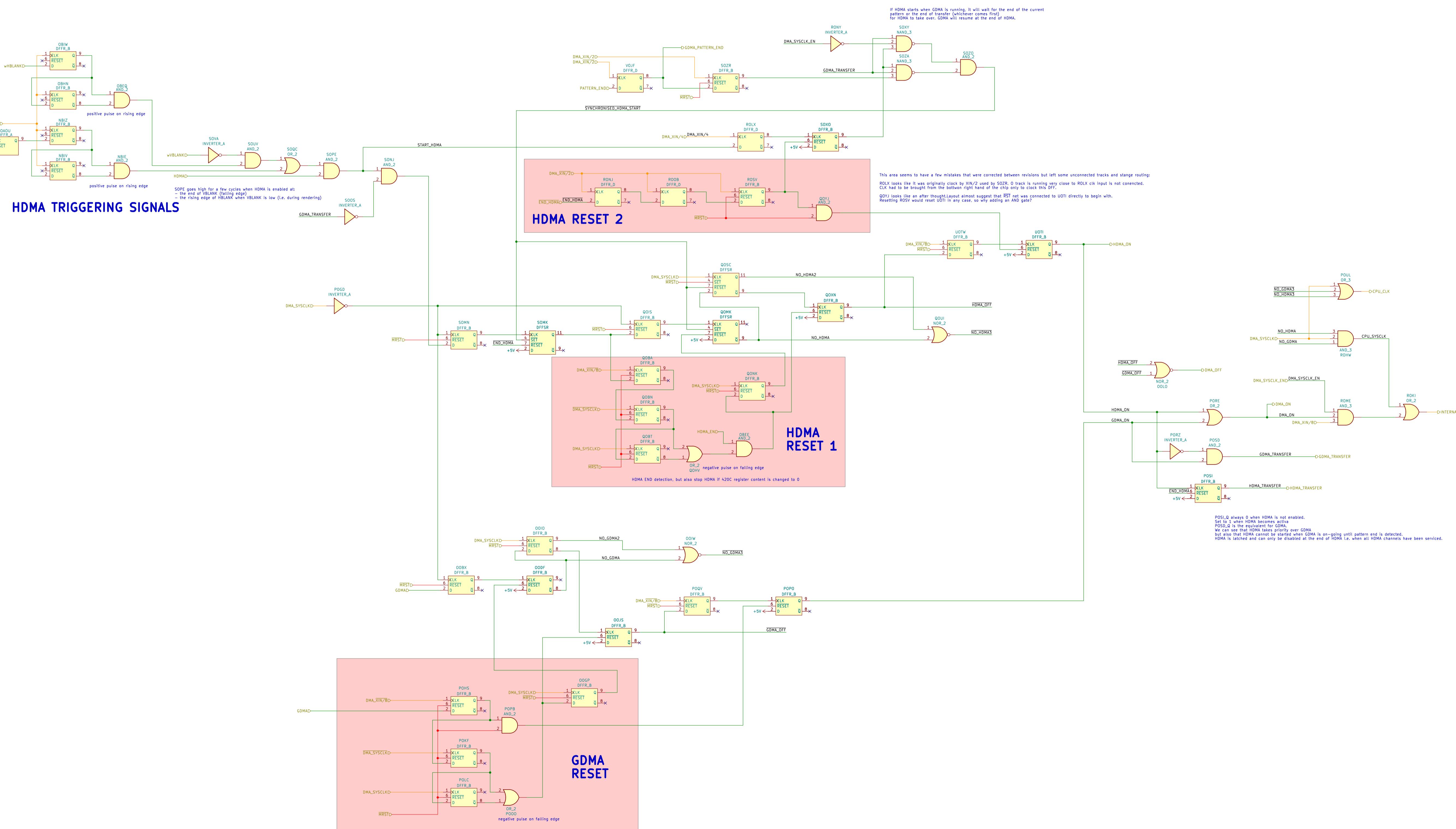
DMA A-BUS

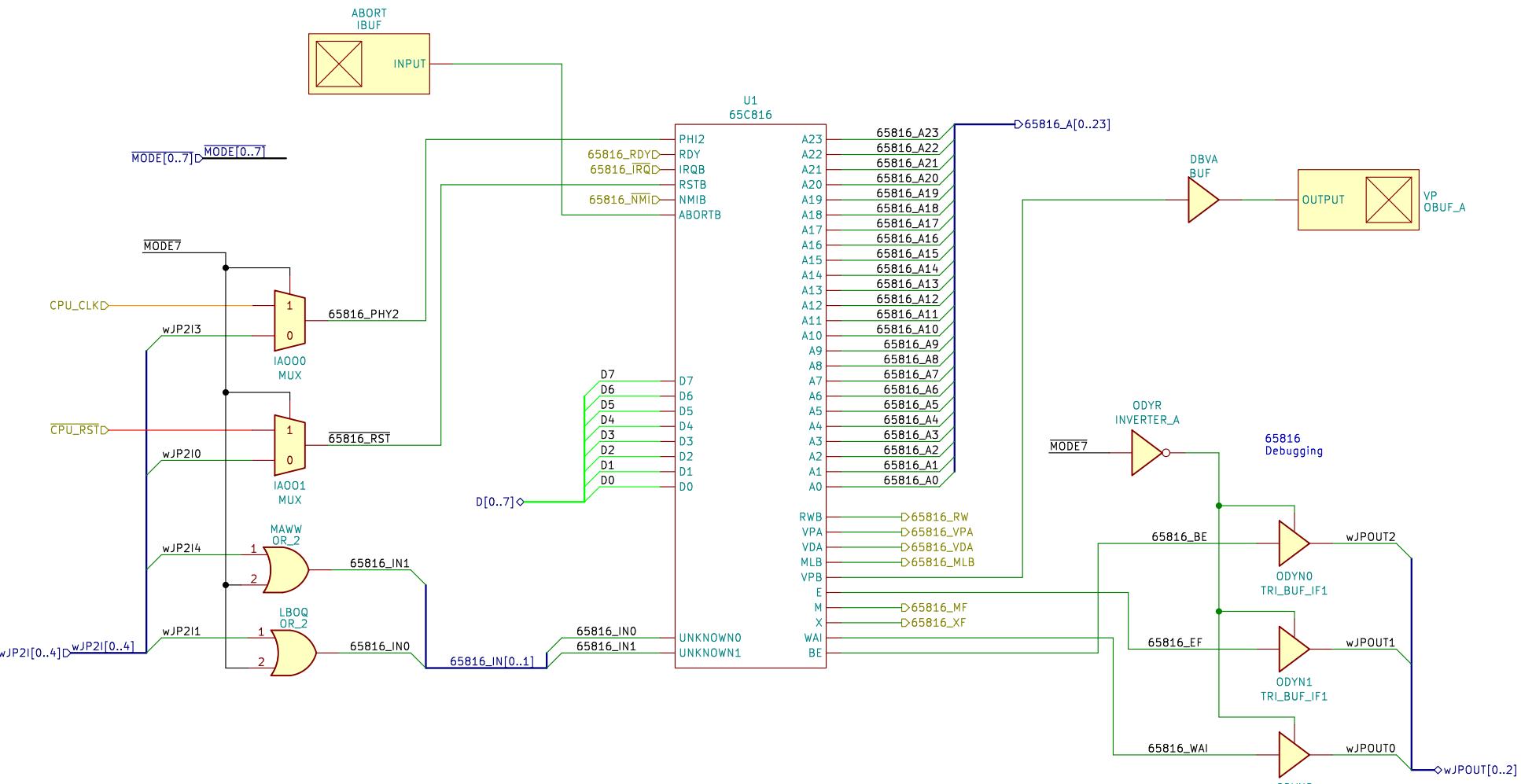


Modes are active low – inputs seems to be active low
 MODE7 = Test mode with external CPU connections bypassing 65816
 MODE4–6 = DMA test modes

MODE0 = SNES mode
 MODE1 = SNES in halt mode where RDY is used to pause the 65816
 MODE2–3 = NES modes where 4200–43FF registers are disabled and CPU connections are external
 as original idea was probably to include the NES CPU on the board







There 3 outputs which I guess must be:
 - Wait for interrupt output (multiplexed with RDY pin in W65C816 chip)
 - Emulation flag
 - Bus Enable (not needed as full 24-address bus is presented at all times)

Author: Regis Galland

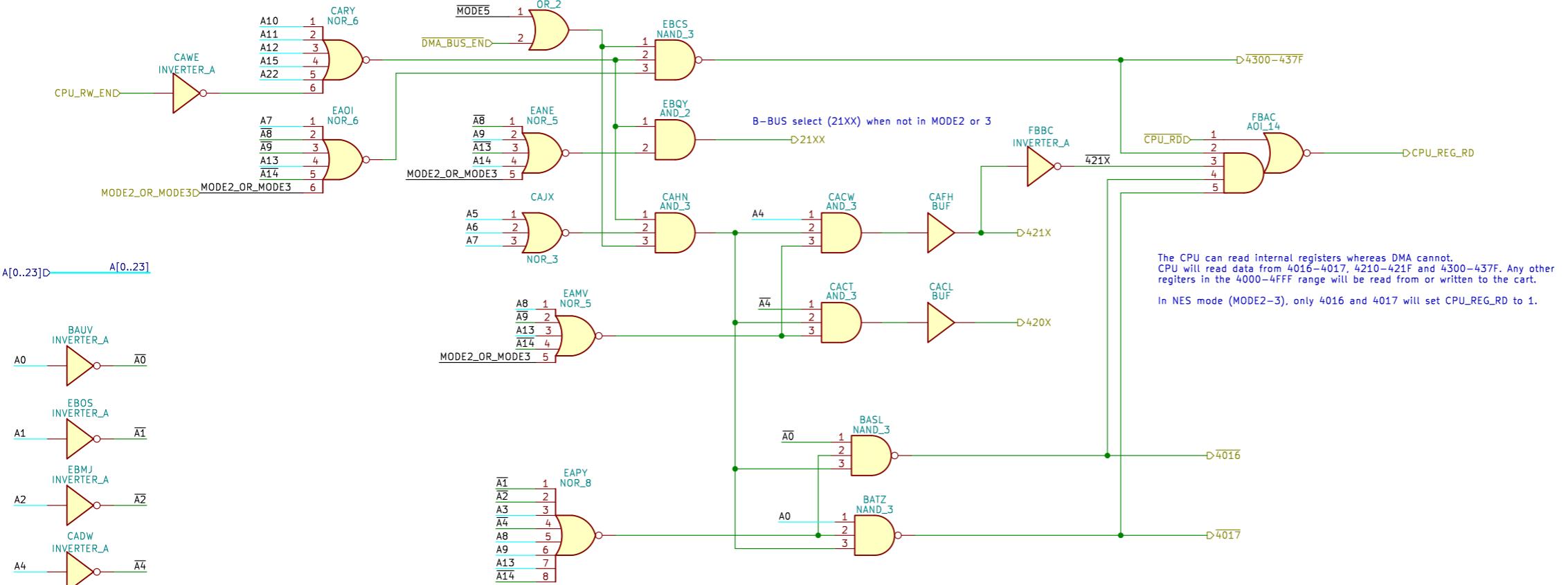
Sheet: /65C816 CPU/
File: 65c816.kicad_sch

Title: Reverse Engineered SNES S-CPU Schematics

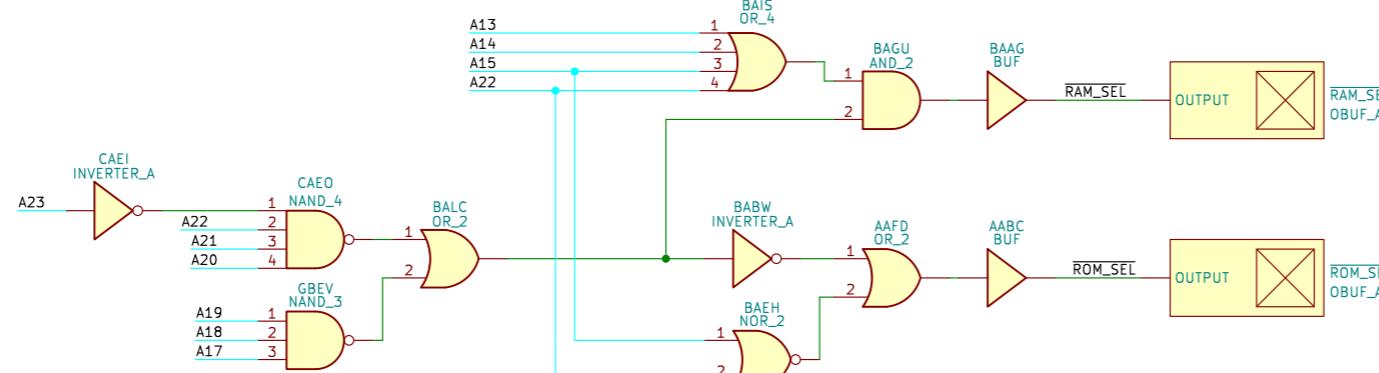
Size: A4 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1

Rev: 0.1
Id: 17/20

Address decoding



RAM and RAM Selection



ROMSEL = $\overline{A23} \cdot A22 \cdot A21 \cdot A20 \cdot A19 \cdot A18 \cdot A17 + A22 \cdot A15$
Consistent with access to:
- 00-3F/80-BF:8000-FFFF or
- 40-70/C0-FF:0000-FFFF

RAMSEL = $\overline{(A23 \cdot A22 \cdot A21 \cdot A20 \cdot A19 \cdot A18 \cdot A17 + A22 \cdot A15 \cdot A14 \cdot A13)}$
Consistent with access to:
- 00-3F/80-BF:0000-1FFF or
- 7E-7F:0000-FFFF

Author: Regis Galland

Sheet: /ADDRESS REGION DECODING/
File: addrdecod.kicad_sch

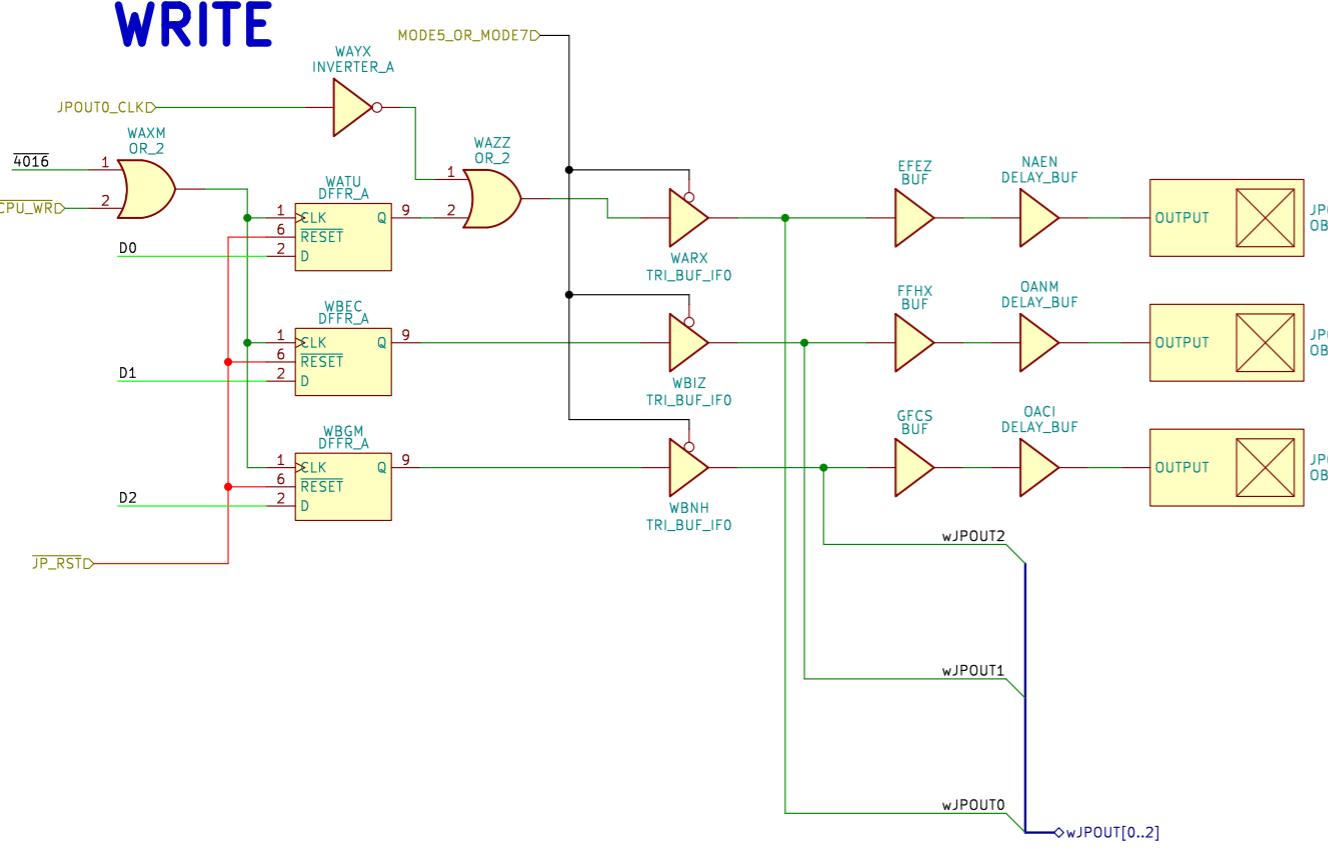
Title: Reverse Engineered SNES S-CPU Schematics

Size: A3 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

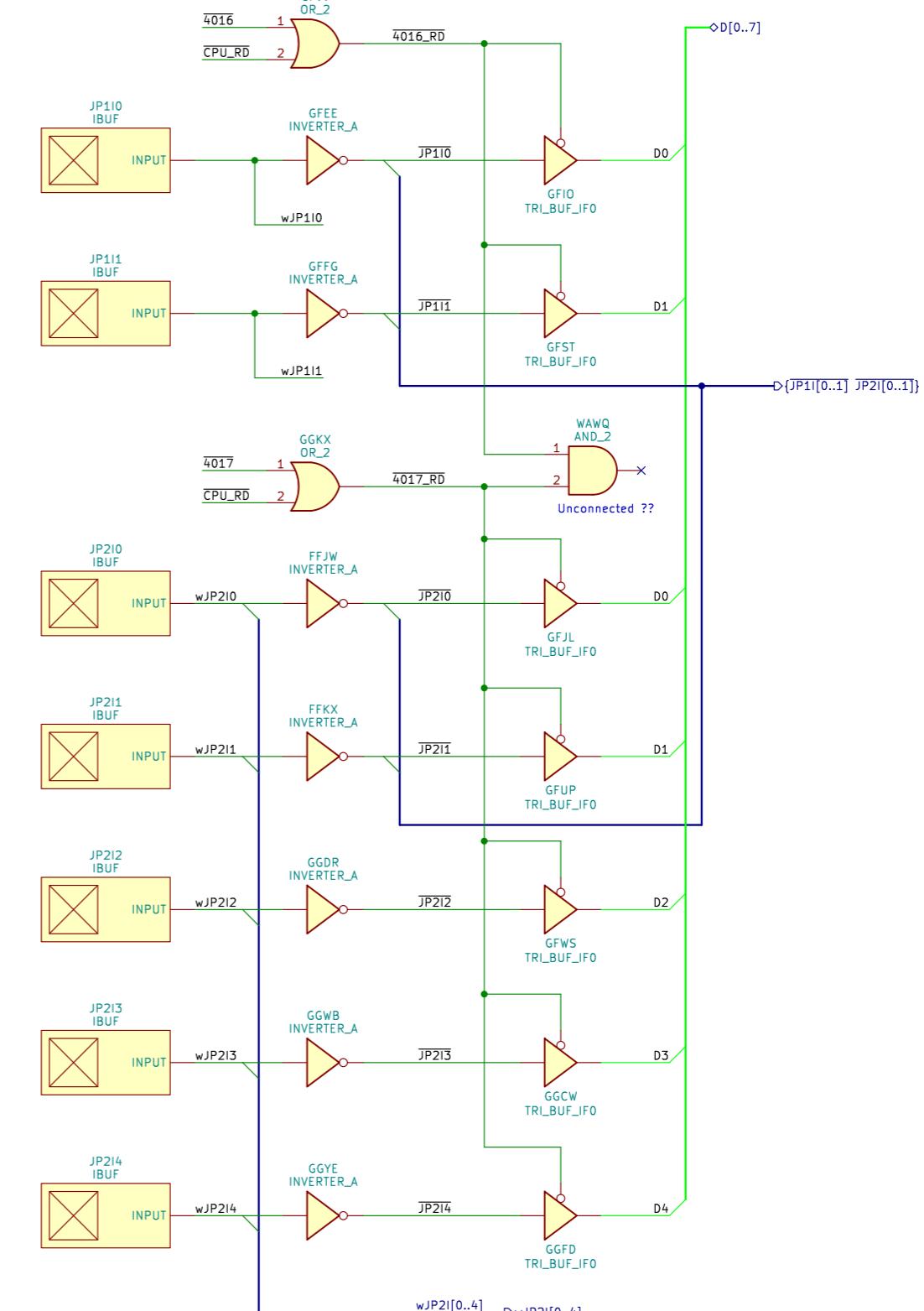
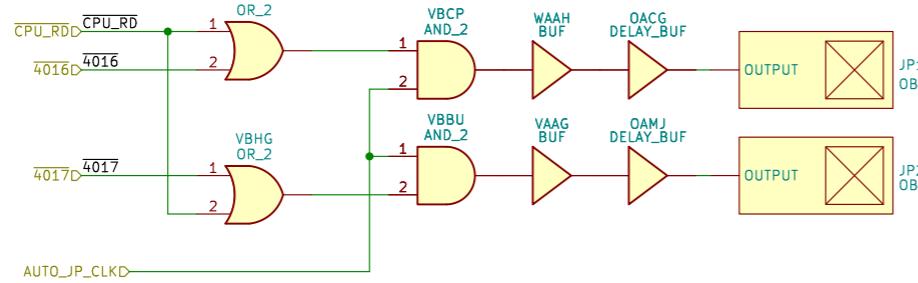
Rev: 0.1 Id: 18/20

4016/4017 READ

4016 WRITE



JPCLK: 4016/4017 READ OR SNES AUTO JP

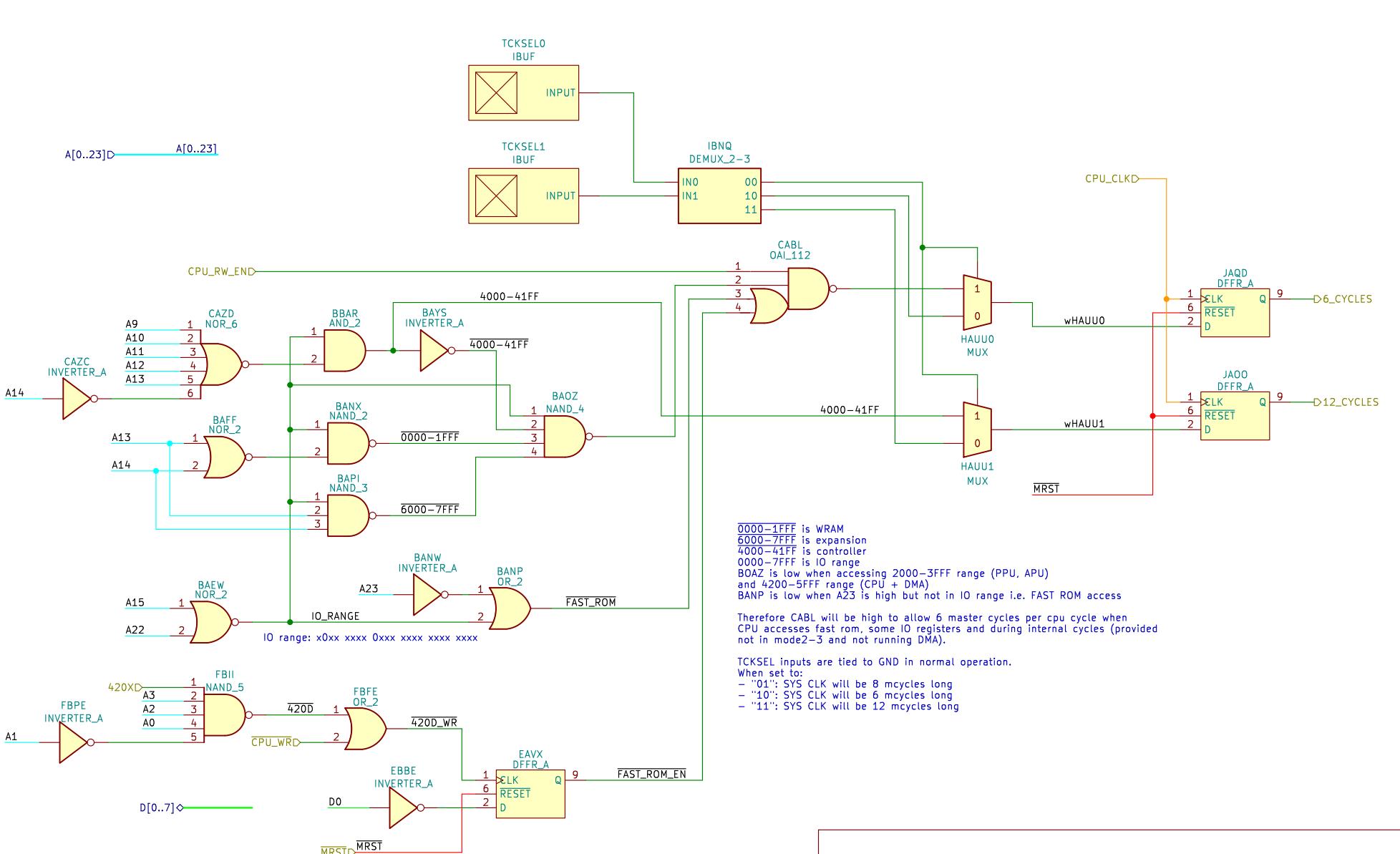


Author: Regis Galland
Sheet: /LEGACY JP REGISTERS/
File: legacyjpres.kicad_sch

Title: Reverse Engineered SNES S-CPU Schematics

Size: A3 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

Rev: 0.1
Id: 19/20



0000-1FFF is WRAM
 6000-7FFF is expansion
 4000-41FF is controller
 0000-7FFF is IO range
 BOAZ is low when accessing 2000-3FFF range (PPU, APU)
 and 4200-5FFF range (CPU + DMA)
 BANP is low when A23 is high but not in IO range i.e. FAST ROM access

Therefore CABL will be high to allow 6 master cycles per cpu cycle when CPU accesses fast rom, some IO registers and during internal cycles (provided not in mode2-3 and not running DMA).

TCKSEL inputs are tied to GND in normal operation.

When set to:

- "01": SYS CLK will be 8 mcycles long
- "10": SYS CLK will be 6 mcycles long
- "11": SYS CLK will be 12 mcycles long

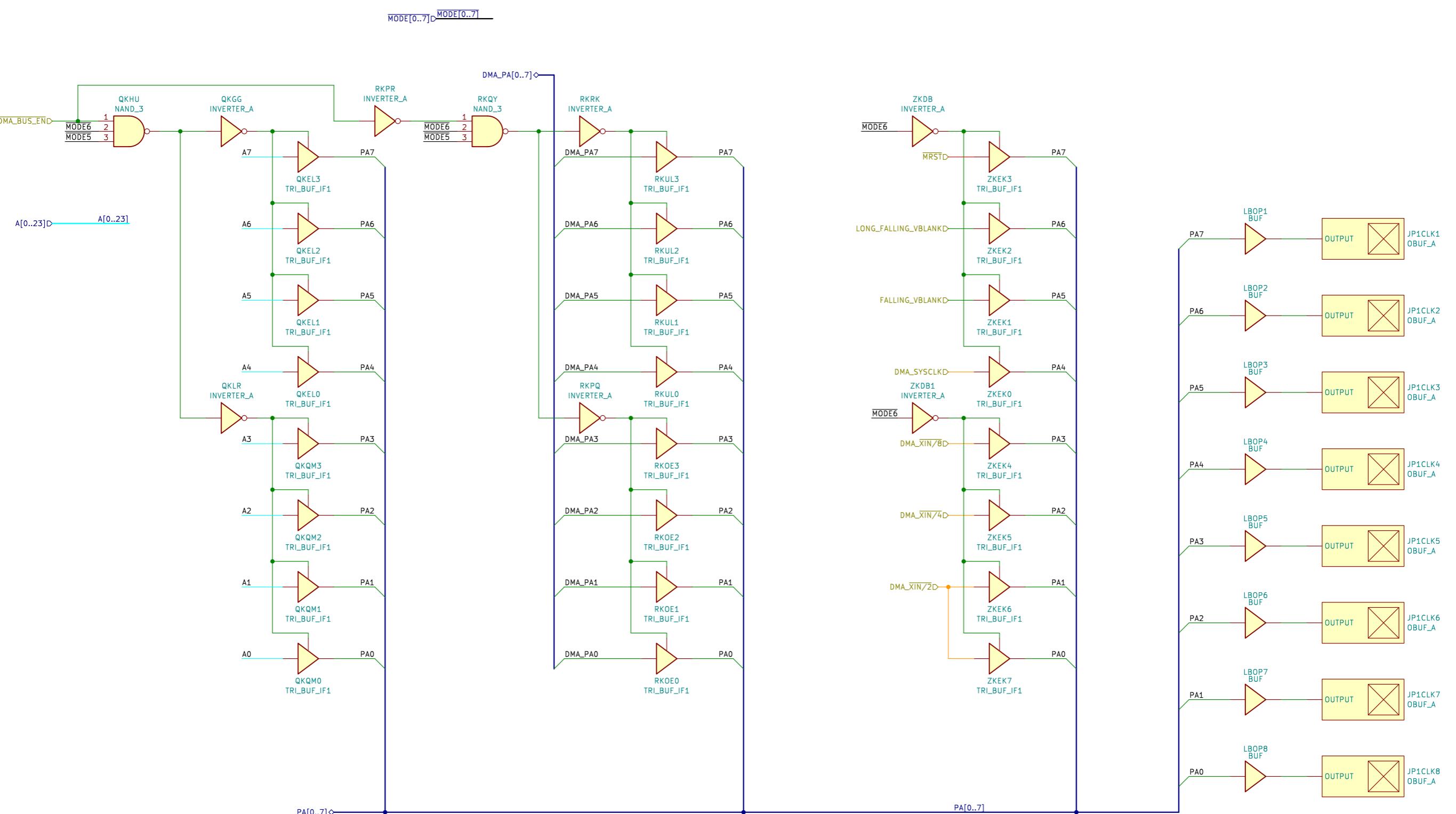
Author: Regis Galland

Sheet: /FAST ROM REG/
 File: fastromreg.kicad_sch

Title: Reverse Engineered SNES S-CPU Schematics

Size: A4 Date: 2024-02-12
 KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1

Rev: 0.1
 Id: 20/20



B-BUS and debug mode signals

Author: Regis Galland
Sheet: /DMA AND B-BUS/B-BUS/
File: bbus.kicad_sch

Title: Reverse Engineered SNES S-CPU Schematics

Size: A3 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

Rev: 0.1 Id: 21/20