

Giulio Luzzati, Ph.D.

PERSONAL INFORMATION

Research Software Engineer
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Born: 19/10/1984, Genova, Italy

IN A NUTSHELL

I am a software engineer with a strong scientific background. My drive is to design and analyse things and mechanisms, understand what makes them tick and how they could be better. I strive to frame my projects within the bigger picture, and I have a track record of delivering solid, dependable, and (re)usable solutions.

EDUCATION

University of Genova, Genova, Italy

Ph.D. in Computer Science

Apr 2016

Thesis topics: resource allocation, communication networks, signal processing

Professional Engineering Qualification

Oct 2012

M.Sc. in Telecommunication Engineering

May 2012

PROFESSIONAL AND ACADEMIC EXPERIENCE

Cambridge Touch Technologies (CTT), Cambridge, United Kingdom

Senior DSP Engineer

Oct 2018 - Current

CTT is a touch screen technology startup, providing cost effective and minimal overhead ways to add pressure sensing capabilities to touchscreen technologies. At CTT I'm in charge of designing and realizing several projects and tools to diagnose, test and benchmark components of the hardware stack. Given my experience in software engineering, I was also tasked with the rearchitecturing of the company's software versioning and CI infrastructure.

5G Innovation Centre, Guildford, United Kingdom

Senior Software Engineer

Nov 2017 - Oct 2018

The 5GIC is a research centre within the University of Surrey, featuring one of the biggest 5G testbeds in the UK and carrying on research and standardization activity in close partnership with some of the largest players in the field. The 5GIC's testbed, a complete cellular network, showcases several research ideas, from the physical layer to network concepts. At the 5GIC I was part of the core network team. My contribution as a software engineer was to develop and maintain the code base for the core network.

AKYA Ltd, Swindon, United Kingdom

DSP Software Engineer

Dec 2016 - Nov 2017

AKYA's core business was a novel "dynamically reconfigurable logic" approach to hardware design, for low power/low cost applications, unlike e.g. FPGA, providing "just enough" reconfigurability to meet design requirements. At AKYA I contributed as a software engineer to the codebase of a framework to synthesise logic from a high-level description of the hardware. My role was to design and develop algorithms and software components that expand and integrate the existing framework, as well as creating tools for testing and data visualization.

DSP Lab, University of Genova, Genova, Italy

Post Doctoral Research Fellow

Jan 2016 - Nov 2016

Ph.D. Student

Jan 2013 - Dec 2015

Research Fellow

Oct 2012 - Dec 2012

During my academic experience at the DSP Labs, as Ph.D. student and then research fellow, I carried out academic (research and teaching) activity, along with projects in collaboration with SMEs and some of the key industries of Italy's communications and tech (Telecom Italia, Leonardo). My main area of research were resource allocation and mathematical optimization in communication networks and in signal processing

TECHNICAL SKILLS

C++ ●●● C ●●●
Python ●●● Matlab ●●●
Latex ●●● Java ●●●

Software Architecture Build Systems CI, DevOps
Containerization Embedded Programming Basic Hardware Diagnostics
Service Oriented Architecture Agile Software Development GNU/Linux OS

SCIENTIFIC SKILLS

Signal processing
Computer networks
Statistics, data science
Mathematical optimization
Working knowledge in machine learning
Scientific writing and teaching

RELEVANT PROJECTS

Touch Model

Individual Project, Cambridge Touch Technologies

2020

A research on human touch interaction models, this project provided experimental data and insights to support and direct product and algorithm design decisions. I designed and prototyped the hardware and software needed to provide a generalized “experiment” platform, to collect touch force profiles for different use cases. The second part was focused on processing and analysing the gathered data, to refine insights from the aggregate. The outcome from this phase of the project is parametrized mathematical models for two basic interaction modes, that I devised from curve fitting in one case, and deriving from first principles in the other. Such parametrized models can be now used to drive a more refined design process and as more “human-like” profiles for test machines.

Signal Injector for Pressure Sensors

Project manager, Cambridge Touch Technologies

2019

The goal of the project was to realize a signal injector, able to “simulate” the behaviour of the physical sensor. An array of DACs at its core, the deliverable consisted in a small box, controlled via REST api, able to physically interface to the pressure sensor amplifier. My role in the project:

- specified the requirements
- designed the high level architecture
- implemented driver, API
- integration (as slave component) with other existing diagnostic tools

The tool proved to be useful and usable, and after the prototype, several units of the tool have been commissioned and are in use by the hardware team.

Touchscreen Analyser

Project Manager, Cambridge Touch Technologies

2019

This tool was aimed at diagnosing manufacturing defects of pressure sensing enabled touch panels. The scope of the project was to harness existing experiments and components in the company, and integrate them organically into a usable tool. The instrument analyses the electrodes of capacitive touch panels, and automatically generates easy to read reports containing physical measures and inferred features.

My role in the project:

- designed the flow of operations, data format and structures, and system level architecture
- coded most of the software and the GUI
- designed and coded signal and data processing algorithms (feature extraction, classification)
- automated report generation (Latex)

The tool as a proof of concept has sparked the interest of the management and its second iteration is now in design.

Quick Http Messages

Individual Project, 5GIC

2018

This project was a proof of concept to provide a barebone, simple playground to test ideas and allow quick prototyping in HTTP service based architectures (SbA), such as the 5G core network. The core idea was to implement a simple HTTP server over bare UDP, to minimize latency. The C++ source code for this project is available at <https://github.com/giulio1/quick-http-messages>. As one-man project, I designed and implemented the entire system. Additionally, I realized a simple automatic generator tool, able to parse 3GPP OpenAPI compliant YML definitions of components in the 5G SbA and generate stubs for their REST APIs.