Single and Dual, Ultralow Distortion, Ultralow Noise Op Amps

Data Sheet

AD8597/AD8599

FEATURES

Low noise: 1.1 nV/√Hz at 1 kHz
Low distortion: −120 dB THD at 1 kHz
Input noise, 0.1 Hz to 10 Hz: <76 nV p-p
Slew rate: 14 V/µs
Wide bandwidth: 10 MHz
Supply current: 4.8 mA/amp typical
Low offset voltage: 10 µV typical
CMRR: 120 dB
Unity-gain stable
±15 V operation

APPLICATIONS

Professional audio preamplifiers
ATE/precision testers
Imaging systems
Medical/physiological measurements
Precision detectors/instruments
Precision data conversion

PIN CONFIGURATIONS

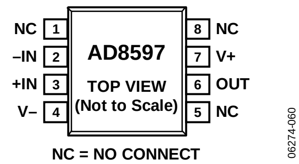

Figure 1. AD8597 8-Lead SOIC (R-8)

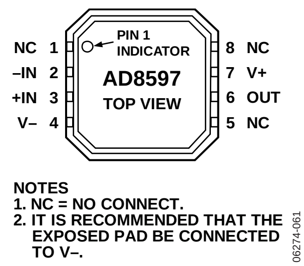

Figure 2. AD8597 8-Lead LFCSP (CP-8-2)

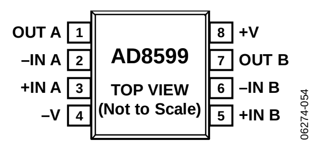

Figure 3. AD8599 8-Lead SOIC (R-8)

GENERAL DESCRIPTION

The AD8597/AD8599 are very low noise, low distortion operational amplifiers ideal for use as preamplifiers. The low noise of 1.1 nV/√Hz and low harmonic distortion of −120 dB (or better) at audio bandwidths give the AD8597/AD8599 the wide dynamic range necessary for preamplifiers in audio, medical, and instrumentation applications. The excellent slew rate of 14 V/µs and 10 MHz gain bandwidth make them highly suitable for medical applications. The low distortion and fast settling time make them ideal for buffering of high resolution data converters.

The AD8597 is available in 8-lead SOIC and LFCSP packages, while the AD8599 is available in an 8-lead SOIC package. They are both specified over a −40°C to +125°C temperature range. The AD8597 and AD8599 are members of a growing series of low noise op amps offered by Analog Devices, Inc. (see Table 1).

Table 1. Low Noise Op Amps

Package	0.9 nV	1.1 nV	1.8 nV	2.8 nV	3.8 nV
Single	AD797	AD8597	ADA4004-1	AD8675	AD8671
Dual		AD8599	ADA4004-2	AD8676	AD8672
Quad			ADA4004-4		AD8674

Rev. E
Document Feedback

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12/09—Rev. B to Rev. C

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10/08—Rev. A to Rev. B

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2/07—Revision 0: Initial Version

SPECIFICATIONS

V_{SY} = ±5 V, V_{CM} = 0 V, V_O = 0 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			15	120	µV
		−40°C ≤ T_A ≤ +125°C			180	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.8	2.2	µV/°C
Input Bias Current	I_B			40	210	nA
		−40°C ≤ T_A ≤ +125°C			340	nA
Input Offset Current	I_{OS}			65	250	nA
		−40°C ≤ T_A ≤ +125°C			340	nA
Input Voltage Range	IVR		−2.0		+2.0	V
Common-Mode Rejection Ratio	CMRR	−2.0 V ≤ V_{CM} ≤ +2.0 V	120	135		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 600 Ω, V_O = −11 V to +11 V	105	110		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Input Capacitance						
Differential Capacitance	C_{DIFF}			15.4		pF
Common-Mode Capacitance	C_{CM}			5.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 600 Ω	3.5	3.7		V
		−40°C ≤ T_A ≤ +125°C	3.3			V
		R_L = 2 kΩ	3.7	3.8		V
		−40°C ≤ T_A ≤ +125°C	3.5			V
Output Voltage Low	V_{OL}	R_L = 600 Ω		−3.6	−3.4	V
		−40°C ≤ T_A ≤ +125°C			−3.3	V
		R_L = 2 kΩ		−3.7	−3.5	V
		−40°C ≤ T_A ≤ +125°C			−3.4	V
Output Short-Circuit Current	I_{SC}			±52		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, A_V = 1		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±18 V to ±4.5 V	120	140		dB
		−40°C ≤ T_A ≤ +125°C	118			dB
Supply Current per Amplifier	I_{SY}			4.8	5.5	mA
		−40°C ≤ T_A ≤ +125°C			6.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	A_V = −1, R_L = 2 kΩ		14		V/µs
		A_V = 1, R_L = 2 kΩ		14		V/µs
Settling Time	t_S	To 0.01%, step = 10 V		2		µs
Gain Bandwidth Product	GBP			10		MHz
Phase Margin	Φ_M			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		76		nV p-p
Voltage Noise Density	e_n	f = 1 kHz		1.07	1.15	nV/√Hz
		f = 10 Hz			1.5	nV/√Hz
Correlated Current Noise		f = 1 kHz		2.0		pA/√Hz
		f = 10 Hz		4.2		pA/√Hz
Uncorrelated Current Noise		f = 1 kHz		2.4		pA/√Hz
		f = 10 Hz		5.2		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	G = 1, R_L ≥ 1 kΩ, f = 1 kHz, V_{RMS} = 1 V		−120		dB
Channel Separation	CS	f = 10 kHz		−120		dB

$V_S = \pm15$ V, $V_{CM} = 0$ V, $V_O = 0$ V, $T_A = +25°C$, unless otherwise specified.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			10	120	µV
		$-40°C \le T_A \le +125°C$			180	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40°C \le T_A \le +125°C$		0.8	2.2	µV/°C
Input Bias Current	I_B			25	200	nA
		$-40°C \le T_A \le +125°C$			300	nA
Input Offset Current	I_{OS}			50	200	nA
		$-40°C \le T_A \le +125°C$			300	nA
Input Voltage Range	IVR		−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	$-12.5\text{ V} \le V_{CM} \le +12.5\text{ V}$	120	135		dB
		$-40°C \le T_A \le +125°C$	115			dB
Large Signal Voltage Gain	A_{VO}	$R_L \ge 600\ \Omega$, $V_O = -11$ V to +11 V	110	116		dB
		$-40°C \le T_A \le +125°C$	106			dB
Input Capacitance						
Differential Capacitance	C_{DIFF}			12.1		pF
Common-Mode Capacitance	C_{CM}			5.1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 600\ \Omega$	13.1	13.4		V
		$-40°C \le T_A \le +125°C$	12.8			V
		$R_L = 2\text{ k}\Omega$	13.5	13.7		V
		$-40°C \le T_A \le +125°C$	13.2			V
Output Voltage Low	V_{OL}	$R_L = 600\ \Omega$		−13.2	−12.9	V
		$-40°C \le T_A \le +125°C$			−12.8	V
		$R_L = 2\text{ k}\Omega$		−13.5	−13.4	V
		$-40°C \le T_A \le +125°C$			−13.3	V
Output Short-Circuit Current	I_{SC}			±52		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, $A_V = 1$		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm18$ V to ±4.5 V	120	140		dB
		$-40°C \le T_A \le +125°C$	118			dB
Supply Current per Amplifier	I_{SY}			5.0	5.7	mA
		$-40°C \le T_A \le +125°C$			6.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$A_V = -1$, $R_L = 2\text{ k}\Omega$		16		V/µs
		$A_V = 1$, $R_L = 2\text{ k}\Omega$		15		V/µs
Settling Time	t_s	To 0.01%, step = 10 V		2		µs
Gain Bandwidth Product	GBP			10		MHz
Phase Margin	Φ_M			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		76		nV p-p
Voltage Noise Density	e_n	f = 1 kHz		1.07	1.15	nV/√Hz
		f = 10 Hz			1.5	nV/√Hz
Correlated Current Noise		f = 1 kHz		1.9		pA/√Hz
		f = 10 Hz		4.3		pA/√Hz
Uncorrelated Current Noise		f = 1 kHz		2.3		pA/√Hz
		f = 10 Hz		5.3		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	G = 1, $R_L \ge 1\text{ k}\Omega$, f = 1 kHz, $V_{RMS} = 3$ V		−120		dB
Channel Separation	CS	f = 10 kHz		−120		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$-V \leq V_{IN} \leq +V$
Differential Input Voltage[1]	±1 V
Output Short-Circuit to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C
Junction Temperature	150°C

[1] If the differential input voltage exceeds 1 V, limit the current to 5 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified with the device soldered on a circuit board with its exposed paddle soldered to a pad (if applicable) on a 4-layer JEDEC standard PCB with zero air flow.

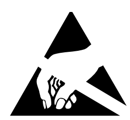
Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP_VD (CP-8-2)	78	20	°C/W
8-Lead SOIC (R-8) (AD8597)	140	39	°C/W
8-Lead SOIC (R-8) (AD8599)	120	36	°C/W

POWER SEQUENCING

Apply the op amp supplies simultaneously. The op amp supplies must be stable before any input signals are applied. In any case, the input current must be limited to 5 mA.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

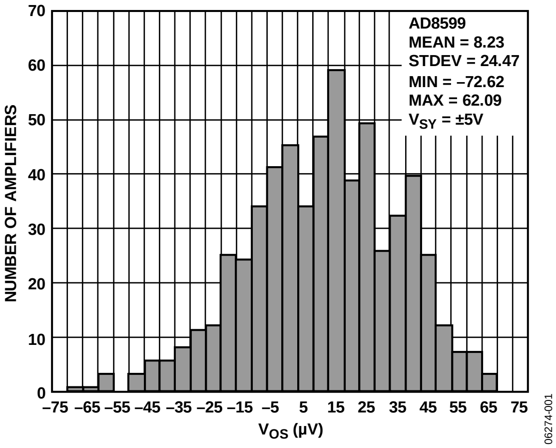


Figure 4. Input Offset Voltage Distribution

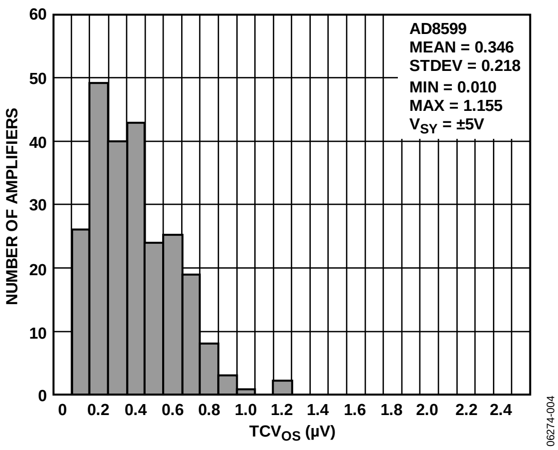


Figure 5. TCV_{OS} Distribution, −40°C ≤ T_A ≤ +125°C

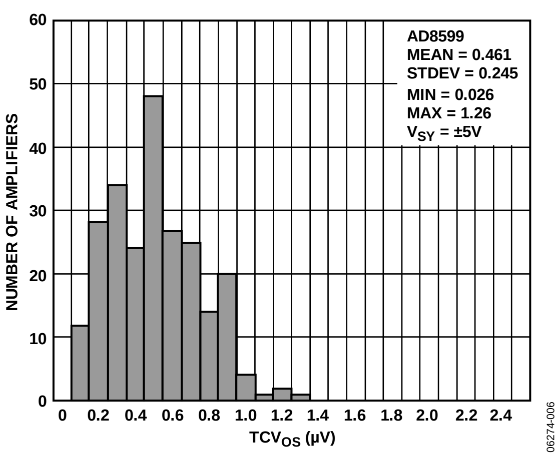


Figure 6. TCV_{OS} Distribution, −40°C ≤ T_A ≤ +85°C

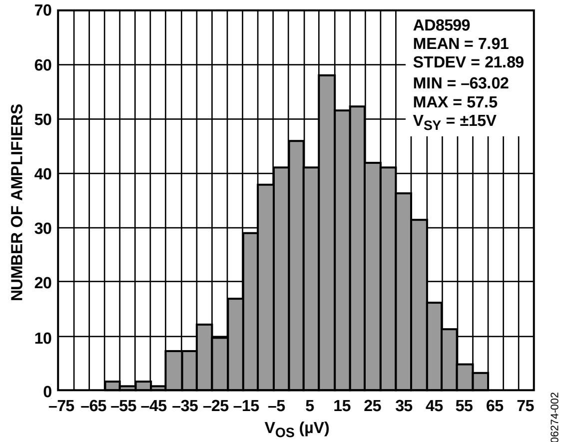


Figure 7. Input Offset Voltage Distribution

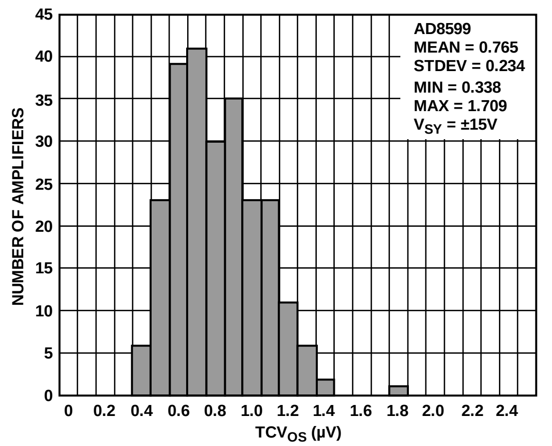


Figure 8. TCV_{OS} Distribution, −40°C ≤ T_A ≤ +125°C

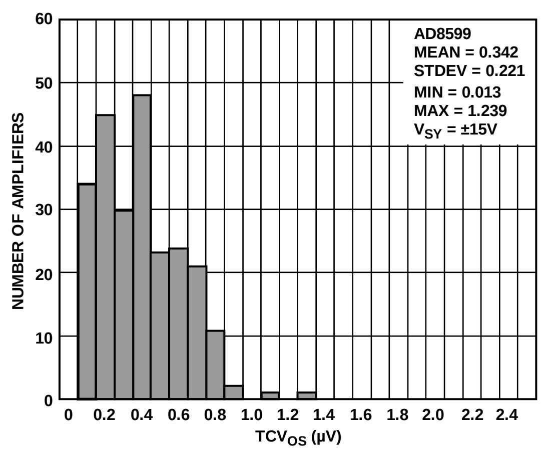


Figure 9. TCV_{OS} Distribution, −40°C ≤ T_A ≤ +85°C

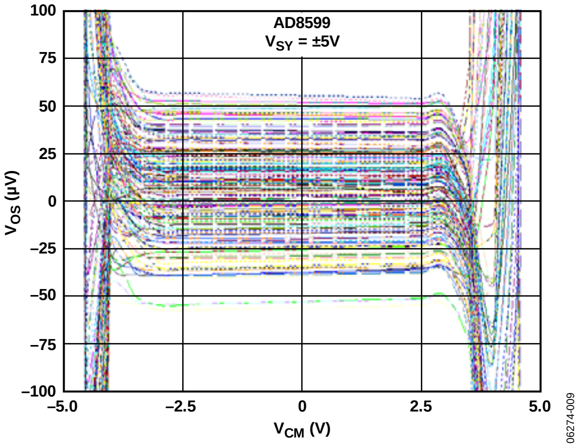


Figure 10. Offset Voltage vs. V_{CM}

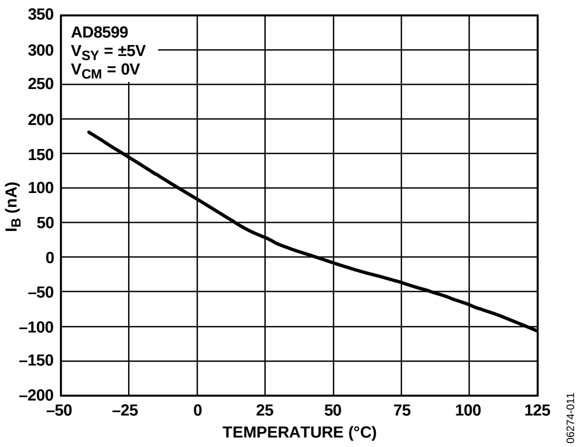


Figure 11. Input Bias Current vs. Temperature

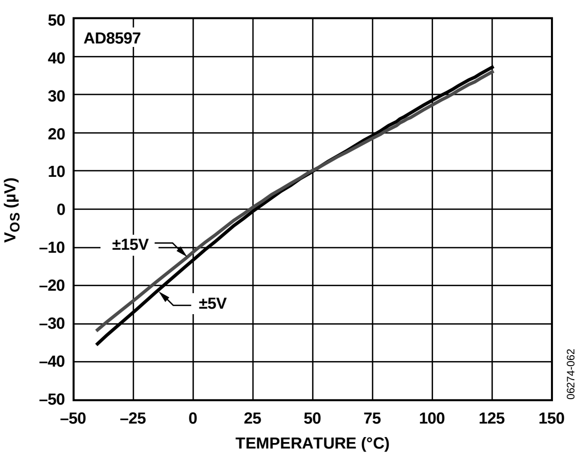


Figure 12. Input Offset Voltage vs. Temperature

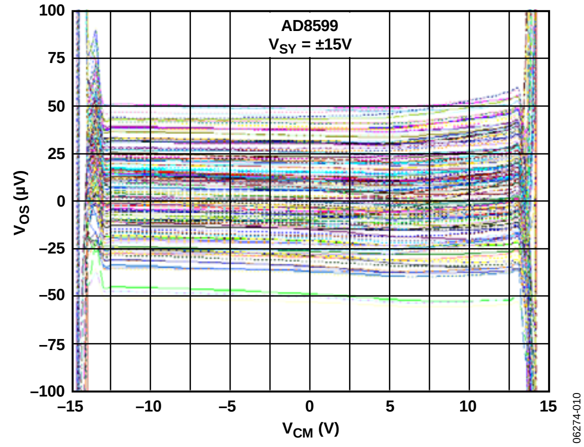


Figure 13. Offset Voltage vs. V_{CM}

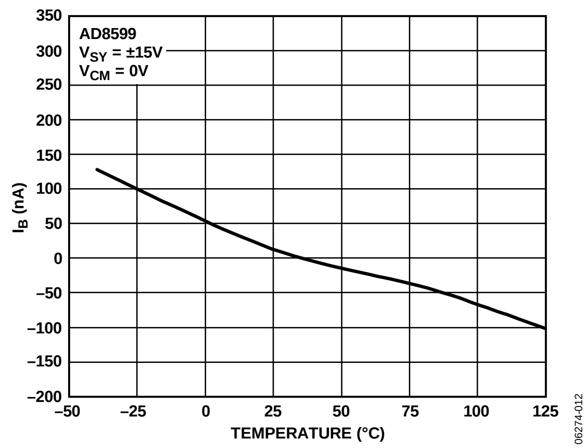


Figure 14. Input Bias Current vs. Temperature

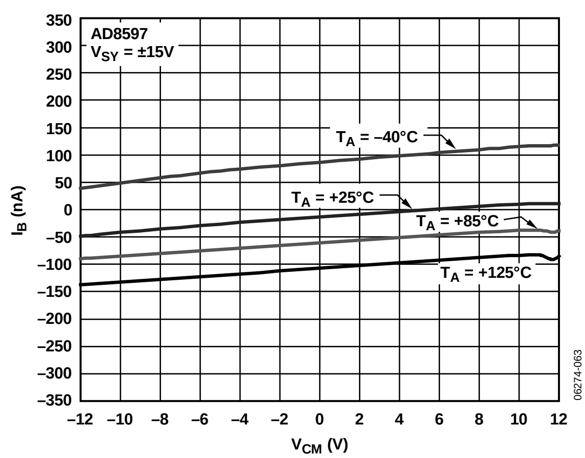


Figure 15. Input Bias Current vs. Common-Mode Voltage (V_{CM}) Over Temperature

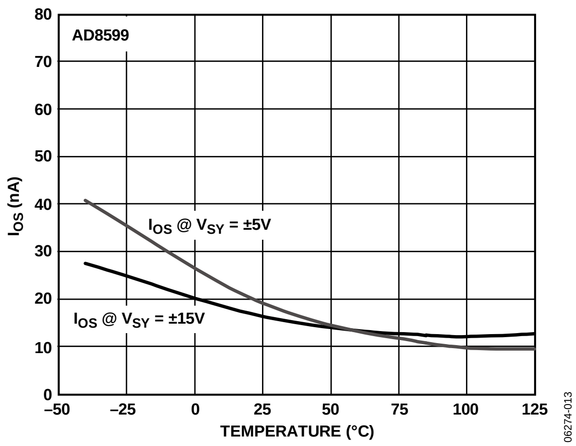


Figure 16. Input Offset Current vs. Temperature

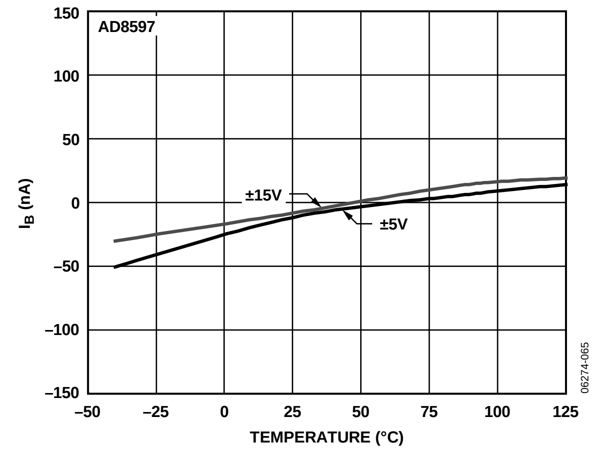


Figure 19. Input Offset Current vs. Temperature

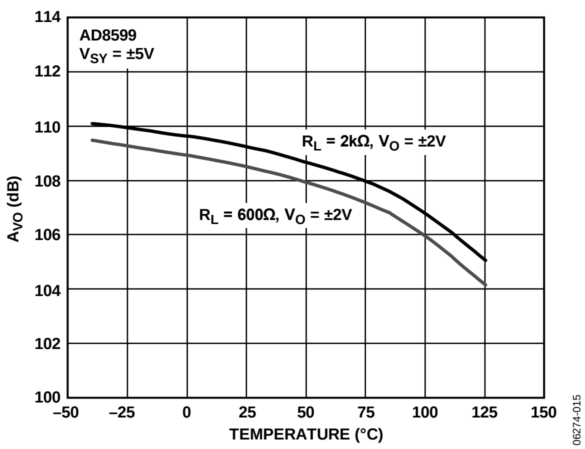


Figure 17. Large Signal Voltage Gain vs. Temperature

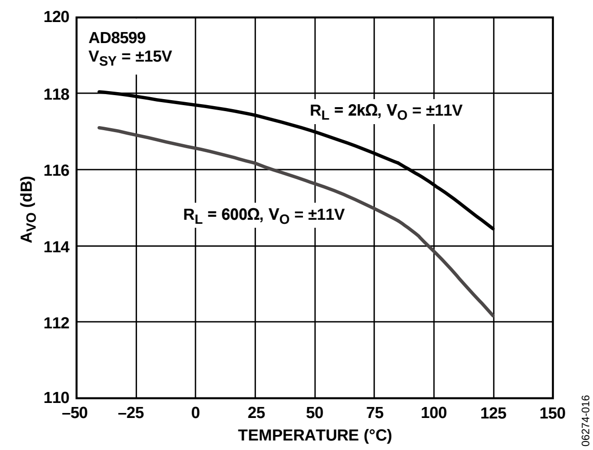


Figure 20. Large Signal Voltage Gain vs. Temperature

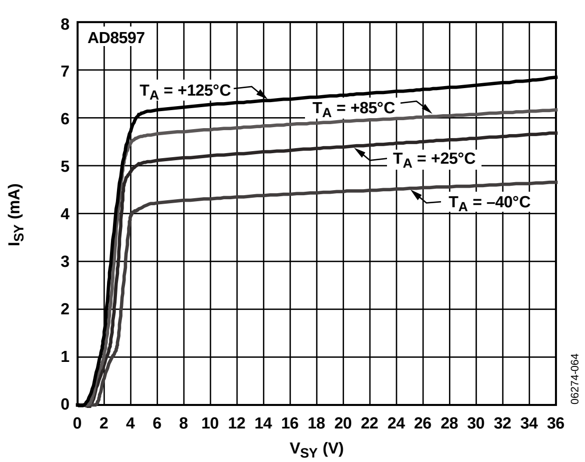


Figure 18. Supply Current vs. Supply Voltage

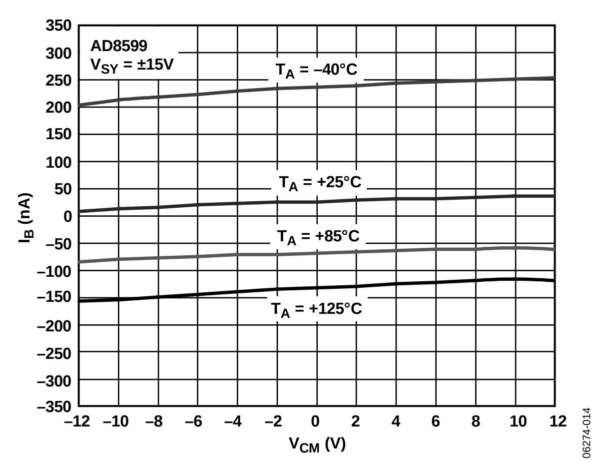


Figure 21. Input Bias Current vs. V_{CM}

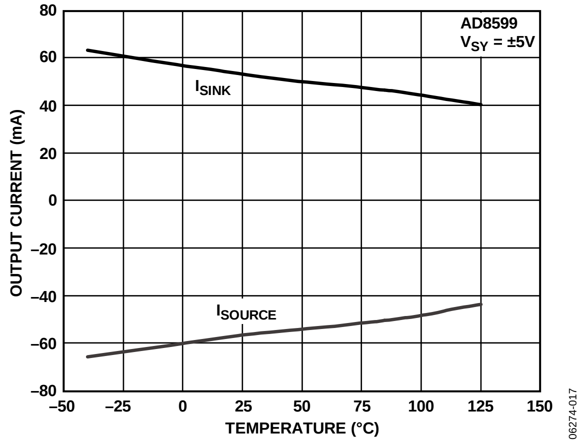


Figure 22. I_{SC} vs. Temperature

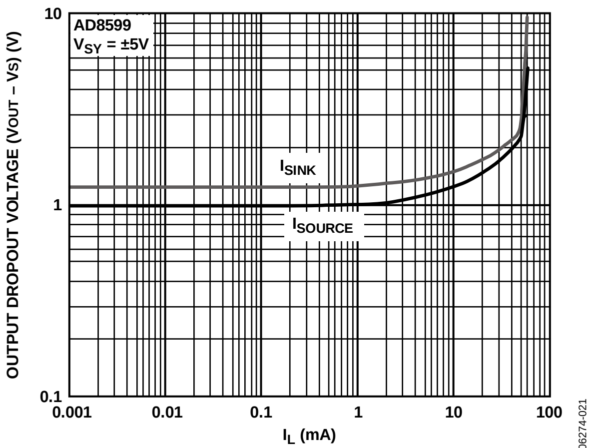


Figure 23. Output Dropout Voltage vs. Current Load

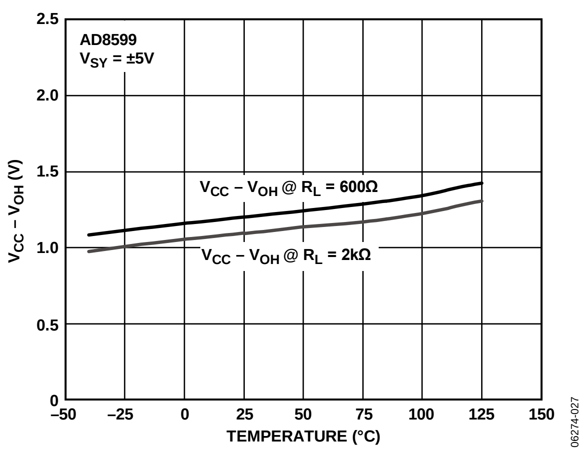


Figure 24. Output Saturation Voltage vs. Temperature

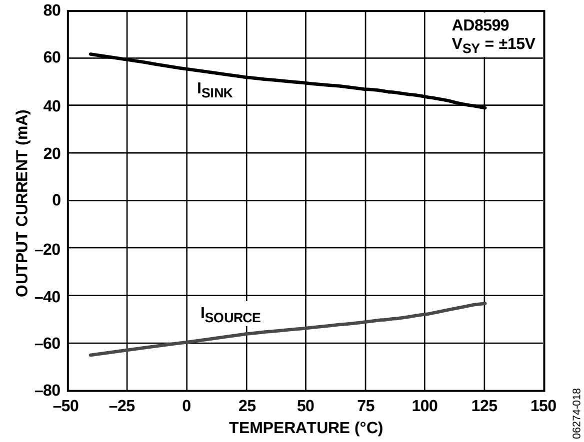


Figure 25. I_{SC} vs. Temperature

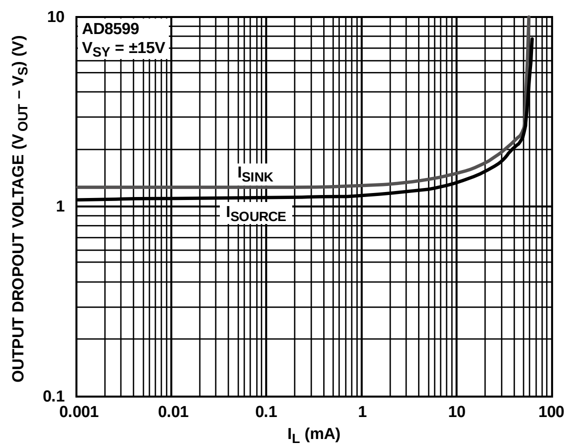


Figure 26. Output Dropout Voltage vs. Current Load

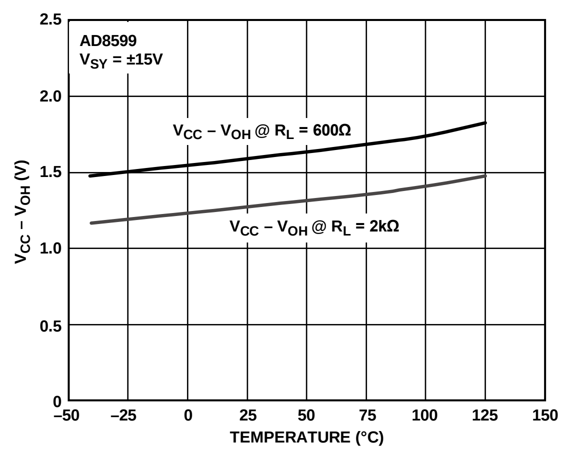


Figure 27. Output Saturation Voltage vs. Temperature

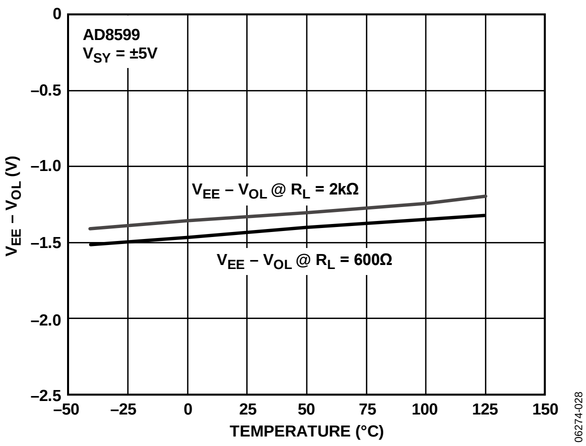


Figure 28. Output Saturation Voltage vs. Temperature

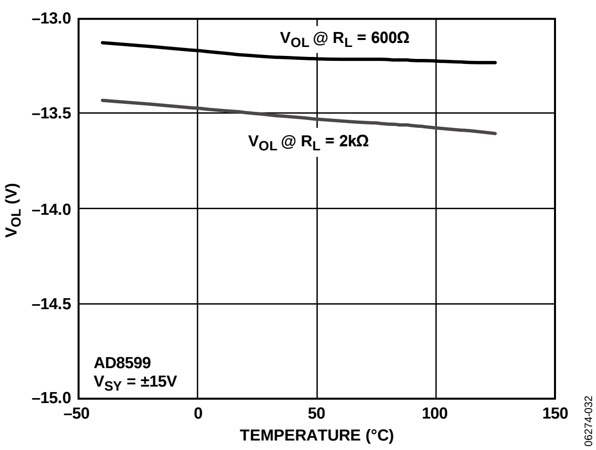


Figure 29. Output Voltage Low vs. Temperature

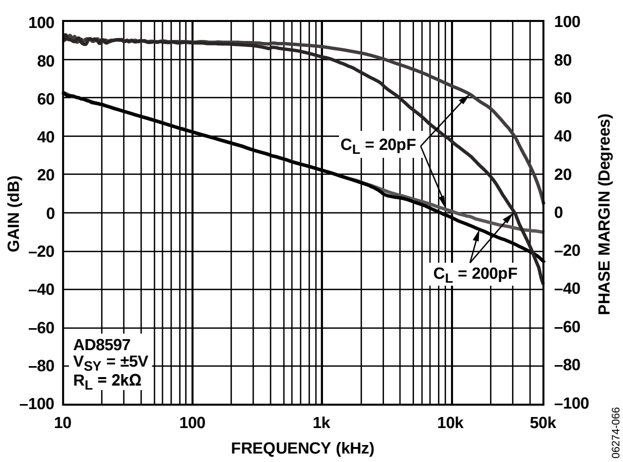


Figure 30. Gain and Phase vs. Frequency

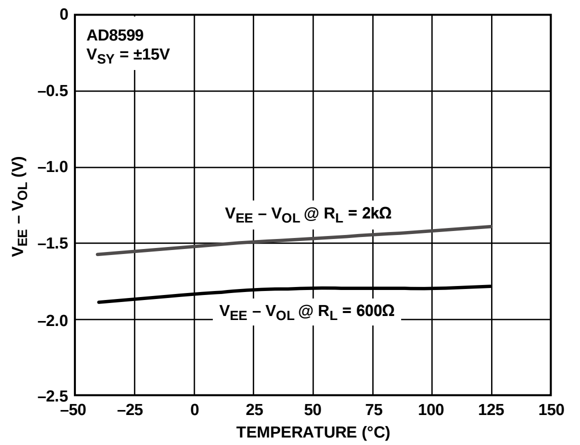


Figure 31. Output Saturation Voltage vs. Temperature

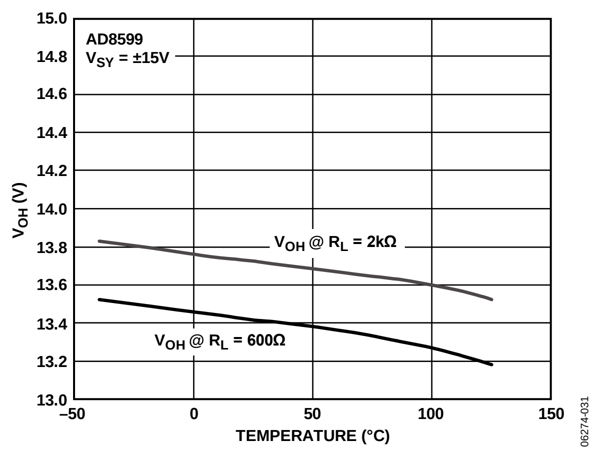


Figure 32. Output Voltage High vs. Temperature

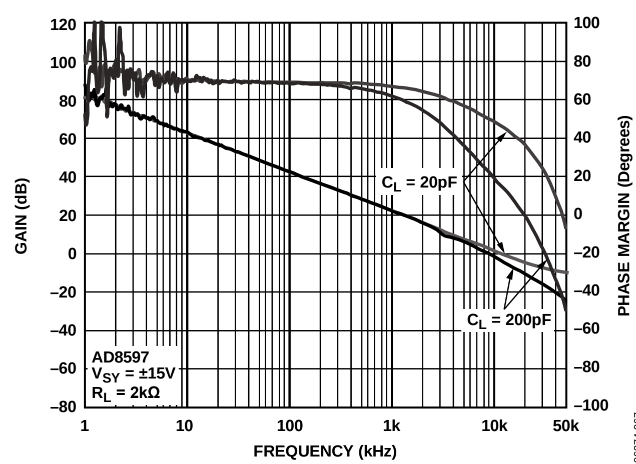


Figure 33. Gain and Phase vs. Frequency

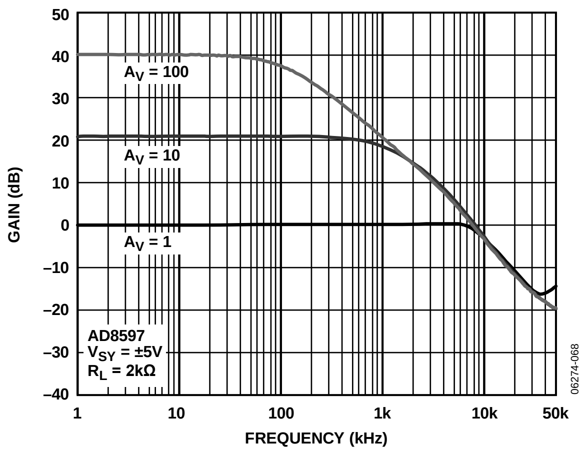


Figure 34. Closed-Loop Gain vs. Frequency

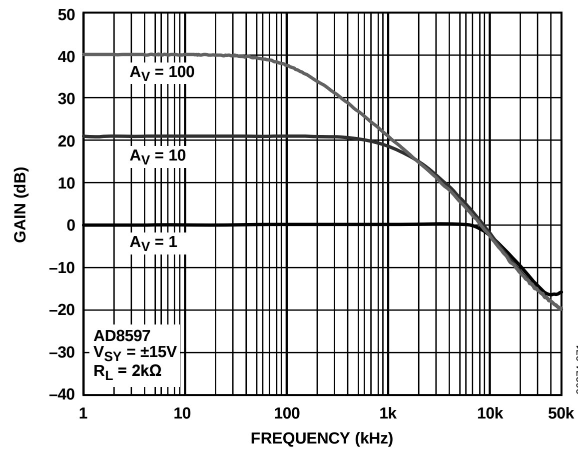


Figure 37. Closed-Loop Gain vs. Frequency

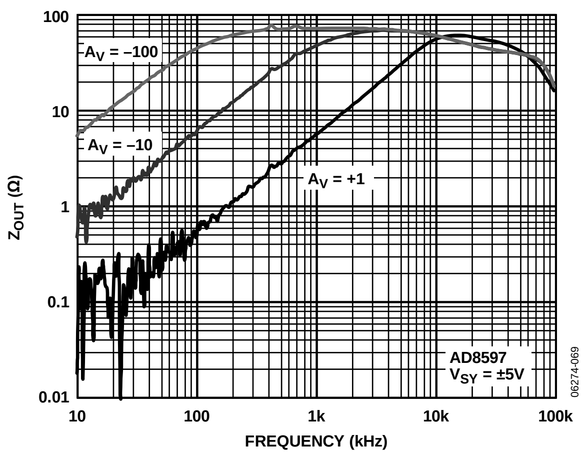


Figure 35. Closed-Loop Output Impedance vs. Frequency

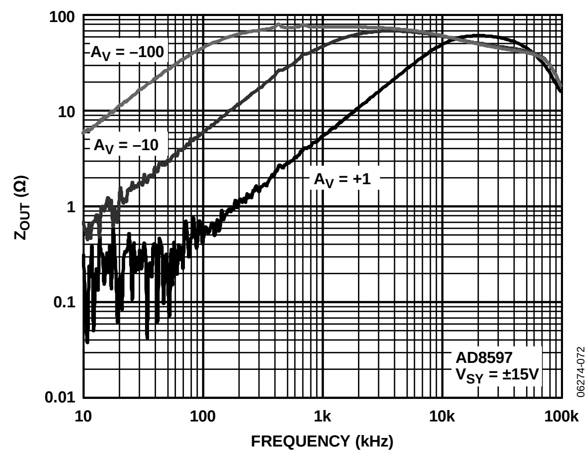


Figure 38. Closed-Loop Output Impedance vs. Frequency

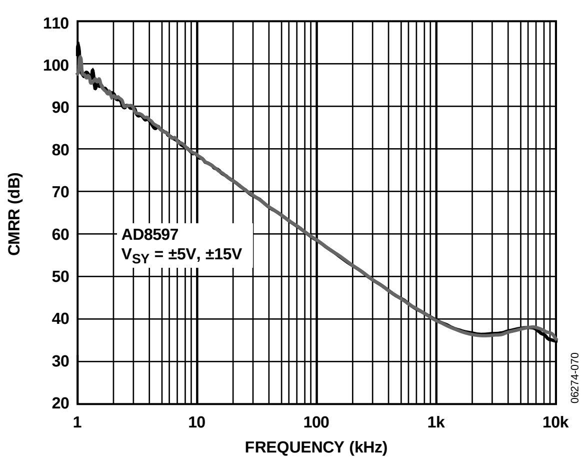


Figure 36. Common-Mode Rejection Ratio vs. Frequency

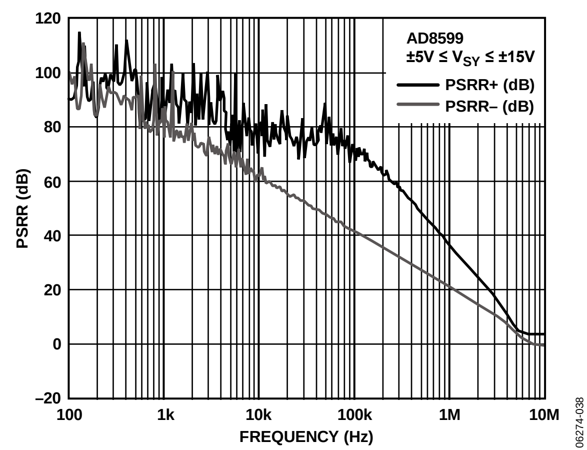


Figure 39. Power Supply Rejection Ratio vs. Frequency

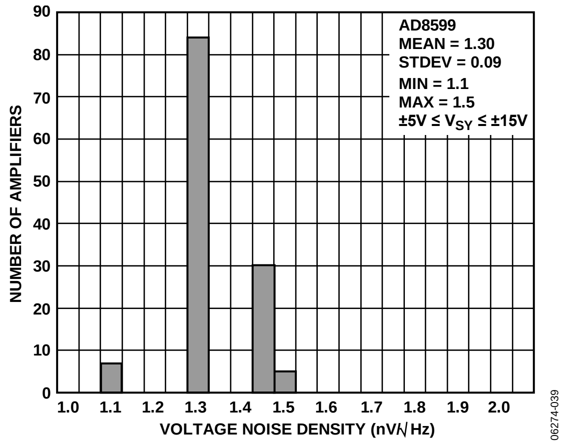


Figure 40. Voltage Noise Density at 10 Hz

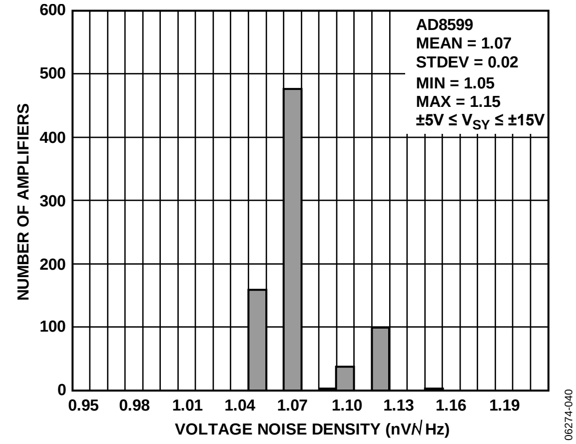


Figure 43. Voltage Noise Density at 1 kHz

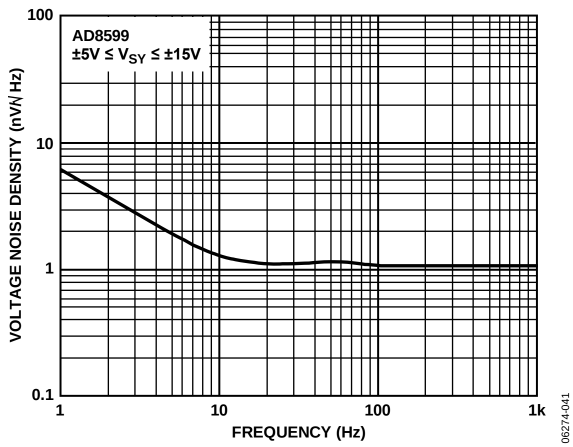


Figure 41. Voltage Noise Density vs. Frequency

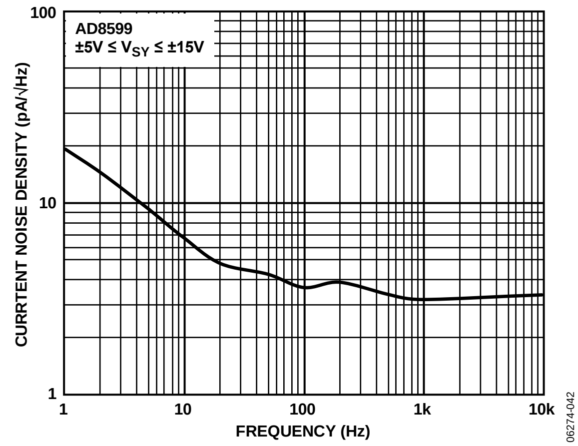


Figure 44. Current Noise Density vs. Frequency

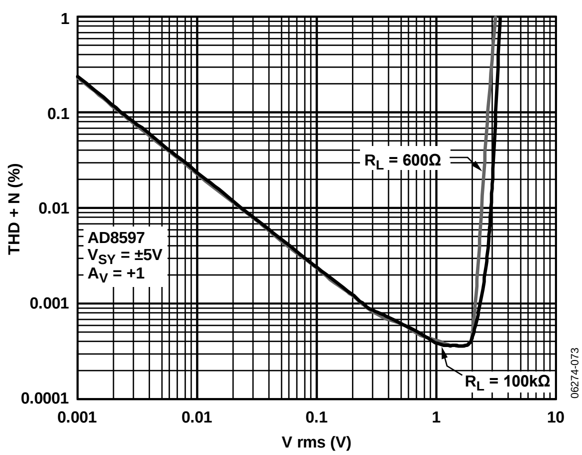


Figure 42. THD + N vs. Amplitude

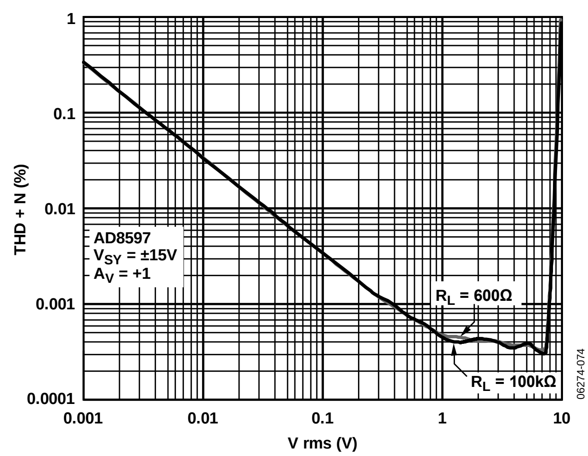


Figure 45. THD + N vs. Amplitude

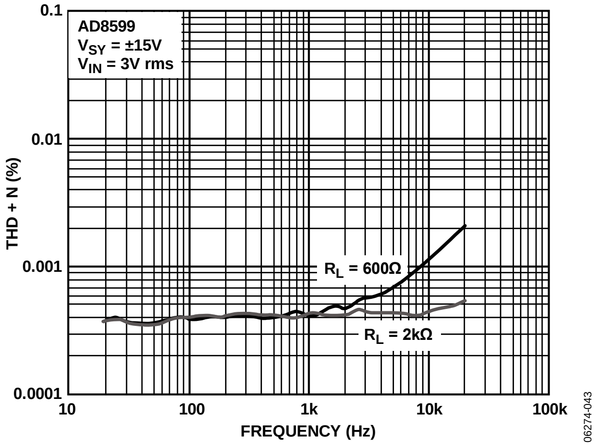


Figure 46. THD + N vs. Frequency

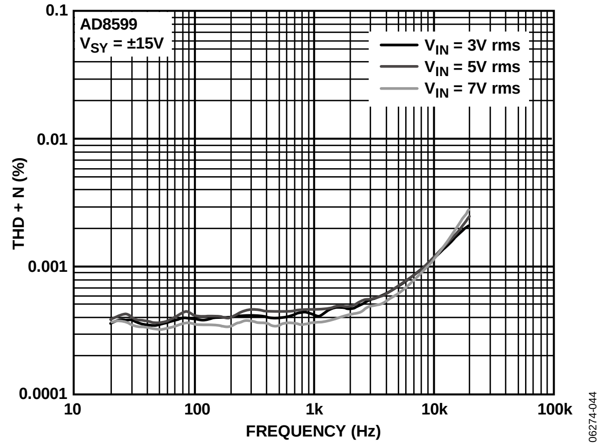


Figure 49. THD + N vs. Frequency

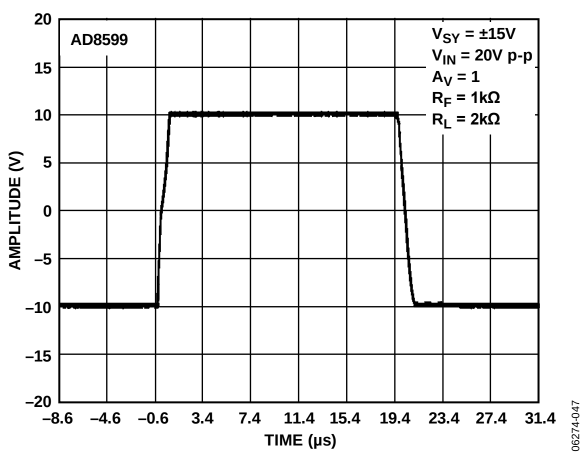


Figure 47. Large Signal Response

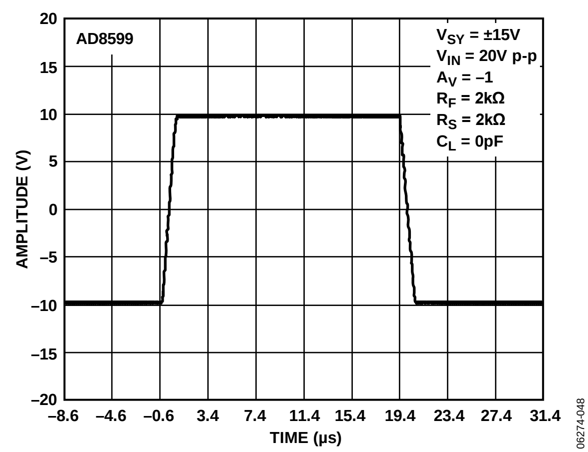


Figure 50. Large Signal Response

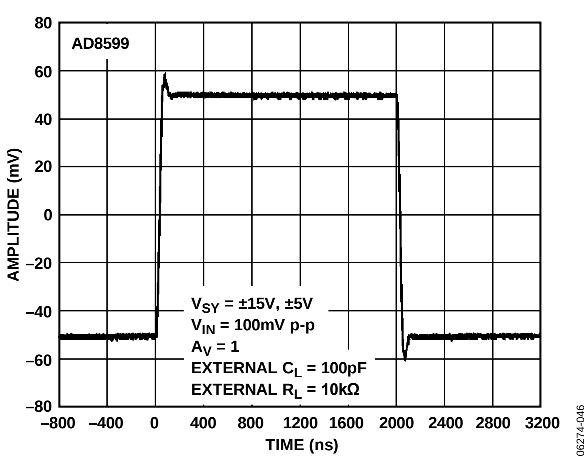


Figure 48. Small Signal Response

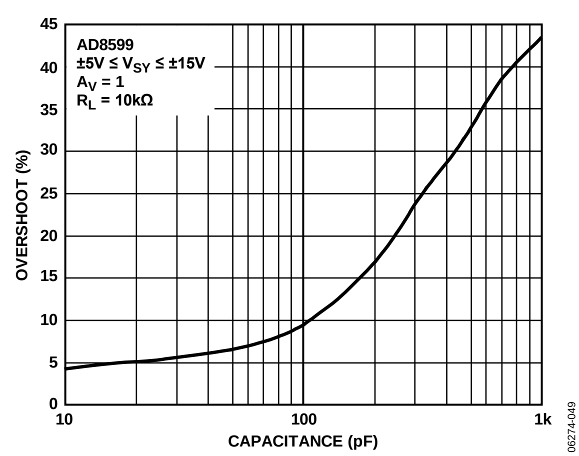


Figure 51. Overshoot vs. Capacitance

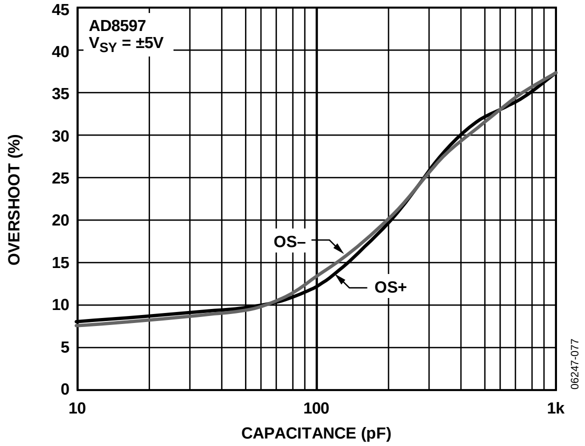


Figure 52. Overshoot vs. Capacitive Load

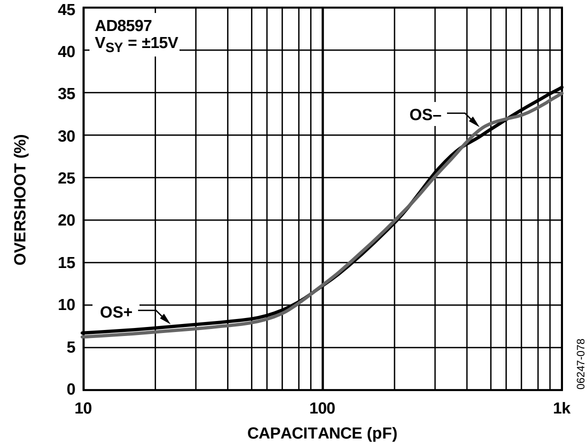


Figure 55. Overshoot vs. Capacitive Load

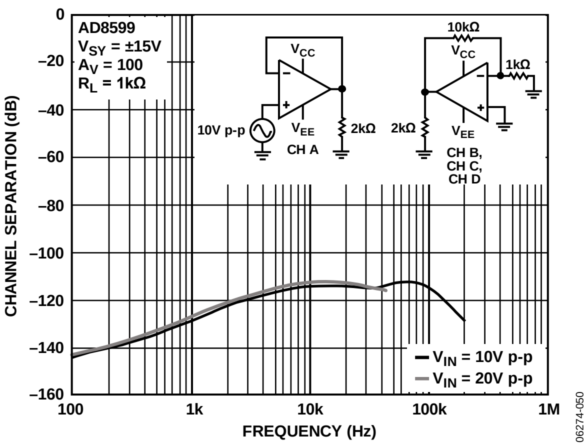


Figure 53. Channel Separation vs. Frequency

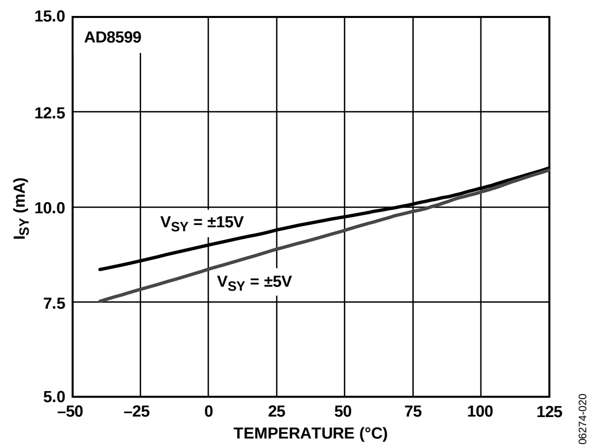


Figure 56. Supply Current vs. Temperature

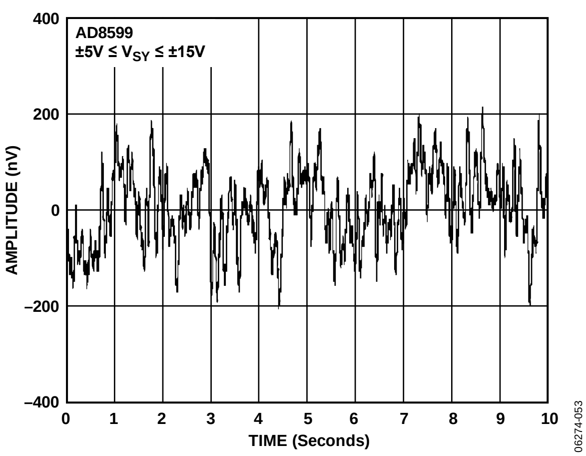


Figure 54. Peak-to-Peak Noise

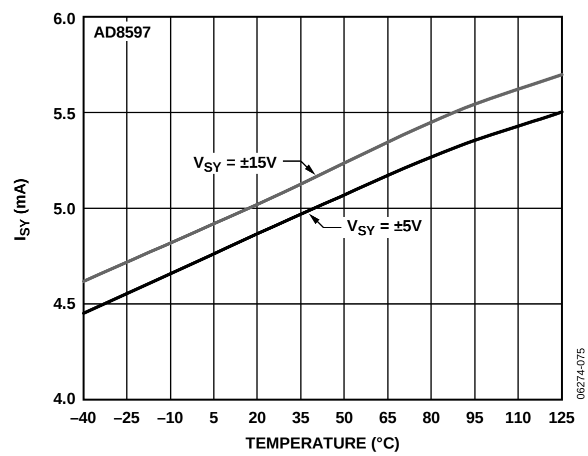


Figure 57. Supply Current vs. Temperature

FUNCTIONAL OPERATION

INPUT VOLTAGE RANGE

The AD8597/AD8599 are not rail-to-rail input amplifiers; therefore, care is required to ensure that both inputs do not exceed the input voltage range. Under normal negative feedback operating conditions, the amplifier corrects its output to ensure that the two inputs are at the same voltage. However, if either input exceeds the input voltage range, the loop opens and large currents begin to flow through the ESD protection diodes in the amplifier.

These diodes are connected between the inputs and each supply rail to protect the input transistors against an electrostatic discharge event and they are normally reverse-biased. However, if the input voltage exceeds the supply voltage, these ESD diodes can become forward-biased. Without current limiting, excessive amounts of current may flow through these diodes, causing permanent damage to the device. If inputs are subject to over-voltage, insert appropriate series resistors to limit the diode current to less than 5 mA maximum.

The input stage has two diodes between the input pins to protect the differential pair. Under high slew rate conditions, when the op amp is connected as a voltage follower, the diodes may become forward-biased and the source may try to drive the output. Place a small resistor in the feedback loop and in the noninverting input. The noise of a 100 Ω resistor at room temperature is ~1.25 nV/√Hz, which is higher than the AD8597/AD8599. Thus, there is a tradeoff between noise performance and protection. If possible, place limiting earlier in the signal path. For further details, see the *Amplifier Input Protection… Friend or Foe?* article at http://www.analog.com/amplifier_input.

Because of the large transistors used to achieve low noise, the input capacitance may seem rather high. To take advantage of the low noise performance, impedance around the op amp must be low, less than 500 Ω. Under these conditions, the pole from the input capacitance must be greater than 50 MHz, which does not affect the signal bandwidth.

OUTPUT PHASE REVERSAL

Output phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. As the common-mode voltage is moved outside the input voltage range, the outputs of these amplifiers can suddenly jump in the opposite direction to the supply rail. This is the result of the differential input pair shutting down that causes a radical shifting of internal voltages that results in the erratic output behavior.

The AD8597/AD8599 amplifiers are carefully designed to prevent any output phase reversal if both inputs are maintained within the specified input voltage range. If one or both inputs exceed the input voltage range but remain within the supply rails, the op amp specifications, such as CMRR, are not guaranteed, but the output remains close to the correct value.

NOISE AND SOURCE IMPEDANCE CONSIDERATIONS

The AD8597/AD8599 ultralow voltage noise of 1.1 nV/√Hz is achieved with special input transistors running at high collector current. Therefore, it is important to consider the total input-referred noise (e_N total), which includes contributions from voltage noise (e_N), current noise (i_N), and resistor noise ($\sqrt{4\,kTR_S}$).

$$e_N\ total = [e_N^2 + 4\,kTR_S + (i_N \times R_S)^2]^{1/2} \quad (1)$$

where R_S is the total input source resistance.

This equation is plotted for the AD8597/AD8599 in Figure 58. Because optimum dc performance is obtained with matched source resistances, this case is considered even though it is clear from Equation 1 that eliminating the balancing source resistance lowers the total noise by reducing the total R_S by a factor of 2.

At a very low source resistance (R_S < 50 Ω), the voltage noise of the amplifier dominates. As source resistance increases, the Johnson noise of R_S dominates until a higher resistance of R_S > 2 kΩ is achieved; the current noise component is larger than the resistor noise.

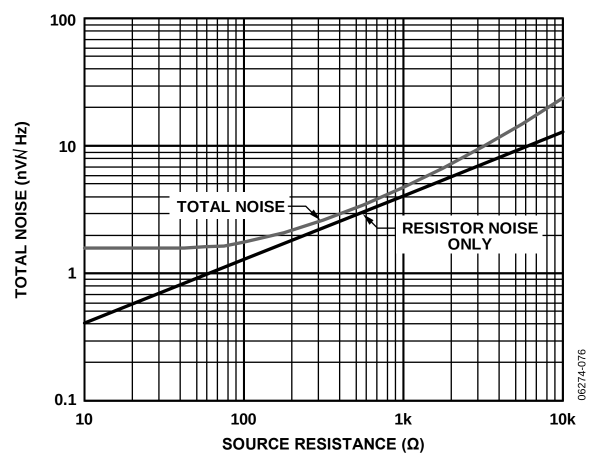


Figure 58. Noise vs. Source Resistance

The AD8597/AD8599 are the optimum choice for low noise performance if the source resistance is kept < 1 kΩ. At higher values of source resistance, optimum performance with respect to only noise is obtained with other amplifiers from Analog Devices. Both voltage noise and current noise must be considered. For more information on avoiding noise from grounding problems and inadequate bypassing, see the AN-345 Application Note, *Grounding for Low- and High-Frequency Circuits*. For general noise theory with extensive calculations, see the AN-358 Application Note, *Noise and Operational Amplifier Circuits*. A good selection table for low noise op amps can be found in AN-940 Application Note, *Low Noise Amplifier Selection Guide for Optimal Noise Performance*. An interesting note on using one section of a monolithic dual to phase compensate the other section is in the AN-107 Application Note, *Active Feedback Improves Amplifier Phase Accuracy*.

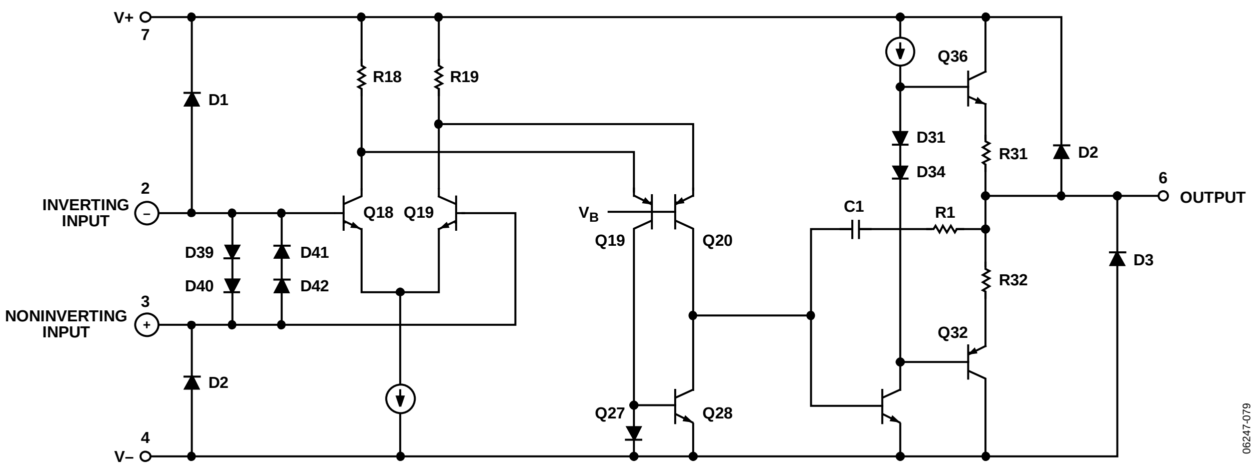


Figure 59. Simplified Schematic

OUTLINE DIMENSIONS

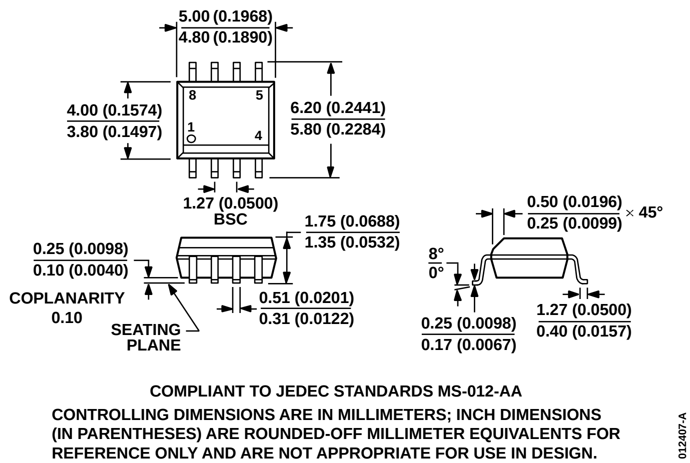


Figure 60. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

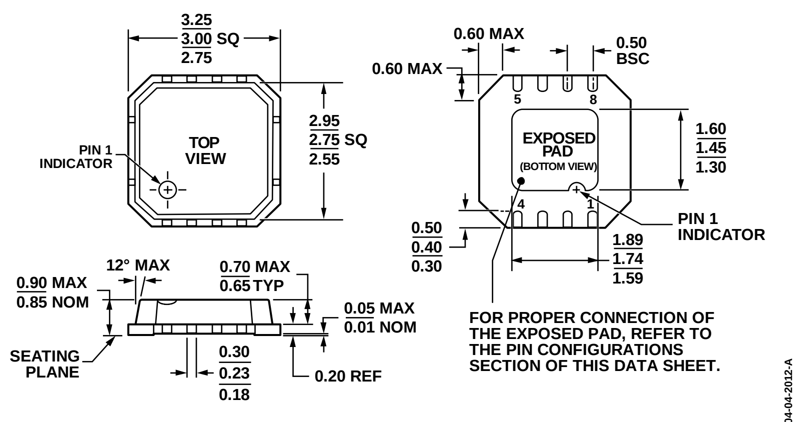


Figure 61. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8597ACPZ-R2	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	A22
AD8597ACPZ-REEL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	A22
AD8597ACPZ-REEL7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	A22
AD8597ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8597ARZ-REEL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8597ARZ-REEL7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8599ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8599ARZ-REEL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8599ARZ-REEL7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

[1] Z = RoHS Complaint Part.

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