SPI Access

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Keywords

- *CC1100*
- *CC1101*
- *CC1150*
- *CC2500*
- *CC2550*
- *SPI*
- *Reset*
- *Burst Access*
- *Command Strobes*

1 Introduction

The purpose of this design note is to show how the SPI interface must be configured to be able to communicate with the CC1100/CC1101/CC1150/CC2500/ CC2550. It also shows how the status bytes should be interpreted, how SW reset is done over the SPI interface, in addition to describing the different SPI accesses that can be used (read/write, single access/burst access, and command strobes).

Table of Contents

2 Abbreviations

MCU	Micro Controller Unit
SPI	Serial Peripheral Interface

3 SPI Interface

CC1100/CC1101/CC1150/CC2500/CC2550 are all configured via a simple 4-wire SPI compatible interface (SI, SO, SCLK and CSn) where the radio is the slave and the MCU is the master. This interface is also used to read and write buffered data. All address and data transfer on the SPI interface is done most significant bit first.

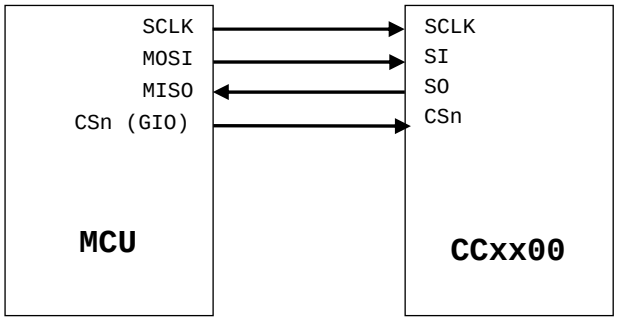

Figure 1. 4-Wire SPI Interface

3.1 Configuring the SPI Interface

The SPI interface on the MCU must be configured to operate in master mode. The Clock phase should be configured so that data is centered on the first positive going edge of the SCLK period and the polarity should be chosen so that the SCLK line is low in idle state.

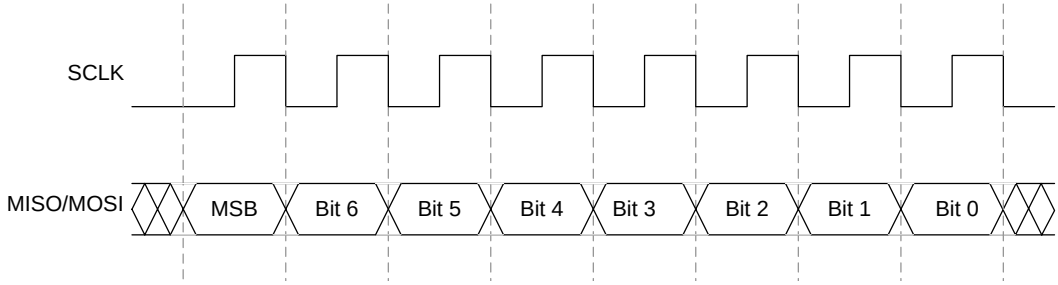

Figure 2. SPI Clock Phase and Clock Polarity

3.2 SPI Interface Timing Requirements

Please see the chip's data sheet for details on the SPI Interface timing requirements. Pay special attention to how the max SCLK frequency (f_{sclk}) changes, depending on how the SPI interface is used. The SPI clock can run at max 10 MHz, given that there is a minimum delay of 100 ns inserted between address byte and data byte (single access), or between address and data, and between each data byte (burst access). See Figure 3.

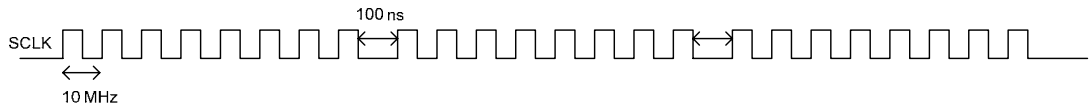

Figure 3. f_{SCLK} = 10 MHz Max

If no delay is inserted between bytes, max clock speed is 9 MHz for single access (see Figure 4) and 6.5 MHz for burst access (Figure 5).

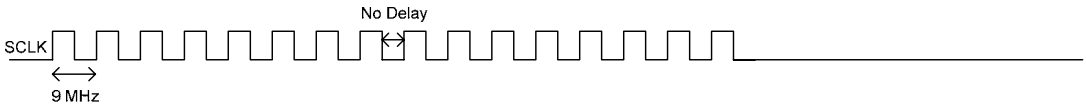

Figure 4. f_{SCLK} = 9 MHz Max

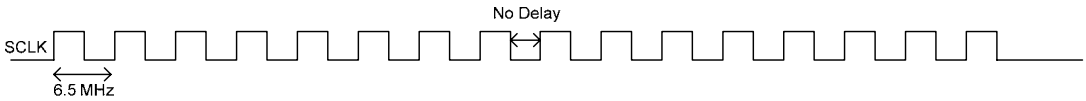

Figure 5. f_{SCLK} = 6.5 MHz Max

4 SPI Accesses

The chips have 47 configuration registers (address 0 to address 0x2E). The R/W bit in the address header controls if the register should be written or read, and the burst bit controls if it is a single access or a burst access.

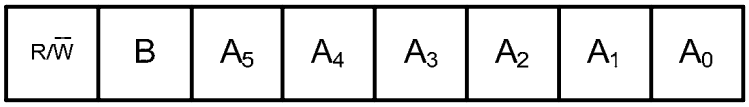

Figure 6. Address Header

After pulling CSn, one should always wait for the MISO to go low (`CHIP_RDYn`), before writing the address header. The `CHIP_RDYn` signal indicates that the crystal is running and the regulated digital supply voltage is stable. Unless the chip is in the SLEEP or XOFF states or an SRES command strobe is issued, the SO pin will always go low immediately after taking CSn low.

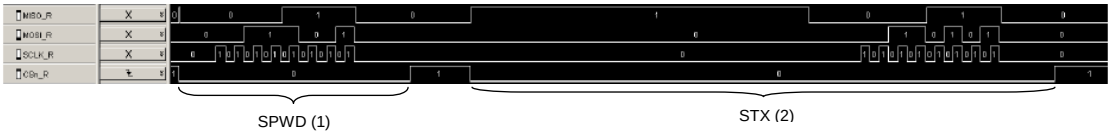

Figure 7. Waiting for `CHIP_RDYn` After Waking the Radio from SLEEP

Figure 7 shows how it looks like if the radio is put in SLEEP state (SPWD) from IDLE (1), and then woken from SLEEP state by transmitting a TX strobe (STX) (2). The radio wakes from SLEEP when CSn goes low. The first time CSn goes low, MISO goes high and then low again immediately, indicating that the chip is ready. Next time CSn goes low, the radio is in SLEEP state, and MISO is therefore high. When the voltage regulator has stabilized and the crystal is up and running MISO goes low and it is safe to transmit the TX strobe.

4.1 Single Access

For single access to the registers, the burst bit has to be set to 0. After transmitting the address header, one can either transmit one data byte or read one byte, depending on the R/W bit. After the data byte a new address is expected; hence, CSn can remain low. Figure 8 shows how 0x0A is first written to register 0x02, and then read from the same register.

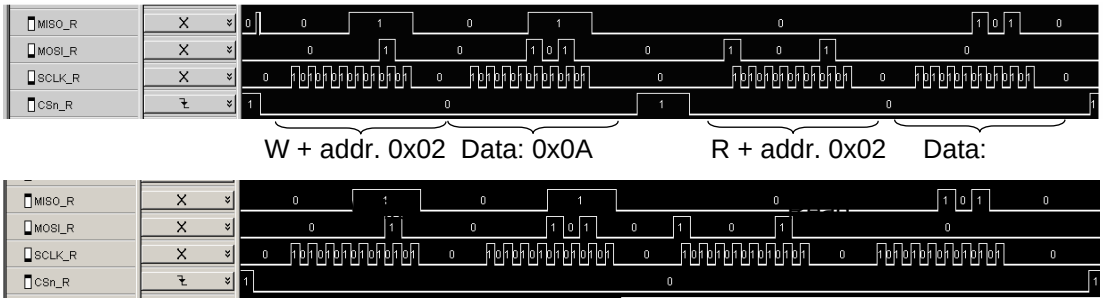

Figure 8. Single Byte Access (Write and Read)

4.2 Burst Access

When the burst bit is set, the radio expects one address byte and then consecutive data bytes until terminating the access by setting CSn high.

```
BYTE xdata regValues[] = {1,2,3};
halSpiWriteBurstReg(0x00, regValues, sizeof(regValues));
halSpiReadReg(0x00);
halSpiReadReg(0x01);
halSpiReadReg(0x02);
```

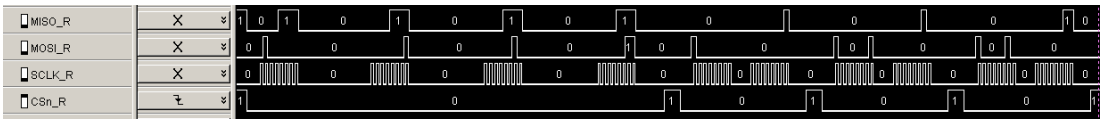

Figure 9. Burst Write Followed by Single Read

4.3 Command Strobes

Command strobes are single byte instructions which will start an internal sequence (start RX, enter power down mode etc). The command strobes share addresses with a set of status registers (address 0x30 to address 0x3F). These status registers can not be accessed in burst mode. If the burst bit is 1, a status register is accessed, if the burst bit is 0, a command strobe is sent. A command strobe may be followed by any other SPI access without pulling CSn high. After issuing an SRES command strobe the next command strobe can be issued when the MISO pin goes low. The command strobes are executed immediately, with the exception of the SPWD and the SXOFF strobes that are executed when CSn goes high.

```
// Strobe IDLE
NSSMD0 = 0;
while (P0_1); // Wait for CHIP_RDYn
SPI0DAT = CCxxx0_SIDLE;
SPI_WAIT();

// Write 0x0A to register 0x00
while (P0_1); // Wait for CHIP_RDYn
SPI0DAT = 0x00;
SPI_WAIT();
SPI0DAT = 0x0A;
SPI_WAIT();

// Reset
while (P0_1); // Wait for CHIP_RDYn
SPI0DAT = CCxxx0_SRES;
SPI_WAIT();

// Read Register 0x00
while (P0_1); // Wait for CHIP_RDYn
SPI0DAT = (0x00 | READ_SINGLE);
SPI_WAIT();
SPI0DAT = 0;
SPI_WAIT();
x = SPI0DAT;
NSSMD0 = 1;
```

Figure 10. Several SPI Accesses with CSn Kept Low

When CSn is pulled low, MISO is already low, indicating that the chip is ready. The SIDLE strobe is followed by a register write and an SRES strobe without having to wait for CHIP_RDYn. After the reset strobe, it takes some time before MISO goes low and register 0x00 can be read. The value read from this register is 0x29 (the default values after reset).

5 Chip Status Byte

When the header byte, data byte or command strobe is sent on the SPI interface, the chip status byte is sent from the radio on the MISO pin. The status byte contains key status signals, useful for the MCU.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>CHIP_RDYn</td><td>Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.</td></tr>
<tr><td>6:4</td><td>STATE[2:0]</td><td>Indicates the current main state machine mode
<table>
<tr><th>Value</th><th>State</th><th>Description</th></tr>
<tr><td>000</td><td>IDLE</td><td>IDLE state
(Also reported for some transitional states instead of SETTLING or CALIBRATE)</td></tr>
<tr><td>001</td><td>RX</td><td>Receive mode</td></tr>
<tr><td>010</td><td>TX</td><td>Transmit mode</td></tr>
<tr><td>011</td><td>FSTXON</td><td>Fast TX ready</td></tr>
<tr><td>100</td><td>CALIBRATE</td><td>Frequency synthesizer calibration is running</td></tr>
<tr><td>101</td><td>SETTLING</td><td>PLL is settling</td></tr>
<tr><td>110</td><td>RXFIFO_OVERFLOW</td><td>RX FIFO has overflowed. Read out any useful data, then flush the FIFO with SFRX</td></tr>
<tr><td>111</td><td>TXFIFO_UNDERFLOW</td><td>TX FIFO has underflowed. Acknowledge with SFTX</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>FIFO_BYTES_AVAILABLE[3:0]</td><td>The number of bytes available in the RX FIFO or free bytes in the TX FIFO</td></tr>
</table>

Table 1. Status Byte Summary

When writing to registers, the status byte is sent on the MISO pin each time a header byte or data byte is transmitted on the MOSI pin. When reading from registers, the status byte is sent on the MISO pin each time a header byte is transmitted on the MOSI pin. Be aware that the 4 LSB of the status byte (FIFO_BYTES_AVAILABLE) can give information on either the TX FIFO (R/W = 0) or the RX FIFO (R/W = 1).

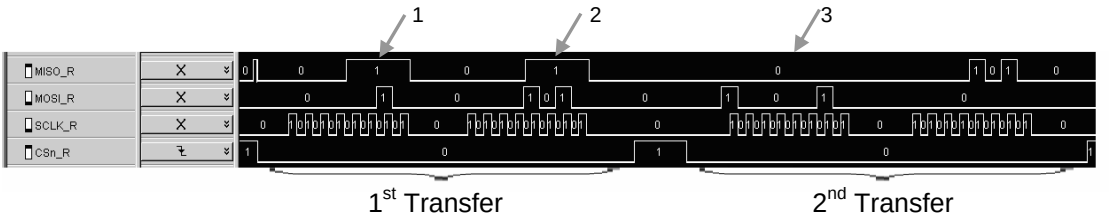

Figure 11. Status Byte Interpretation

The first transfer writes 0x0A to register 0x02. Since it is a write operation, the status byte is transmitted on the MISO line both when the address header is transmitted (1) and when the data byte is transmitted (2). The status bytes (0x0F) tell us that the radio is in IDLE state and that there are 15 or more free bytes in the TX FIFO (FIFO_BYTES_AVAILABLE = 15).

The second transfer reads register 0x02. Since this is a read operation, the status byte is only returned on the MISO line when the address header is transmitted (3). The next byte on the MISO line is the content of register 0x02, which is 0x0A. The status byte tells us that the radio is in IDLE state (STATE = 0) and that there are 0 bytes available in the RX FIFO (FIFO_BYTES_AVAILABLE = 0).

Reset

When the power supply complies with the requirements specified in the data sheet, proper Power-On-Reset functionality is guaranteed. Otherwise, the chip should be assumed to have unknown state until a SW reset is implemented (see Figure 12).

- Strobe CSn low / high.
- Hold CSn high for at least 40 µs relative to pulling CSn low
- Pull CSn low and wait for SO to go low (`CHIP_RDYn`).
- Issue the SRES strobe on the SI line.

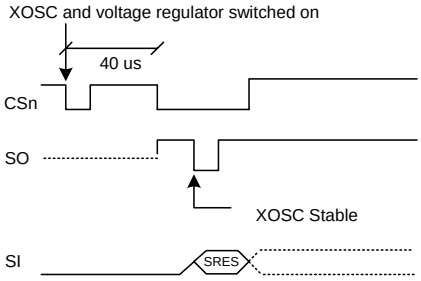

Figure 12. Power-On-Reset with SRES

See code below:

```
//-----------------------------------------------------------------------------------
// Macro to reset the CCxxx0 and wait for it to be ready
#define RESET_CCxxx0()         \
    do {                       \
        NSSMD0 = 0;            \
        while (P0_1);          \
        SPI0DAT = CCxxx0_SRES; \
        SPI_WAIT();            \
        NSSMD0 = 1;            \
    } while (0)
//-----------------------------------------------------------------------------------


//-----------------------------------------------------------------------------------
// Macro to reset the CCxxx0 after power_on and wait for it to be
// ready
// IMPORTANT NOTICE:
// The file Wait.c must be included if this macro shall be used
// The file is located under: ..\Lib\Chipcon\Hal\CCxx00
//
//                min 40 us
//             <----------------------->
// CSn      |--|  |--------------------|          |-----------
//          |  |  |                    |          |
//             --                      ----------
//
// MISO                                          |---------------
//          - - - - - - - - - - - - - - -|  |
//                                         --
//               Unknown / don't care
//
// MOSI     - - - - - - - - - - - - - - ---------- - - - - -
//                                      | SRES |
//          - - - - - - - - - - - - - - ---------- - - - - -
//
#define POWER_UP_RESET_CCxxx0() \
    do { \
        NSSMD0 = 1; \
        halWait(1); \
        NSSMD0 = 0; \
        halWait(1); \
        NSSMD0 = 1; \
        halWait(41); \
        RESET_CCxxx0(); \
    } while (0)
//-----------------------------------------------------------------------------------
```

6 General Information

6.1 Document History

Revision	Date	Description/Changes
SWRA112B	2007.10.22	Removed logo from header. Added CC1101. Changed Table 1 and Figure 12.
SWRA112A	2006.10.27	Figure 12 has been changed.
SWRA112	2006.07.06	Initial release.

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