Group Members: Grant Martinez (me), Eduardo Alvarez, Samuel Cole

Individually I was in charge of designing the decode and writeback stages as well as creating the time diagrams for each instruction we implemented. The decode and writeback stages also included the register file design.

- Decode: I created the decode stage by decoding icode and reading from the given rA, rB, or rsp depending on the icode.
- Writeback: The writeback stage was by far the more difficult of the two. It began with similar steps to decode. Firstly icode was decoded to determine what our write_address and write_data would be. This was straightforward. The difficult step was implementing the double writeback for popq. We ended up hardcoding a delay into writeback so that it ran 3 cycles no matter what. This allowed us to write once to the first register and then get the write_data and write_address for the second write.
- Time Diagrams: This was more tedious than difficult, but it also helped me to better understand the flow of our machine. I tracked the length of each stage as well as when the different outputs such as valA, valB, valC, etc. were being given.

This assignment felt like a much improved and more rewarding version of lab 4. Given almost an entire month we were able to distribute the work evenly and work in a timely manner as a group. While we did a majority of our implementations individually we did collaboratively fix bugs, suggest improvements to each other's designs, and test the programs. This lab was challenging yet very rewarding. After finishing it I can now say that I significantly contributed in a group effort to make a y86 CPU.