

ECE 243S – Computer Organization – 2016
Simple Multi-Cycle Processor

Overview

This implementation of a simple multi-cycle processor consists of the datapath, control (FSM), and various inputs and outputs. The processor supports only fixed-length 8-bit instructions and data, and can only access memory one byte at a time. Overall, 10 instructions are implemented in hardware.

Functional Description

The inputs and outputs include:

Inputs:

- reset – clears the values of all registers and control signals, resets the condition flags, and resets the control FSM (KEY[0])
- clock – all writes and cycle transitions happen on the positive edge of the clock (KEY[1])
- SW[3:0] – Two sets of two-bit select signals to choose which registers or control signals to display on the seven-segment displays and LEDs. This is needed because we want to observe more signals than available displays and LEDs. SW[3:2] controls the LEDs, while SW[1:0] controls seven-segment displays.

Outputs:

- SW[3:2] = 0
 - PCWrite – LEDR[9]
 - AddrSel – LEDR[8]
 - MemRead – LEDR[7]
 - MemWrite – LEDR[6]
 - IRLoad – LEDR[5]
 - OpASel – LEDR[4]
 - MDRLoad – LEDR[3]
 - OpABLoad – LEDR[2]
 - RFWrite – LEDR[1]
 - RegIn – LEDR[0]
- SW[3:2] = 1
 - N (negative) – LEDR[1]
 - Z (zero) – LEDR[0]
- SW[3:2] = 2
 - ALU2[2:0] – LEDR[9:7]
 - ALU1 – LEDR[5]
 - ALUOp[2:0] – LEDR[4:2]
 - ALUOutWrite – LEDR[1]
 - FlagWrite – LEDR[0]

- SW[1:0] = 0
 - PCwire – HEX5 and HEX4
 - r0 – HEX3 and HEX2
 - r1 – HEX1 and HEX0
- SW[1:0] = 1
 - PCwire – HEX5 and HEX4
 - r2 – HEX3 and HEX2
 - r3 – HEX1 and HEX0
- SW[1:0] = 2
 - ALU1wire – HEX5 and HEX4
 - ALU2wire – HEX3 and HEX2
 - ALUwire – HEX1 and HEX0

Instructions

- Addition (add)
- Subtraction (sub)
- NAND (nand)
- Shifting (shift)
- OR with Immediate (ori)
- Load (load)
- Store (store)
- Branch If Positive Zero (bpz)
- Branch If Zero (bz)
- Branch If Not Zero (bnz)