

University of Washington Bothell

B EE 504 Laboratory 2

MOSFET Characterization and Circuits

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Date submitted: 3/5/2023

Activity	Student name
Circuit construction	Mateo Balcorta & Gwen Montague
Data collection	Mateo Balcorta & Gwen Montague
Data analysis	Mateo Balcorta & Gwen Montague
Answers to questions	Mateo Balcorta & Gwen Montague
Lab report writing	Mateo Balcorta & Gwen Montague

BEE 504 : Device electronics

Winter Term 2023

Dr. Lawrence Lam

Lab 2-1A – MOSFET IV Characteristics

I. Objectives

The objective of this lab is to observe characteristics of Metal-Oxide Field-Effect Transistor (MOSFETs) by performing various procedures and producing IV characteristics and I_D vs V_{GS} graphs. These graphs give us insight into the workings of MOSFETs and the ability to compare to ideal models.

II. Materials Used

Breadboard (with metal back in plate attached)

Digital multimeter

Various sized jumper wires

$100\ \Omega$ 1% 1/4 W

$1.0\ k\Omega$ 1% 1/4 W

2N7000

Bench power supply

III. Procedure, Analysis, Calculations, Results, and Questions

A. Experiment 2-1A-I: Measuring I_D versus V_{GS} Curve

1.1.1 For this procedure the following circuit in Figure 4 was constructed. The MOSFET pin assignment from Figure 1 was followed to orient pins correctly in the circuit. Two DC power supplies were connected to V_{DD} and V_{GG} . Voltage readings were taken for voltage across $V(R_D)$.

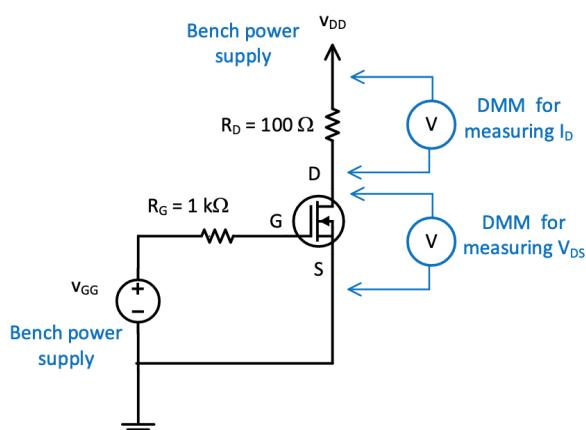


Figure 4 – MOSFET test circuit.

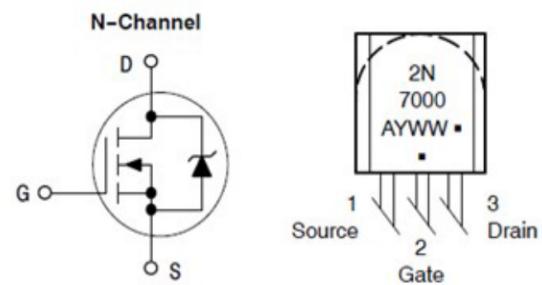


Figure 1 – MOSFET symbol and pin assignment.

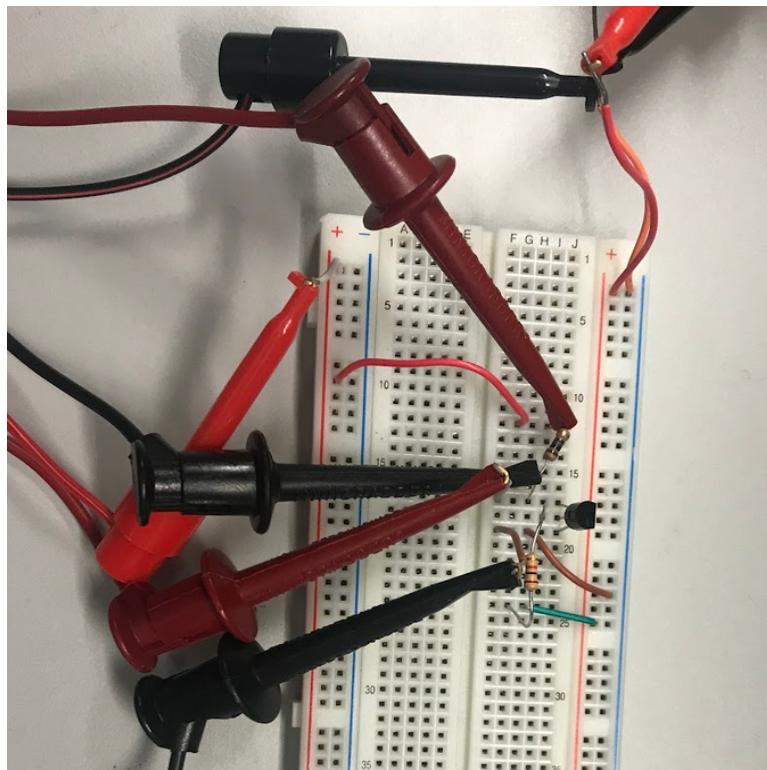


Figure 1.1 shows the circuit built from Figure 4. Multimeter is connected at terminal ends of the 100Ω resistor. Flat side of the MOSFET is facing the right hand side of the breadboard therefore pin orientation for drain, gate and source is from top of breadboard to the bottom.

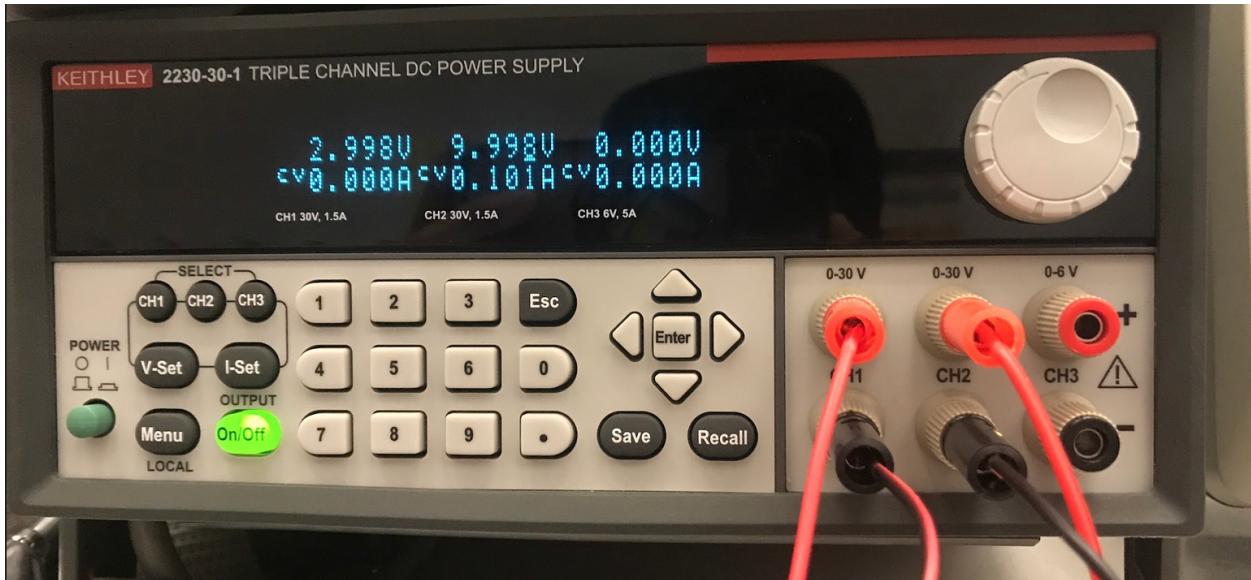


Figure 1.2 Shows DC power supply used to provide power to V_{DD} and V_{GG}

1.1.2 V_{DD} was set to constant 12V and V_{GG} increased by 0.2 V for 13 trials. V_{GG} was recorded as V_{GS} as they are the same value and $V(R_D)$ was also recorded. I_D is obtained by ohms law using $\frac{V(R_D)}{100 \Omega}$. We graphed the results of I_D Vs. V_{GS} and when our graph appeared similar to Figure 3 we concluded our trials. As V_{GS} increased past 2 volts, our 100Ω resistor began to darken and smell burnt. After the trials we tested the 100Ω resistor and it was still functioning accordingly.

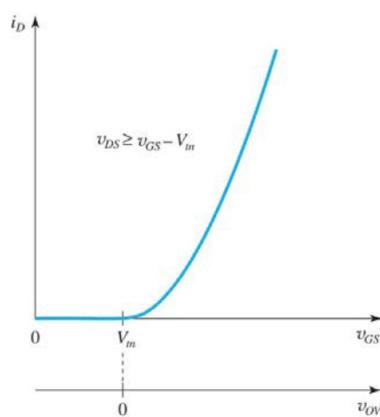
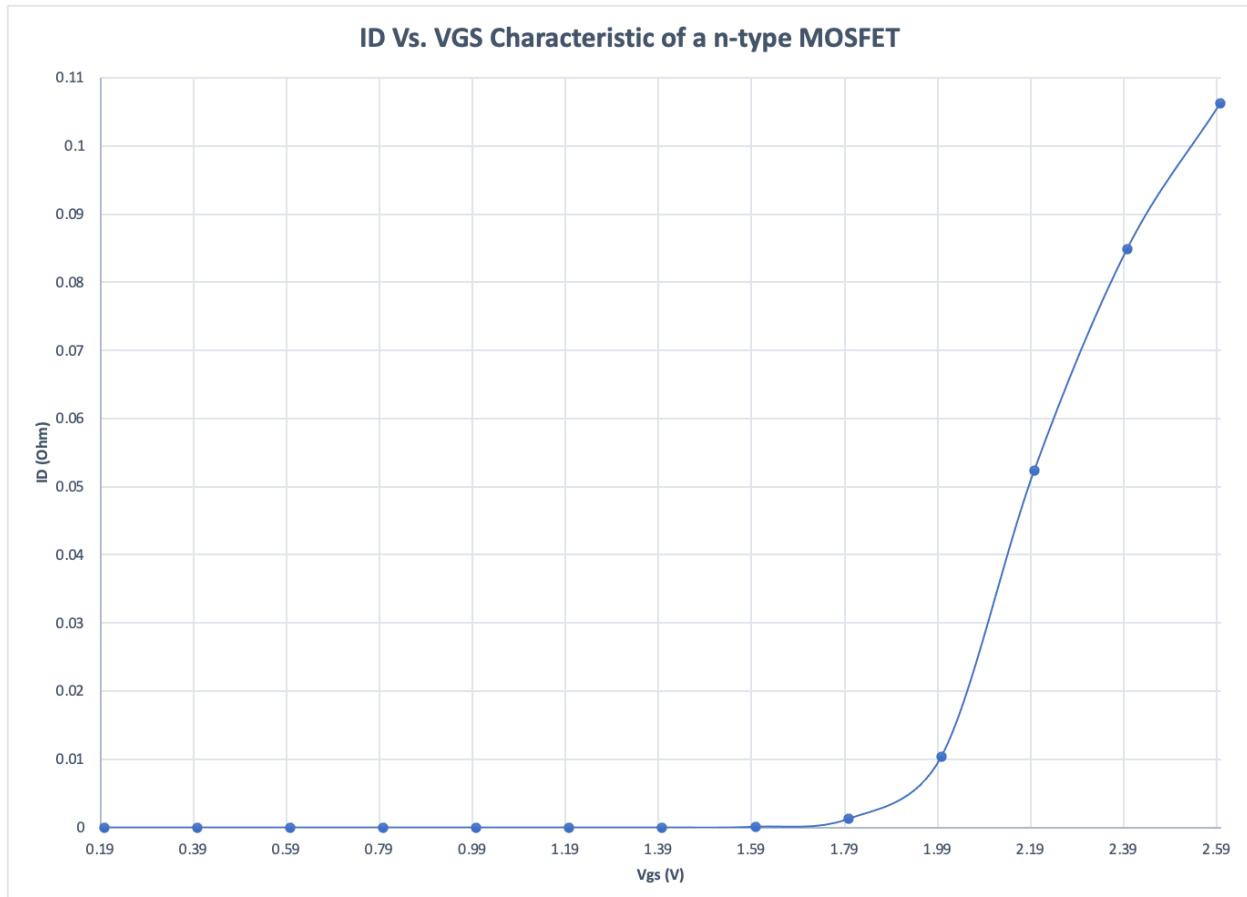


Figure 3 – I_D vs. V_{GS} characteristic of a n-type MOSFET

Procedure 1.1.2 Data

Table 1 – ID vs. VGS Sample Data

<i>Trial</i>	VGS(v)	V(RD) (mV)	<i>ID</i> (Ohm)
1	0.199	0.11	0.0000011
2	0.399	0.11	0.0000011
3	0.599	0.11	0.0000011
4	0.798	0.11	0.0000011
5	0.998	0.12	0.0000012
6	1.198	0.15	0.0000015
7	1.398	0.76	0.0000076
8	1.598	10.92	0.0001092
9	1.798	126.2	0.001262
10	1.998	1036	0.01036
11	2.198	5237	0.05237
12	2.398	8490	0.0849
13	2.598	10620	0.1062



1.1.3 Graph of I_D Vs V_{GS}

B. Experiment 2-1A-II: Measuring I_D versus V_{DS} Curves

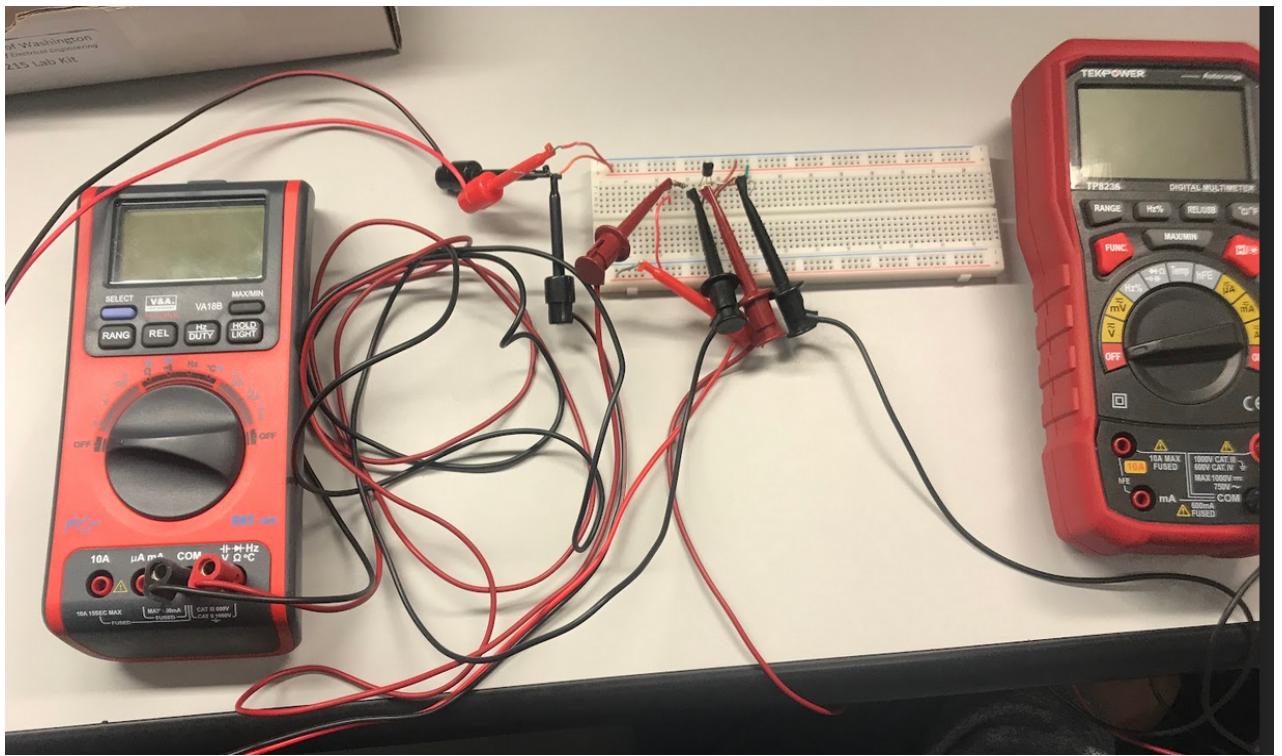


Figure 1.3 Displays setup for measuring both $V(R_D)$ and V_{DS} . Multimeter on left read voltage values for V_{DS} and multimeter on right read values for $V(R_D)$.

1.1.4 The same circuit was used from Figure 4. V_{GS} was set at a constant value of 1.5 V. V_{DD} was started at 1 V and incremented by 0.5V for each trial till 10V was reached. Both $V(R_D)$ and V_{DS} were measured as indicated in Figure 4.

1.1.5 These steps for 1.1.4 were repeated again with V_{GS} at 2.0V.

1.1.6 These steps for 1.1.4 were repeated again with V_{GS} at 2.5V.

1.1.7 These steps for 1.1.4 were repeated again with V_{GS} at 3V.

Table 2 – ID vs. VDS Sample Data for VGS = 1.5 V

VDD (V)	V(RD) (mV)	ID (Ohms)	VDS (V)
0.999	0.85	0.0000085	0.997
1.498	1.07	0.0000107	1.497
1.999	1.22	0.0000122	1.997
2.498	1.33	0.0000133	2.496
2.998	1.43	0.0000143	2.996
3.499	1.52	0.0000152	3.496
3.998	1.6	0.000016	3.996
4.498	1.68	0.0000168	4.496
4.998	1.75	0.0000175	4.996
5.499	1.82	0.0000182	5.496
5.999	1.89	0.0000189	5.996
6.499	1.96	0.0000196	6.48
6.999	2.03	0.0000203	6.98
7.499	2.1	0.000021	7.47
7.999	2.16	0.0000216	7.97
8.498	2.23	0.0000223	8.47
8.999	2.29	0.0000229	8.97
9.498	2.35	0.0000235	9.47
9.998	2.42	0.0000242	9.97

Table 2 – ID vs. VDS Sample Data for VGS = 2.0 V

VDD (V)	V(RD) (mV)	ID (Ohms)	VDS (V)
0.999	273.8	0.002738	0.723
1.498	348.8	0.003488	1.148
1.998	410.7	0.004107	1.585
2.498	462.3	0.004623	2.038
2.998	501.4	0.005014	2.494
3.498	532.6	0.005326	2.964
3.998	557.5	0.005575	3.438
4.498	575.8	0.005758	3.92
4.998	594.8	0.005948	4.402
5.499	618.3	0.006183	4.877
5.999	644	0.00644	5.351
6.499	664	0.00664	5.83
6.999	687	0.00687	6.29
7.499	708	0.00708	6.77
7.999	729	0.00729	7.74
8.498	759	0.0075	7.72
8.999	750	0.00759	8.22
9.498	770	0.0077	8.7
9.998	809	0.00809	9.15

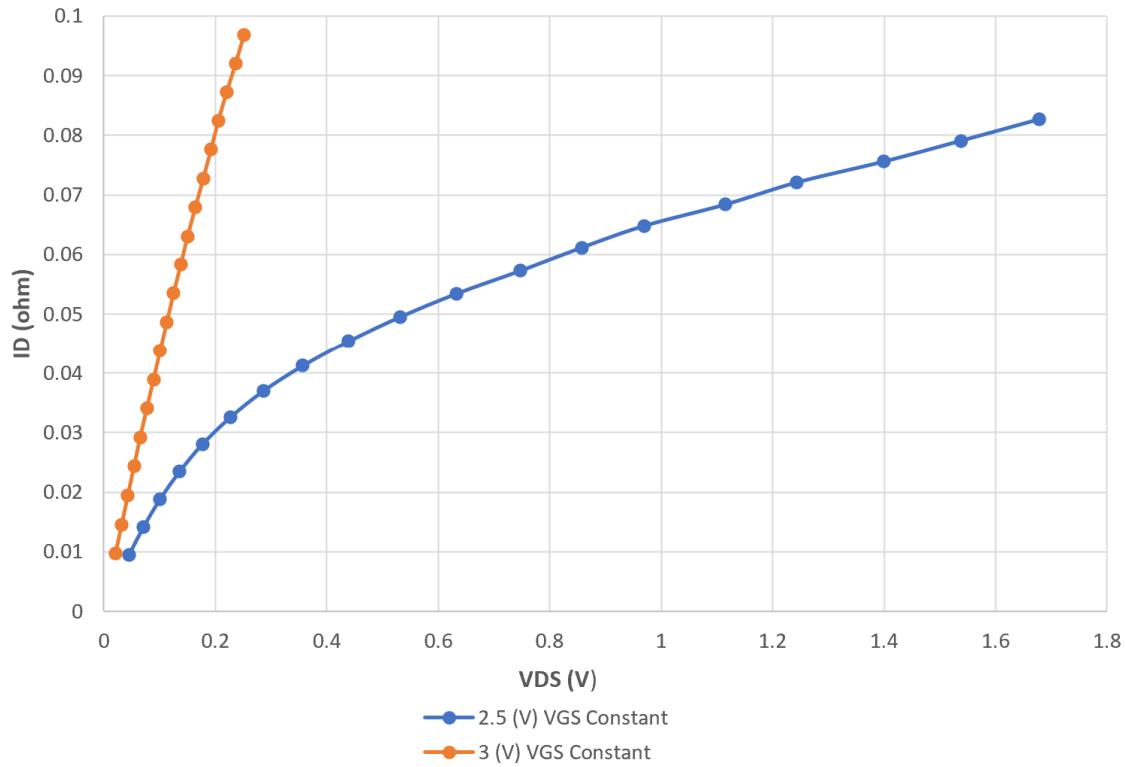
Table 3 – ID vs. VDS Sample Data for VGS = 2.5 V

VDD (V)	V(RD) (V)	ID (Ohms)	VDS (V)
0.999	0.949	0.00949	0.045
1.498	1.42	0.0142	0.071
1.998	1.888	0.01888	0.101
2.498	2.352	0.02352	0.136
2.998	2.808	0.02808	0.177
3.498	3.258	0.03258	0.227
3.998	3.697	0.03697	0.286
4.498	4.124	0.04124	0.357
4.998	4.54	0.0454	0.439
5.499	4.949	0.04949	0.531
5.999	5.344	0.05344	0.633
6.498	5.727	0.05727	0.747
6.999	6.116	0.06116	0.857
7.499	6.48	0.0648	0.969
7.999	6.84	0.0684	1.115
8.499	7.21	0.0721	1.243
8.999	7.56	0.0756	1.399
9.498	7.91	0.0791	1.538
9.998	8.27	0.0827	1.678

Table 3 – ID vs. VDS Sample Data for VGS = 3 V

VDD (V)	V(RD) (V)	ID (Ohms)	VDS (V)
0.999	0.972	0.00972	0.021
1.498	1.459	0.01459	0.032
1.999	1.947	0.01947	0.043
2.498	2.433	0.02433	0.054
2.998	2.92	0.0292	0.065
3.499	3.407	0.03407	0.077
3.998	3.892	0.03892	0.089
4.498	4.379	0.04379	0.101
4.998	4.865	0.04865	0.113
5.499	5.351	0.05351	0.125
5.999	5.836	0.05836	0.138
6.499	6.3	0.063	0.15
6.999	6.79	0.0679	0.164
7.499	7.27	0.0727	0.178
7.999	7.76	0.0776	0.192
8.498	8.24	0.0824	0.205
8.999	8.72	0.0872	0.22
9.499	9.2	0.092	0.236
9.998	9.68	0.0968	0.251

ID versus VDS Characteristic of a n-type MOSFET



1.1.8 Excel plot ID versus V_{DS} for $V_{GS} = 2.5 \text{ V}$ and $V_{GS} = 3 \text{ V}$

1.2 Questions for 2-1A

1.2.5

As seen by our data of I_D Vs V_{GS} in table 1 we can see a non zero current begins to be produced at 1.59 V_{GS} therefore we can infer that the threshold voltage for our MOSFET in this procedure is less than 1.59 V . According to datasheet for 2N7000 the V_{GS} value can be seen between the values of 0.8 to 3.0, so we are well within range for this device.

1.2.6

We found that I_D starts to saturate when V_{DS} is greater than 0.969 V . When comparing this measured value of V_{DS} to the computed value of $V_{GS} - V_t$ we are

able to see that there is less than 0.07 V difference at the boundary of the triode and saturation regions.

1.2.7

Based on our measurements we are able to conclude that the MOSFET turns on around 1.59 V, so when V_{GS} is less than 1.59 V the operation of the MOSFET is in the cutoff region. Additionally, we can infer from our measurements that the MOSFET operates in the triode region up until V_{DS} reaches 0.969 V. At this point the MOSFET operation reaches the boundary of the triode and saturation regions. Once V_{DS} exceeds 0.969 V the MOSFET is operating in the saturation region as the ID curve starts to saturate.

Experiment-2

Lab 2-1B – CMOS NAND Gate Logic Circuit

I. Objectives

The objective of this lab is to learn how to analyze and build a CMOS logic circuit from individual transistors in a CD4007 Transistor Array IC.

II. Materials Used

Breadboard (with metal back in plate attached)
Digital multimeter
Various sized jumper wires
CD4007
Bench power supply

III. Procedure, Analysis, Calculations, Results, and Questions

4.1 Procedure for Building a NAND Gate from CMOS Transistors

4.1.1 NAND Gate from Figure 9 was build as shown in figure Figure 2.1

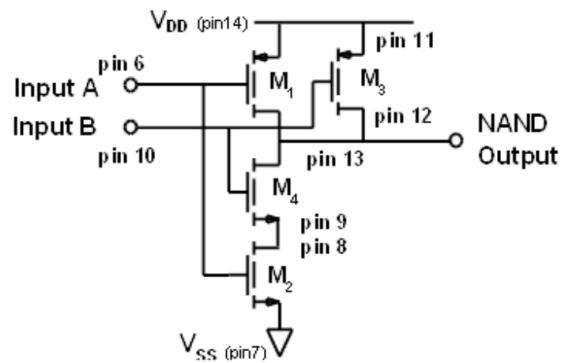


Figure 9 – NAND from individual CMOS transistors.

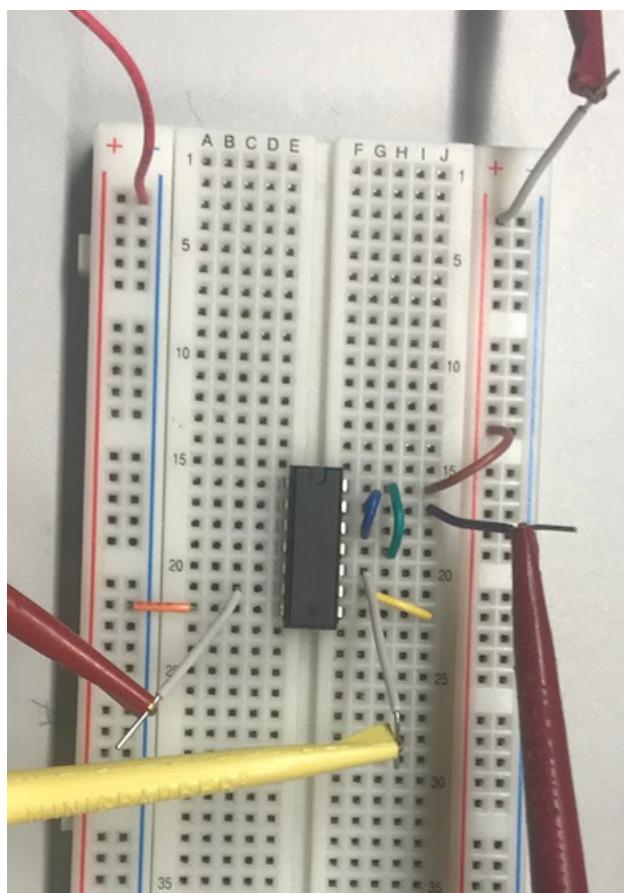


Figure 2.1 Show the circuit built according to Figure 9. CD4007 transistor was placed in the middle of the breadboard with various jumper wires connecting individual transistors. Pin 14 was connected to VDD with a voltage of 5 Volts and pin 7 connected to ground. Input values were applied at pin 6 and pin 10.



Figure 2.2 DC power supply was used to power CD4007 transistor and inputs for both input a and b according to each trial. Channel 1 connected to VDD, channel 2 to input A and channel 3 to input B.

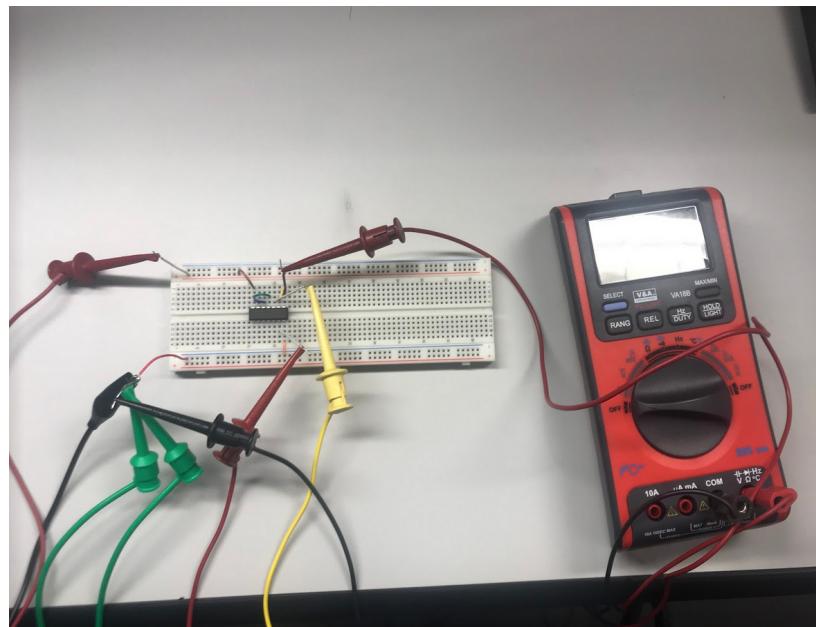


Figure 2.3 shows the setup for measuring M values on each trial. In this picture the voltage value of M2 was measured.

4.1.3 Values were alternated at inputs A and B for each trial. In each trial voltage at output pin 13 was measured and these values were confirmed with the truth table for NAND gate. Once correct configuration was completed M values were measured. M values were measured between voltage drain to

ground of each transistor for all M values. M values of 1,3 and 4 were the same output due to connection created between pins 13 and 12 and pins 14 and 11.

Truth Table – CMOS NAND Gate

Input A (v)	Input B (v)	M1 (V)	M2 (V)	M3 (v)	M4 (v)	Output (v)
0	0	4.997	0	4.997	4.997	4.997
0	4.998	4.996	2.007	4.996	4.996	4.996
4.998	0	4.996	0	4.996	4.996	4.997
4.998	5	0	0	0	0	0

4.2 Questions for 2-1B

4.2.1 Our NAND gate consists of 4 individual CMOS transistors. The four transistors are labeled M 1-4. Transistors M1 and M3 function as PMOS transistors and M2 and M4 function as NMOS transistors. The division of transistors forms a pull up network and a pull down network with PMOS in parallel as pull up network and NMOS in series as the pull down network. When M1 and M3 are input at least one digital low value at the gates an output of VDD will be our outcome. During this instance both M2 and M4 will be an open circuit and not conducting. When M1 and M3 are input digital high values at both gates the circuit will be an open circuit. During this instance both M2 and M4 will be conducting and produce ground voltage.

4.2.2

Logic level and Voltage output Table

Input A	Input B	M1	M2	M3	M4	Output
0 (0 V)	0 (0 V)	1 (4.997 V)	0 (0 V)	1 (4.997 V)	1 (4.997 V)	1 (4.997 V)
0 (0 V)	1 (4.998 V)	1 (4.997 V)	X (2.007 V)	1 (4.996 V)	1 (4.996 V)	1 (4.996 V)
1 (4.998 V)	0 (0 V)	1 (4.997 V)	0 (0 V)	1 (4.996 v)	1 (4.996 V)	1 (4.997 V)
1 (4.998 V)	1 (5 V)	0 (0 V)				

For our first test we applied 0 volts to both input A and input B. As a result of applying a digital low value the output at M1 and M3 was VDD. Additionally, M2 and M4 are open circuit and are not conducting, therefore the output of our CMOS is VDD.

For our second test we applied 0 volts to input A and 5 volts to input B. As a result of applying a digital low value M1 and M3 had an output of VDD, and M4 acted as an open circuit. During this particular test we got an undefined result for M2, as its output is a floating voltage/ invalid logic state. Since M2 was undefined our overall output for the CMOS was VDD.

For our third test we applied 5 volts to input A and 0 volts input B. As a result M1 and M3 had an output of VDD. Meanwhile, M2 and M4 acted as an open circuit, so the overall output for the CMOS was VDD.

For our fourth and final test we applied 5 volts to both input A and input B. As a result M1 and M3 were open circuit since they had a digital high applied to their gates. Additionally, M2 and M4 both conducted and produced ground voltage which was the overall output for the CMOS.

Conclusion

In this lab we observed the operating characteristics of MOSFET's, and measured the I_D versus V_{GS} and I_D versus V_{DS} curves for the 2N7000 MOSFET. Additionally, we explored the properties of a MOSFET bias circuit and learned how to build and analyze a CMOS logic circuit from individual transistors in a CD4007 transistor array IC.

Initially, we collected data and plotted the I_D versus V_{GS} characteristic for our MOSFET. At this point we were able to identify when our MOSFET turned on. Next, we ran four separate tests and set V_{GS} to a constant 1.5 V, 2 V, 2.5 V, and 3 V. We then plotted the I_D versus V_{DS} characteristic. The characteristic for $V_{GS} = 2.5\text{ V}$ was the data set that most resembled the curve that we were expecting. Through this data we were able to measure when the MOSFET was no longer in the cutoff region as well as find the boundary between the triode and saturation regions. We found through our tests that the IV characteristics of our n-type 2N7000 MOSFET didn't quite align with our expected results. We believe that this is solely a result of the lack of quality of our MOSFET and not due to any errors with the collection of our data.

In the final part of our lab we built and analyzed a NAND gate consisting of four CMOS transistors. Two of the transistors functioned as PMOS transistors and formed a pull-up network. The other two transistors functioned as NMOS transistors and formed a pull-down network. Through our tests and analysis we were able to confirm that our NAND gate CMOS were constructed correctly as the output of our tests aligned with our truth table predictions. The only outlier we had in our testing was with one of our NMOS transistors (M2) that output an undefined result (floating voltage) during one test.