ReRAM Compute ASIC Fabrication

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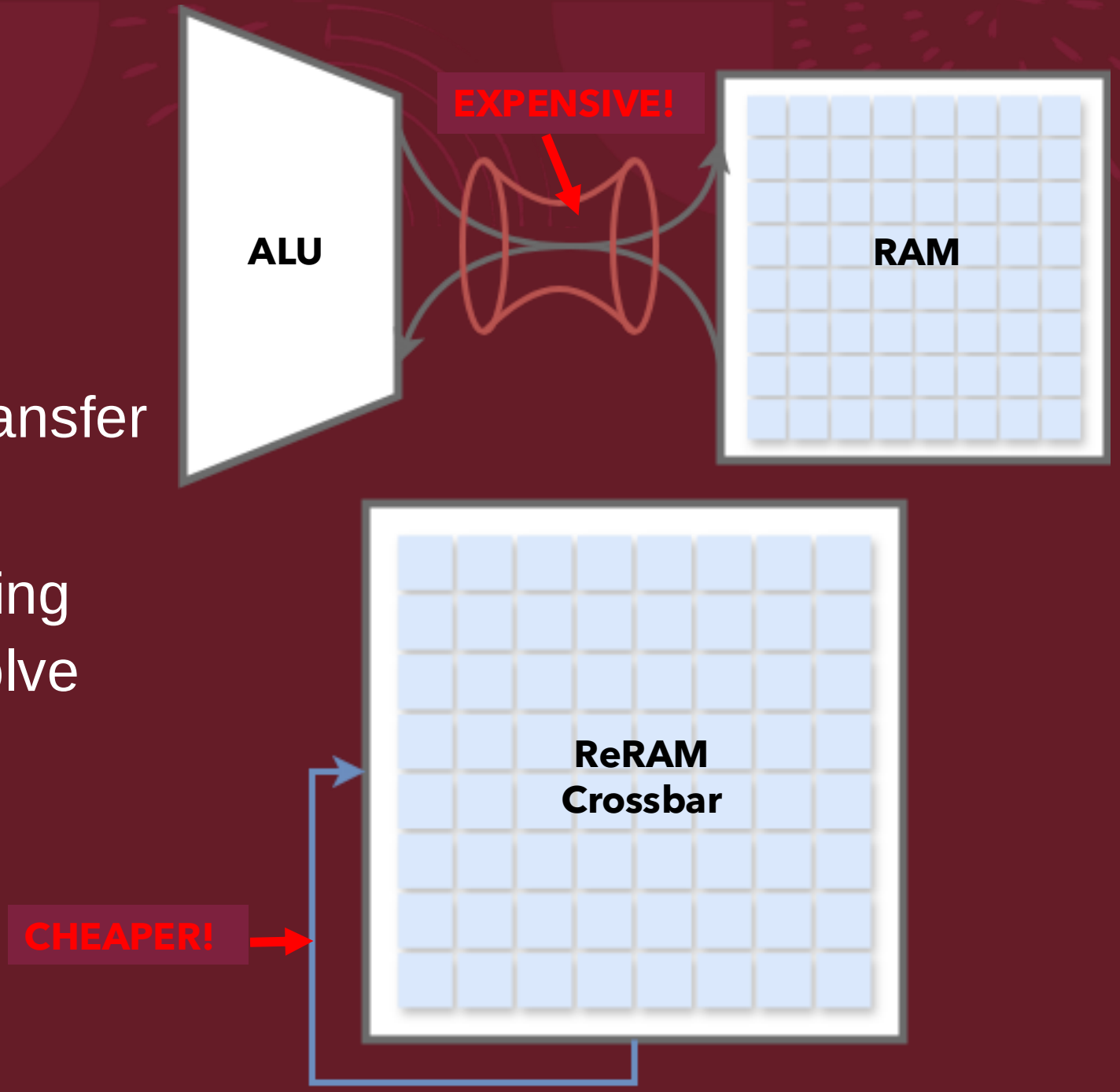
Client: Dr. Henry Duwe
Advisor: Dr. Cheng Wang

Project Overview

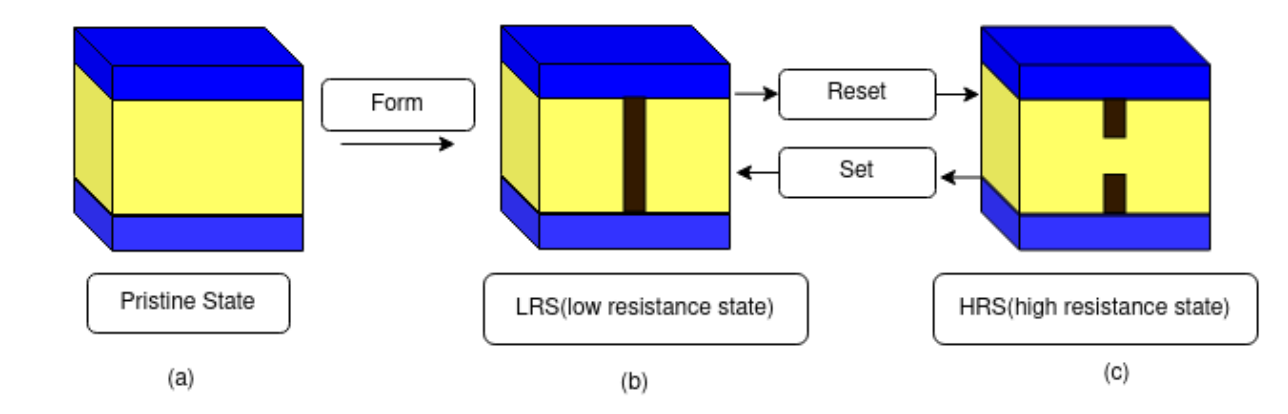
- Problem
  - ReRAM is an emerging memory technology
  - Not commercially available
  - Has the potential to be used in more efficient in-memory computation
- Goals
  - Create a research vehicle for silicon proving in memory computation utilizing ReRAM
  - Create documentation on our process and on solutions to common issues

Broad context

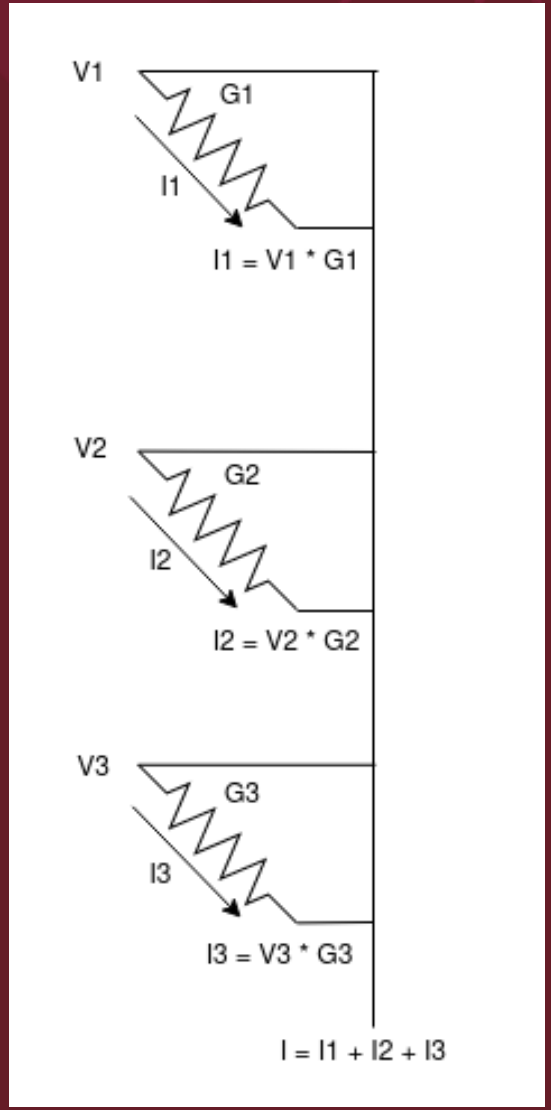
- Machine learning...
  - Bottlenecked by data transfer from memory to CPU
- In memory computation using matrix multiplication can solve the bottleneck



ReRAM



How ReRAM works



ReRAM MAC

ReRAM pros and cons

Pros	Cons
High memory density	Variation due to random noise
Non-volatile memory	Different manufacturing process
Low power consumption	Not an established technology
Ability to scale to smaller processes	

Still an active research area, hope to further enable solutions with this test chip

Users

- Graduate Students
  - Documentation on Efabless process and tool flow for use in research settings
- Undergrad Students
  - Easy to follow lab documentation
  - Gain the ability to bring up a chip in parallel with their regular coursework
- Professor Duwe and Professor Wang
  - Practical example of a crossbar for research and testing
  - Provide valuable resources for the co-curricular chip program

Requirements

- Functional Requirements
  - Design an 8x8 ReRAM crossbar that can perform matrix vector multiplication
  - Create an ADC with a sufficiently high resolution to distinguish between all possible MAC output values
  - 40 MHz clock speed
  - Fit within 1/8th the provided area
  - Characterization of peripheral circuits

- Non-functional Requirements
  - Project Documentation
  - Bring-up plan for testing the fabricated chip

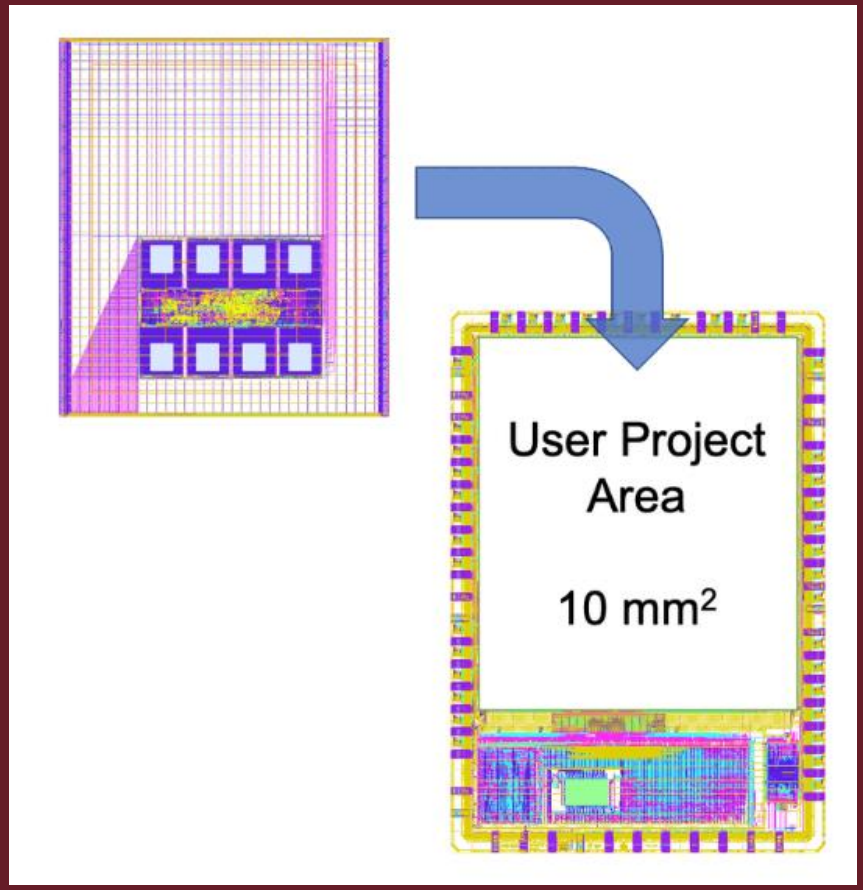
Efabless Fabrication

Efabless runs a shuttle program every few months

- Low-cost development
- Projects are required to be open-source
- Uses open Skywater 130nm process

Design Process

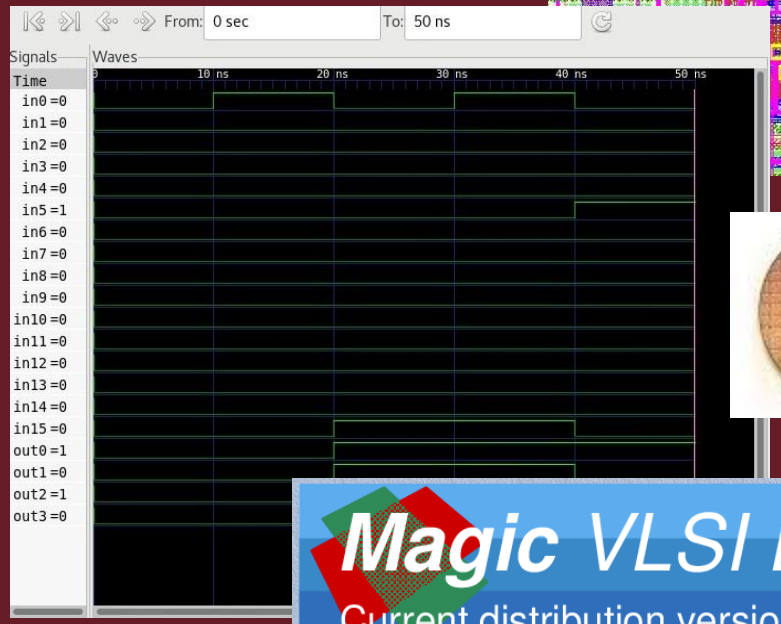
- Create a design
- Integrate it into the caravel harness
- Submit for fabrication



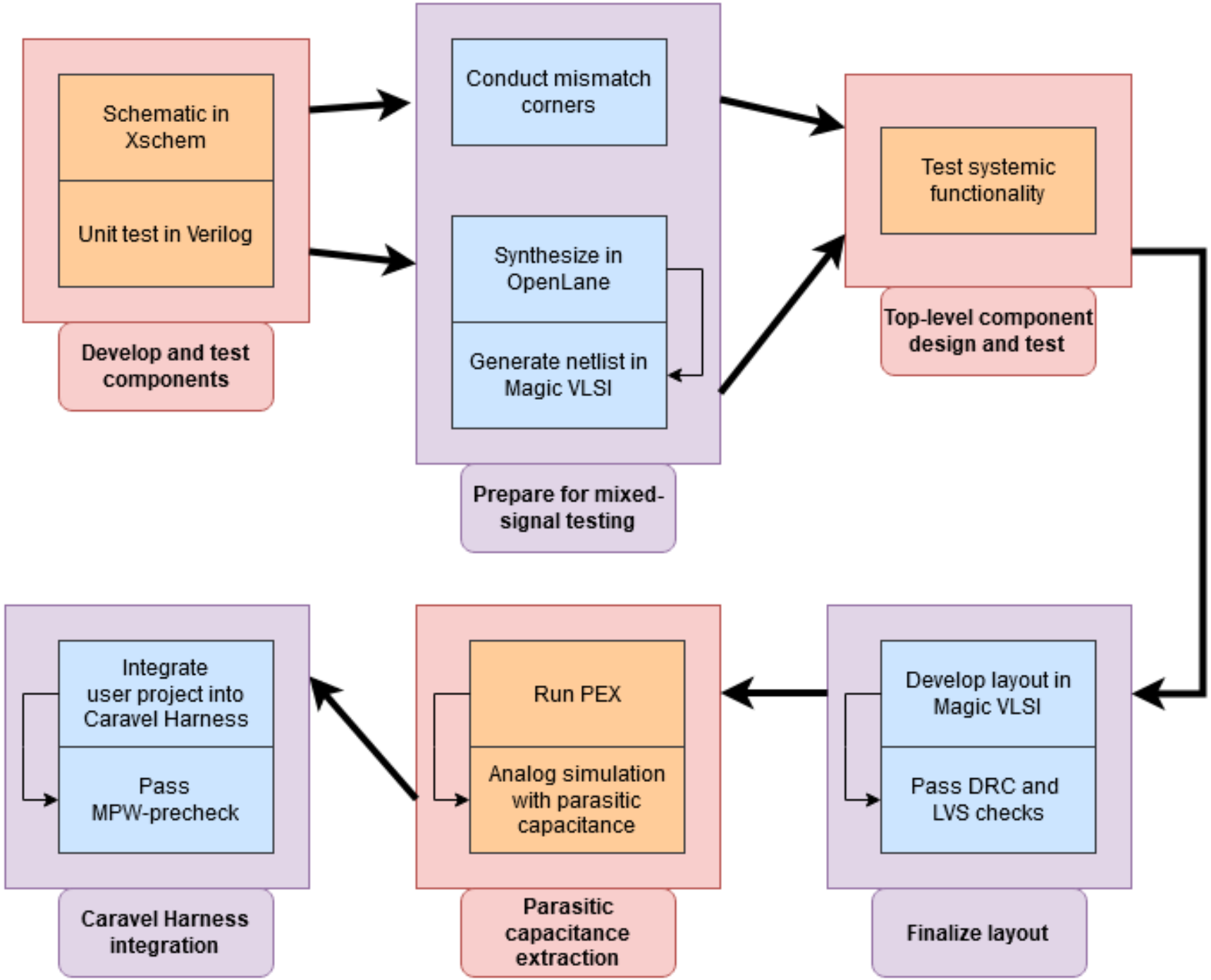
Source 1

Design Tools

- Xschem - Schematic capture
- Netgen – Used for LVS
- Ngspice – Spice simulator
- Magic - Layout creation
- Klayout – GDSII viewer
- GTKwave – Verilog waveforms

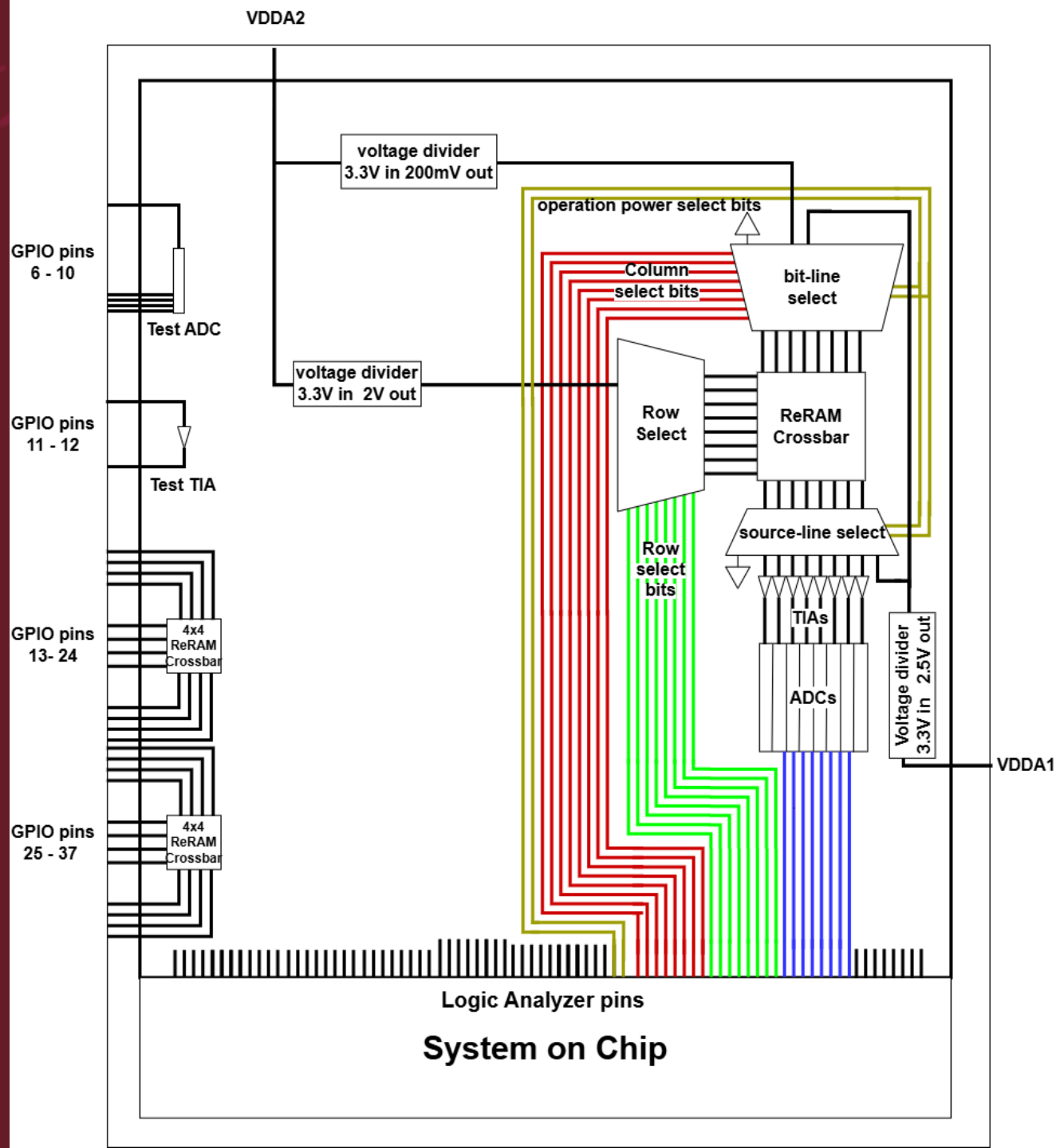


Efabless Design Flow



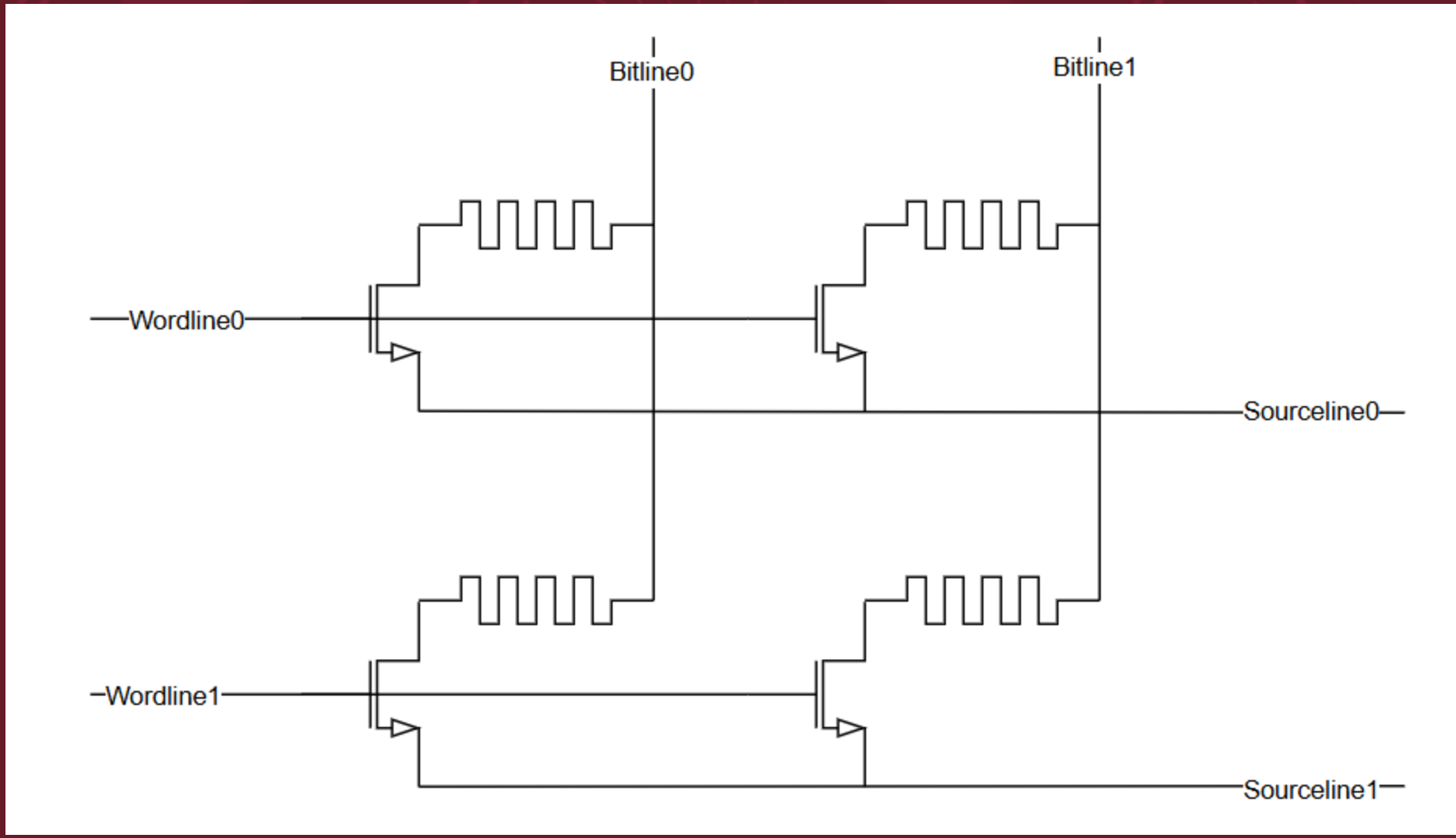
Top level design

- Control circuits – Logic analyzer, row, power, and column select, decides what operation is performed
- DAC – used during standalone operation
- Power select – selects the voltage values being used
- ADC and TIA network – Convert ReRAM analog output to a logic analyzer compatible digital output

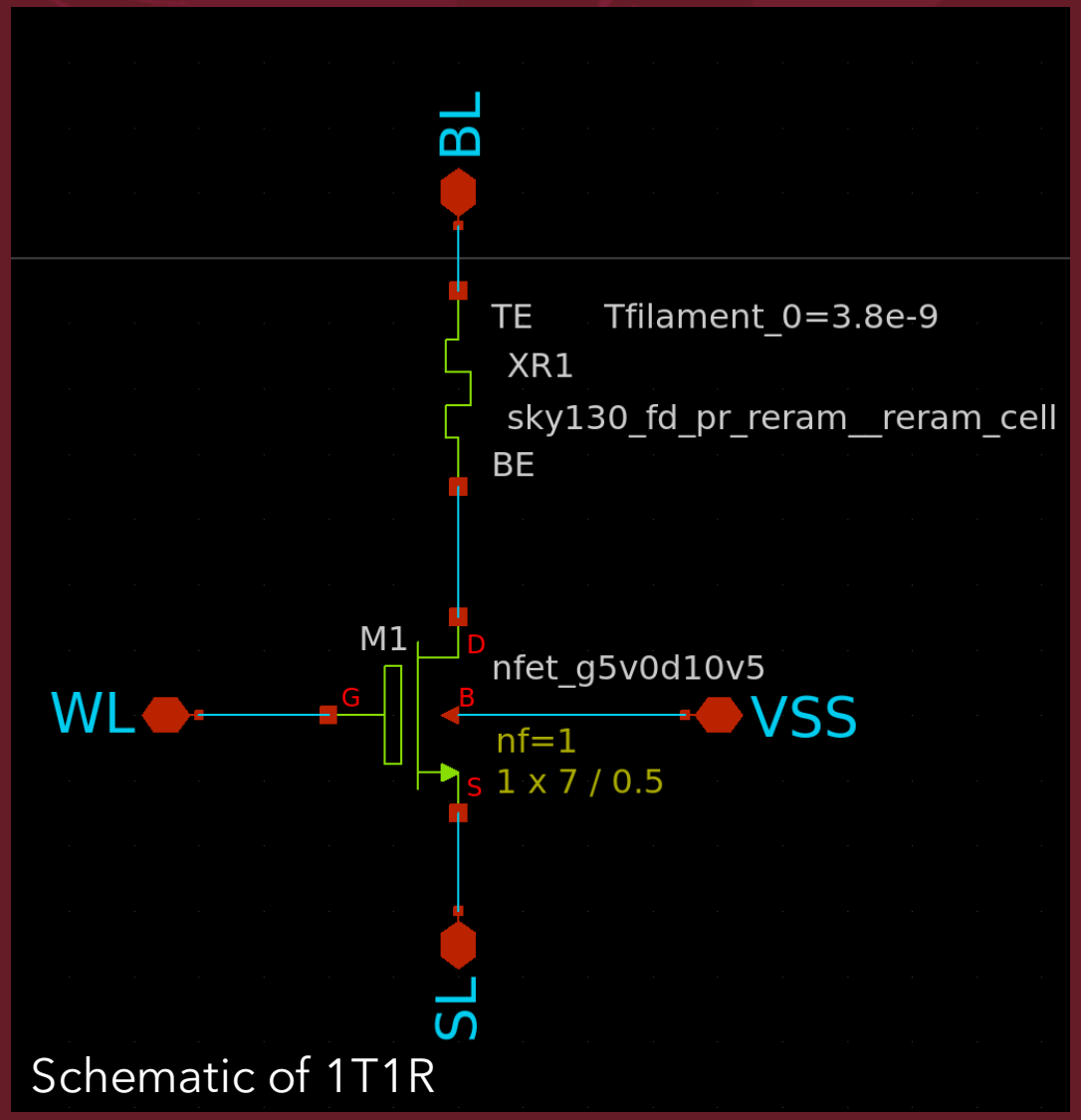


Crossbar

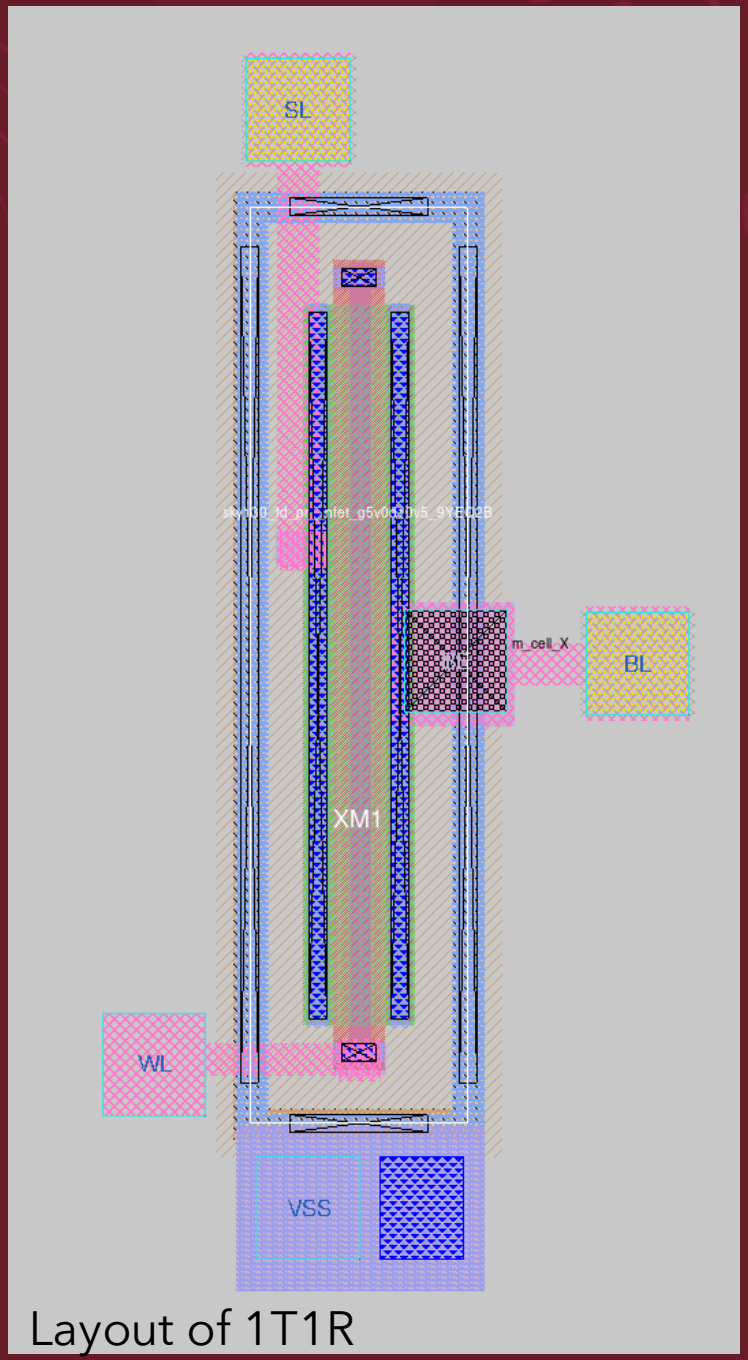
- 8x8 used for our design



The ReRAM cell



Schematic of 1T1R

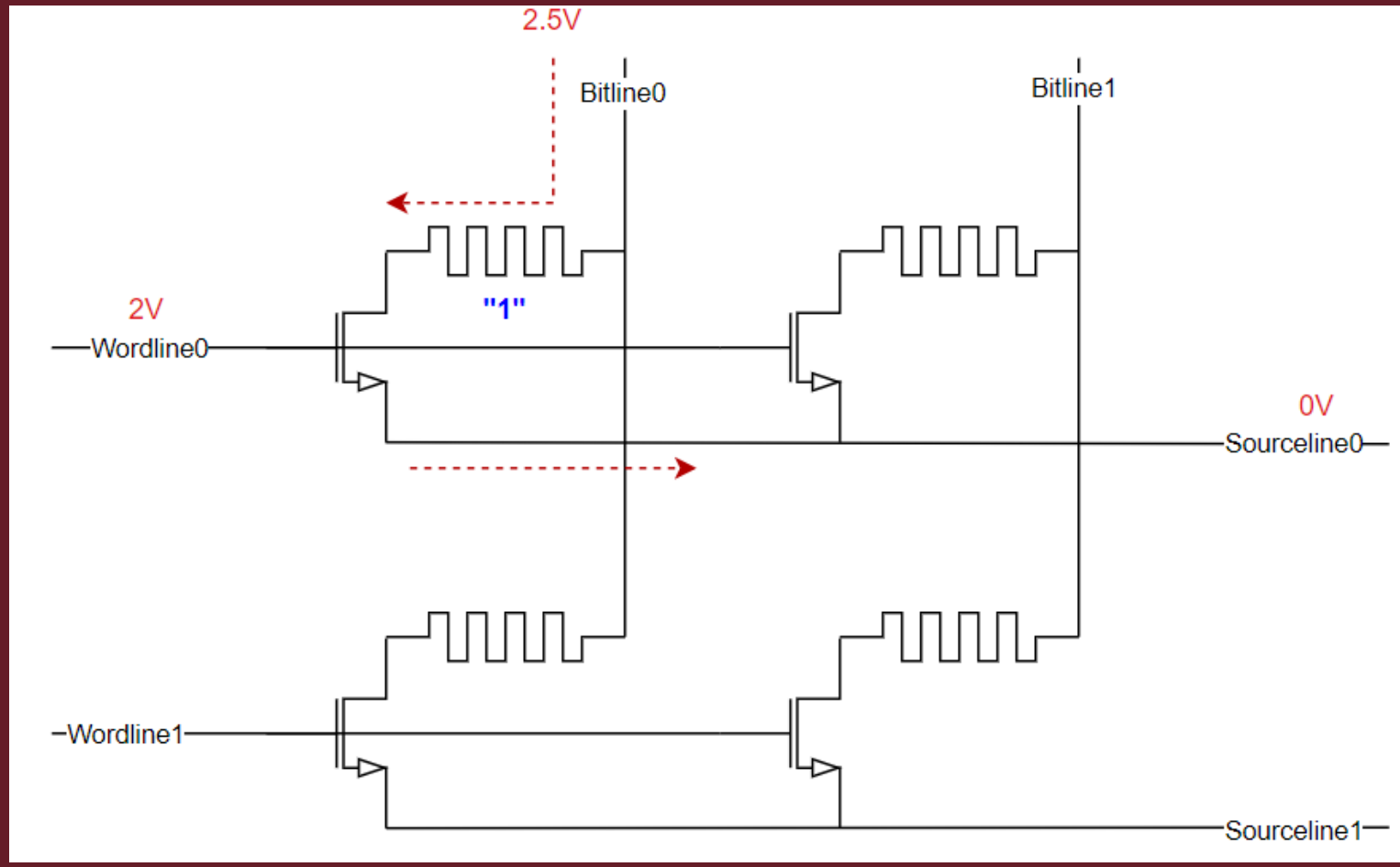


Layout of 1T1R

ReRAM operations

Write – set

- Positive voltage across the cell
- Wordline selects row

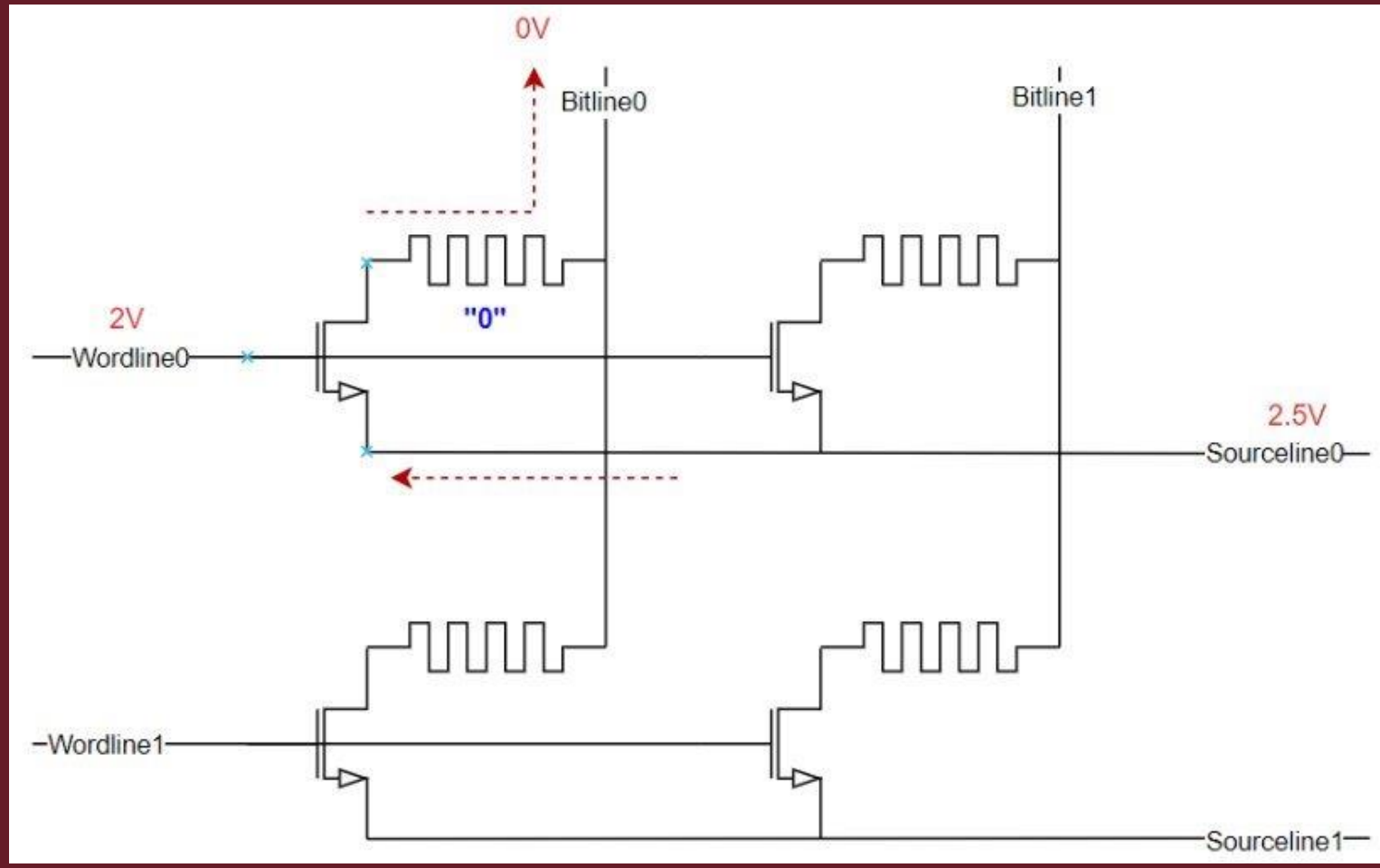


ReRAM set

ReRAM operations

Write – reset

- Negative voltage across the cell
- Wordline selects row

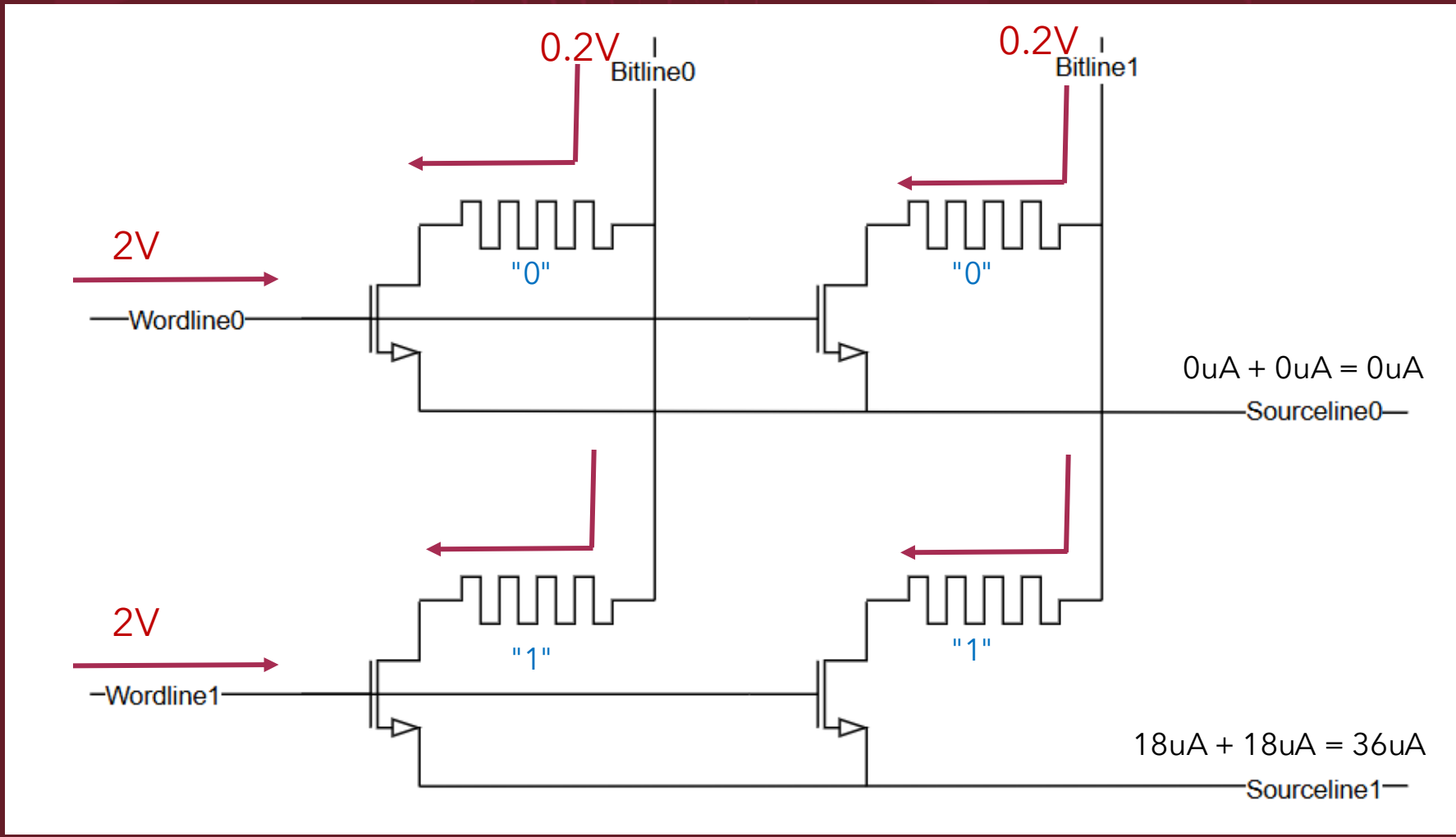


ReRAM reset

ReRAM Operations

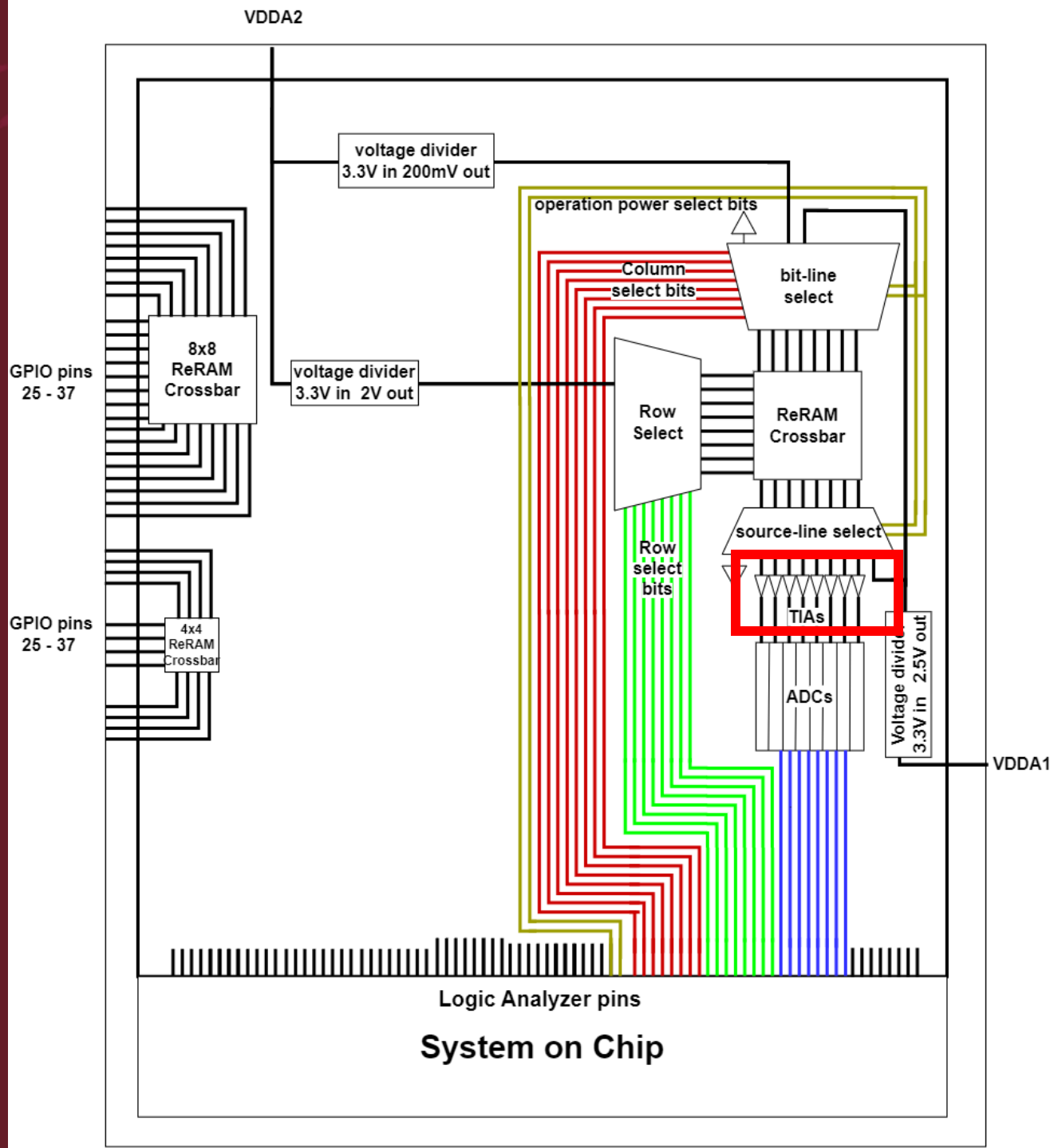
MAC/read

- Currents add
- Resistor multiplies
  - I = VG
  - G = 1/R



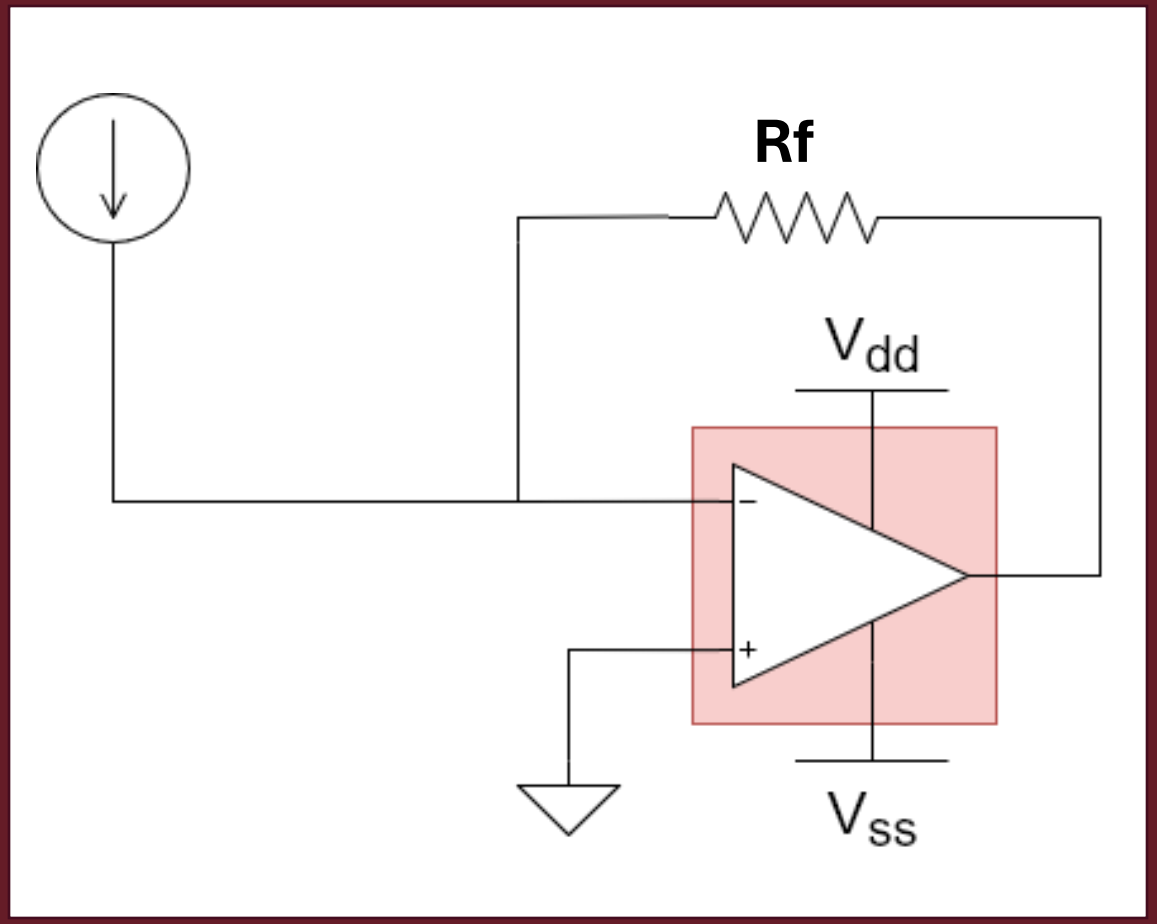
Trans-Impedance Amplifier (TIA)

- Converts input current to output voltage
- Desired TIA characteristics
  - Linear output
  - High trans-impedance gain
  - Low input impedance



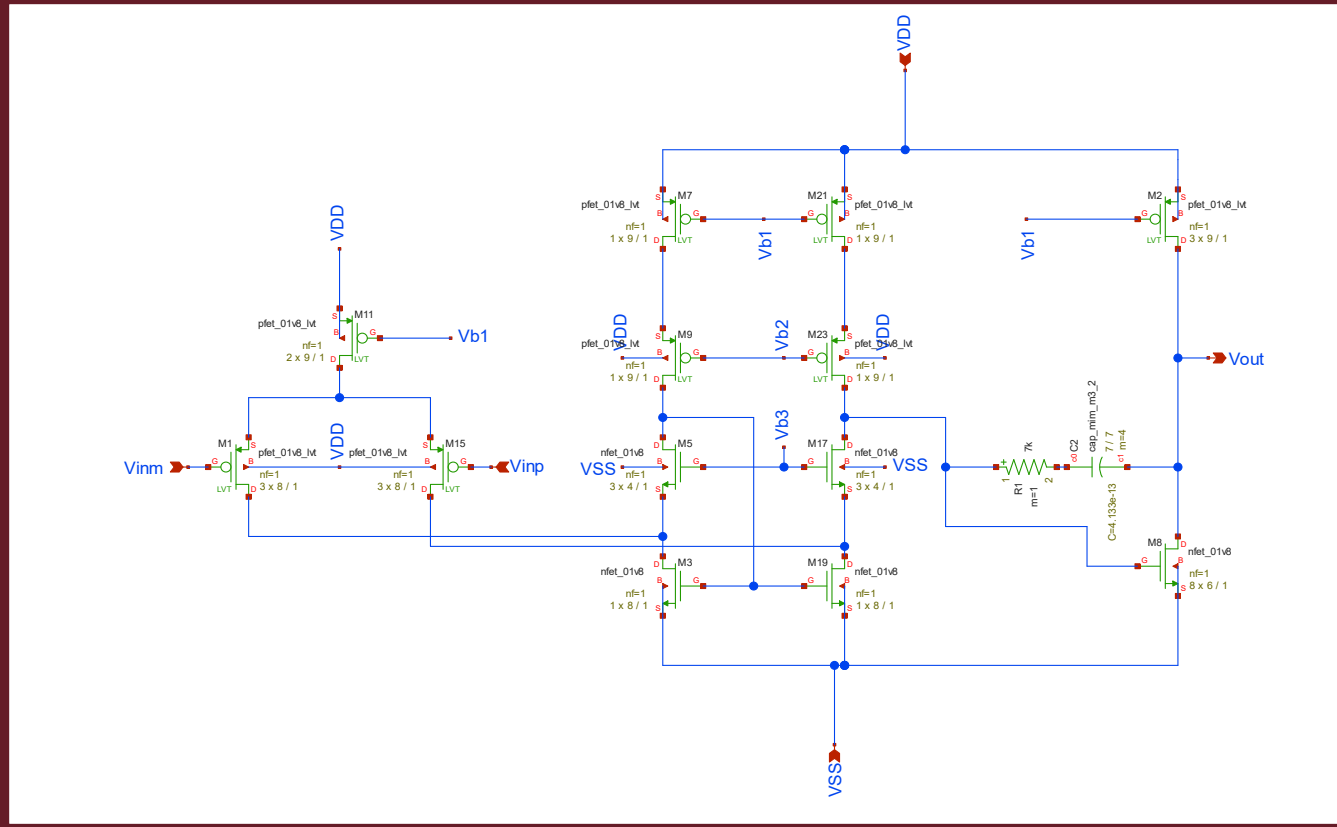
Trans-Impedance Amplifier (TIA)

- Op-Amp Architecure Considerations
  - 2 stage
    - Increased Gain
    - BW dependant on first



Trans-Impedance Amplifier (TIA)

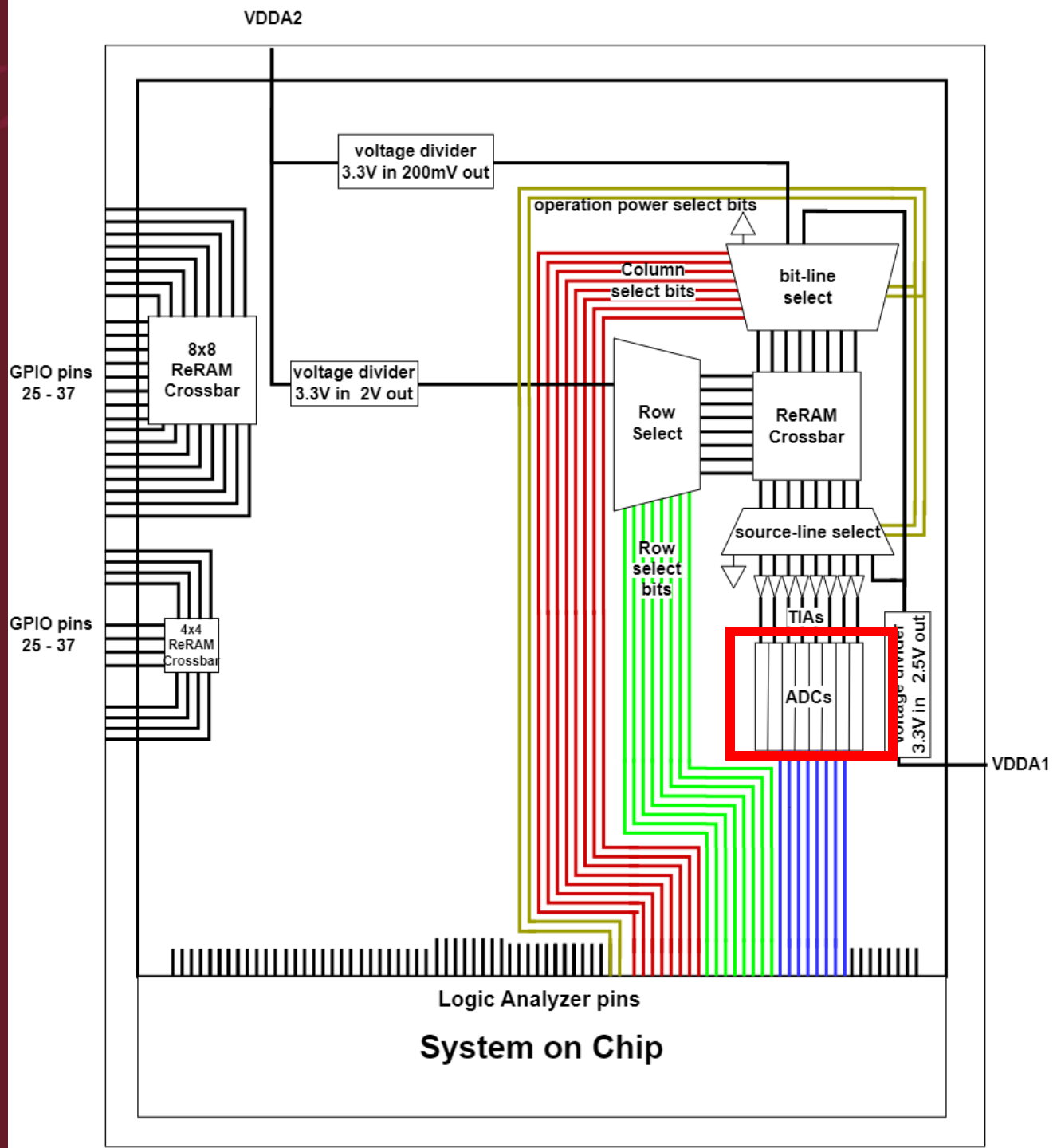
- Folded Cascode Architecure
  - Gain of 96.4dB
  - Phase margin of 58 degrees
  - Input Range 0 to 1.35V
  - Output range 0.2mV to 1.72V
  - Gain bandwidth product of 89MHz



Design doc:
Section 5.7.3 (Pg 26-27)
Sec 4.3.2 (Pg 18)

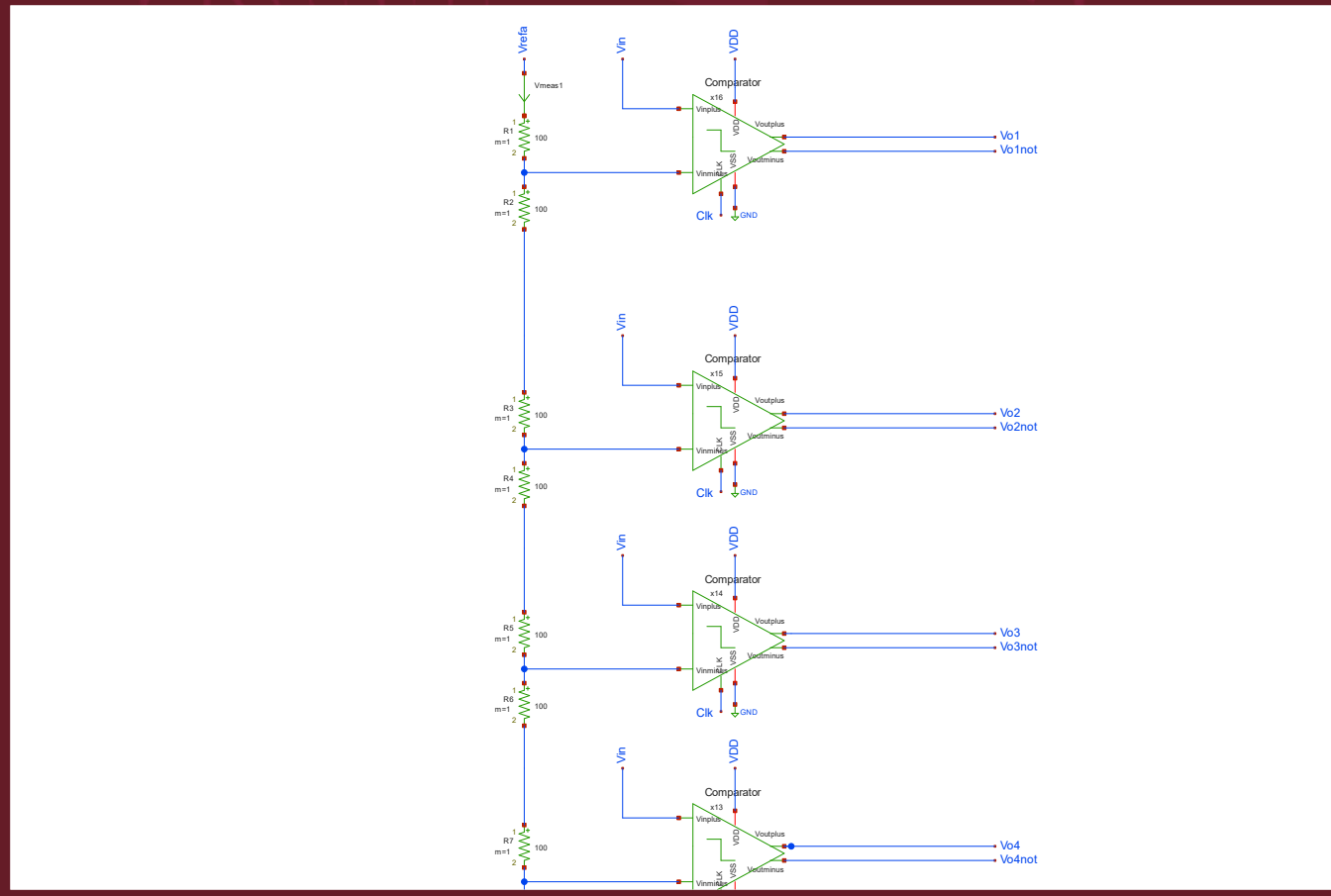
Analog to Digital Converter

- Converts analog voltage to digital code
- Desired ADC characteristics
  - Linear output
  - 4 effective number of bits (ENOB)
  - Sampling frequency of 40MS/s
  - No missing codes



Analog Digital Converter

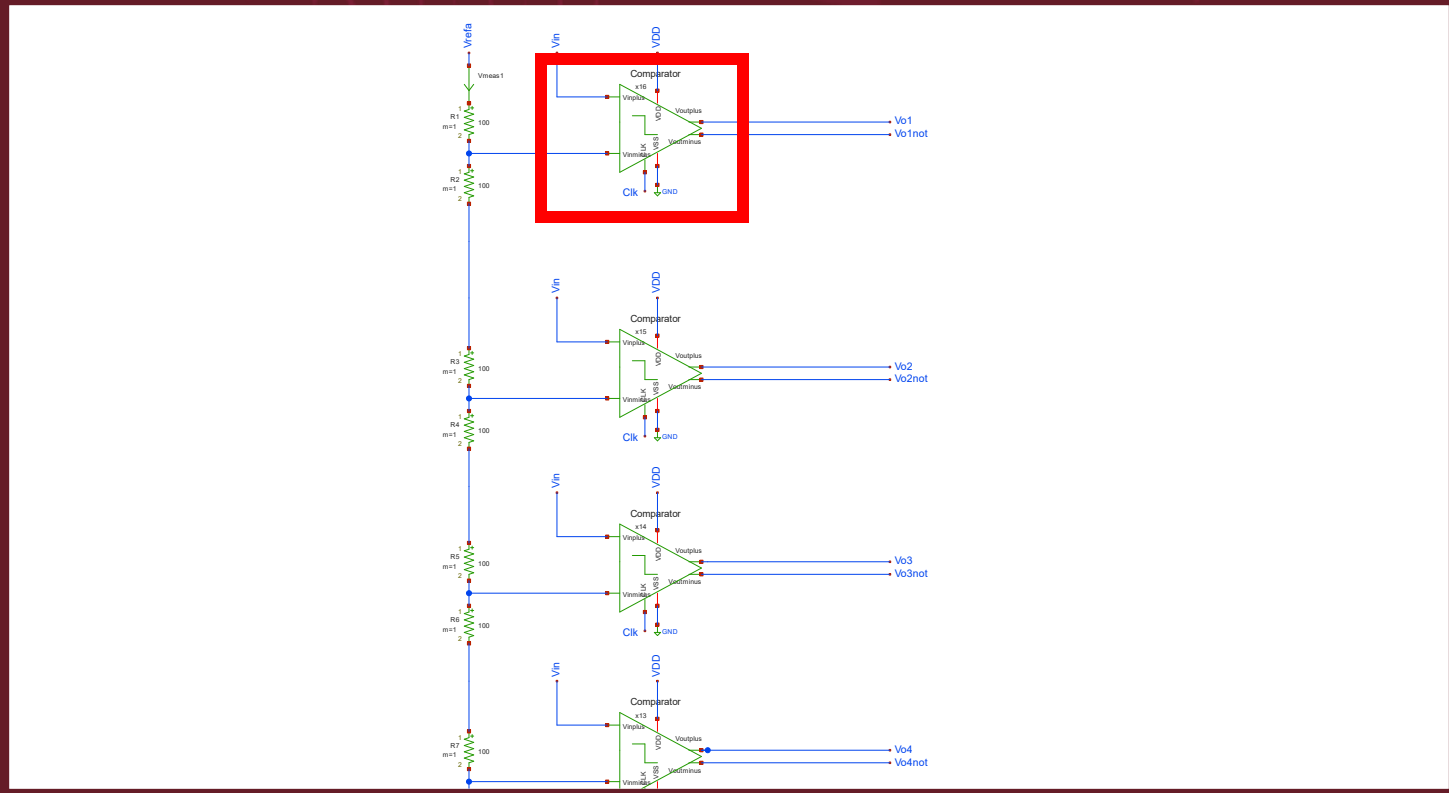
- Flash ADC
  - Simple
  - Fast
- 4-bit resoultion
- Integral non-linearity (INL) 0.62 LSBs
- Effective number of bits (ENOB) based INL 3.69
- Measured at 40MS/s sampling Rate



Design doc:
Section 5.7.5 (Pg 28-30)
Sec 4.3.2 (Pg 16-17)

Comparator

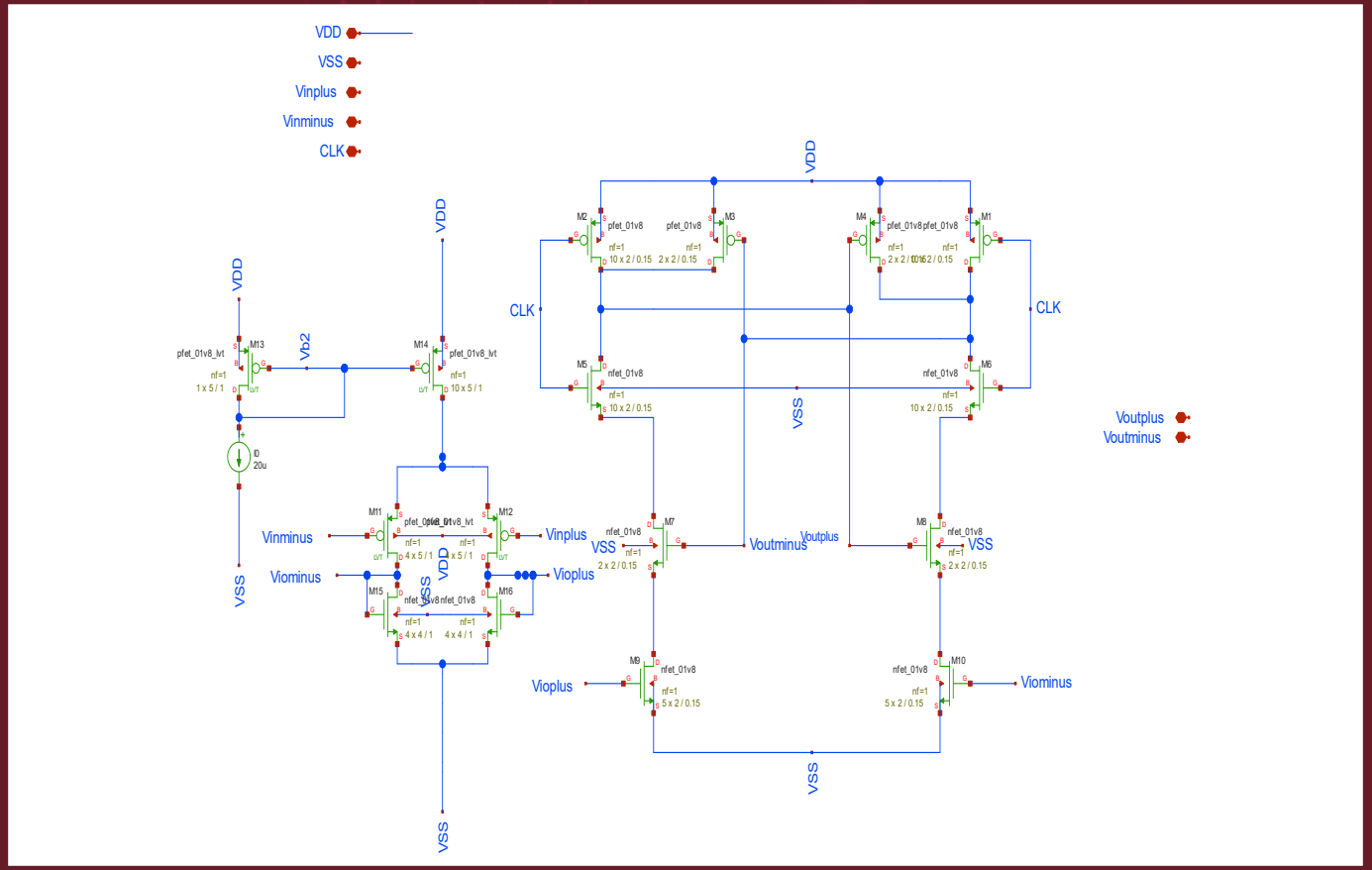
- Desired Comparator characteristics
  - Fast slew rate
  - Rail to rail outputs
  - High input impedance
  - Low offset voltage



Design doc:
Section 5.7.2 (Pg 25)
Sec 4.3.2 (Pg 17)

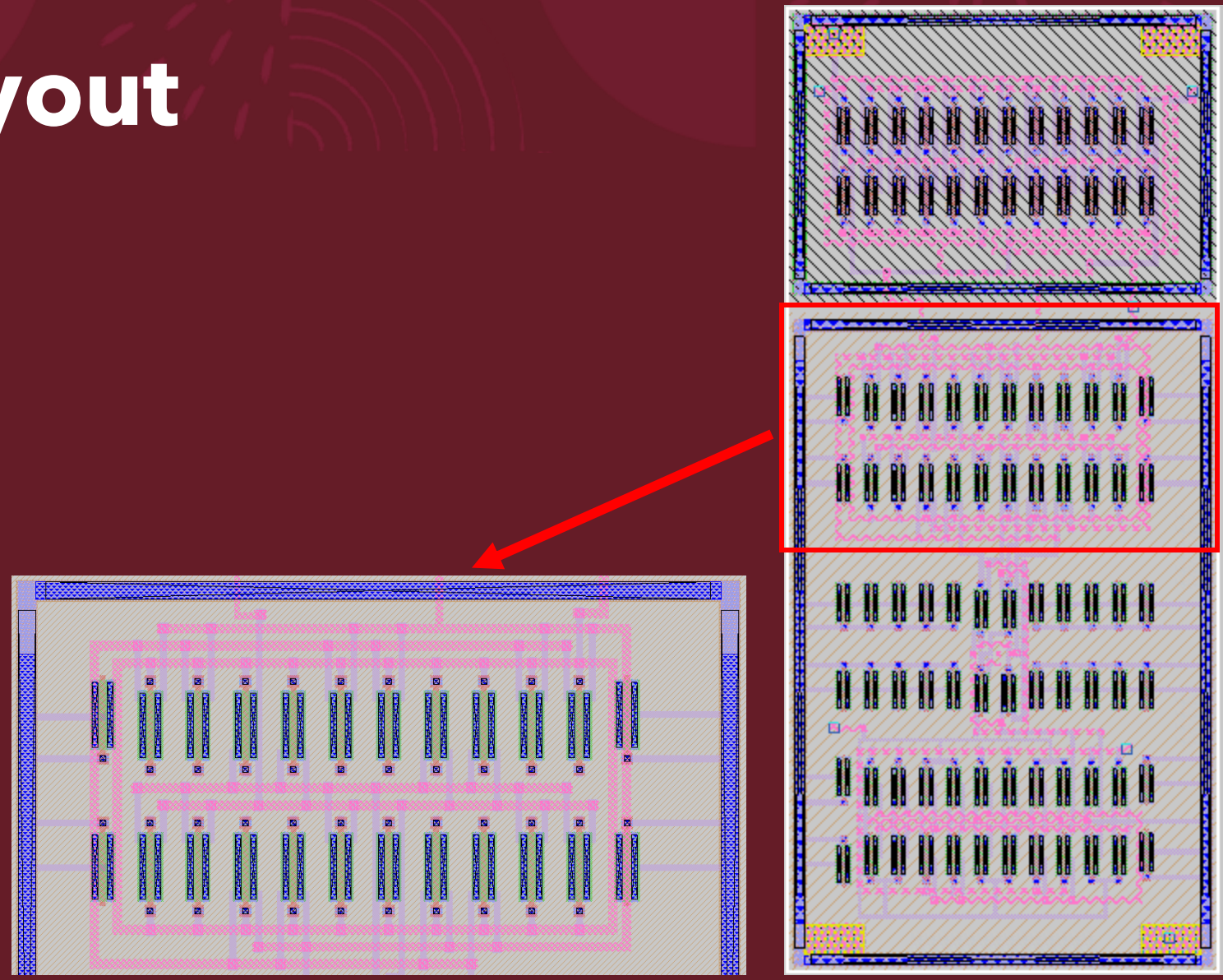
Comparator

- StrongARM Comparator
  - Zero static power consumption
  - Rail to rail outputs
  - Reduction in input referred offset voltage
- Results
  - Slew rate 1493.42V/us
  - Output range 0 to 1.8V



Comparator Layout

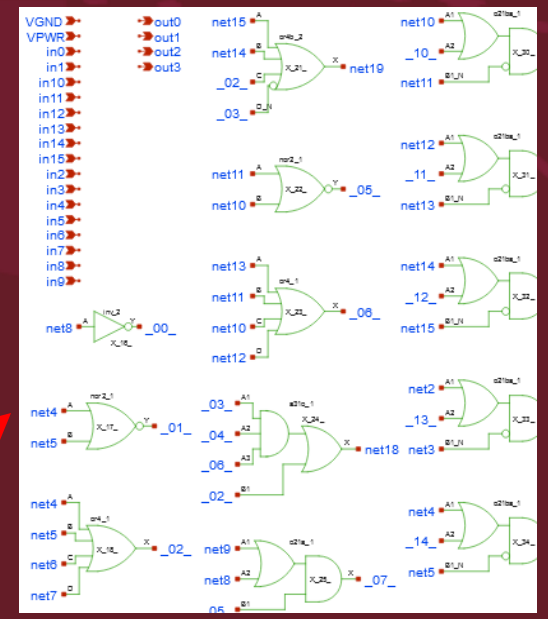
- Implemented using a common centroid approach
  - Approach aimed to decrease effects of mismatch
  - Requires parallel device interconnections and dummy devices
- Created a TCL script to assist device generation and placement in Magic VLSI
  - Not an ideal solution

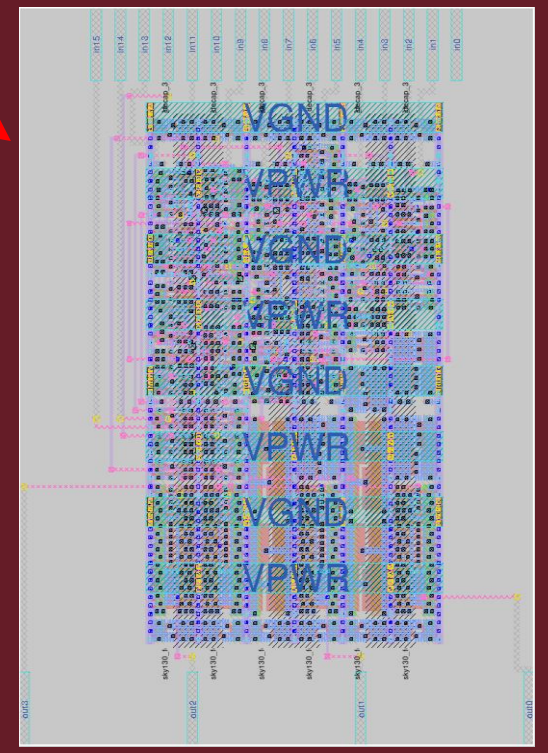


Priority Encoder

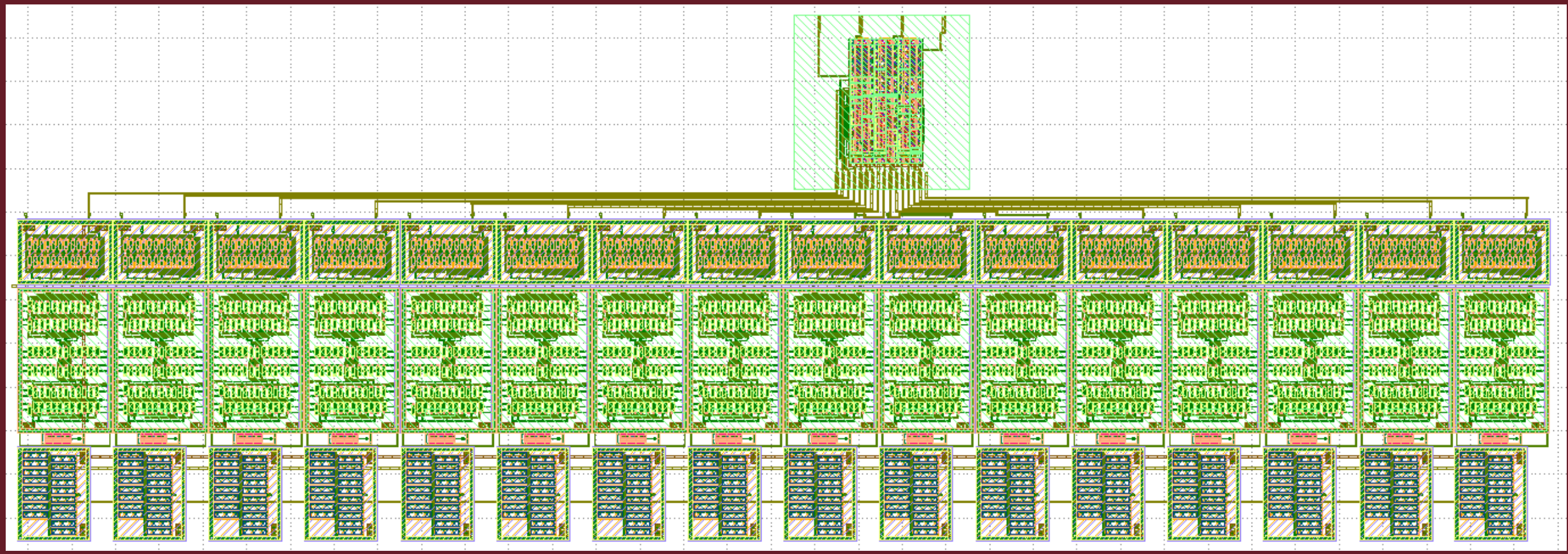
- Converts to binary encoding
- Fully digital component
  - Verilog to combinational circuit conversion achieved with an .awk script
  - Synthesized and hardened through Openlane

```
3  module Priority_Encoder_16t4 (
4
5      `ifdef USE_POWER_PINS
6          input VPWR,
7          input VGND,
8      `endif
9      input in0,
10     input in1,
11     input in2,
12     input in3
```



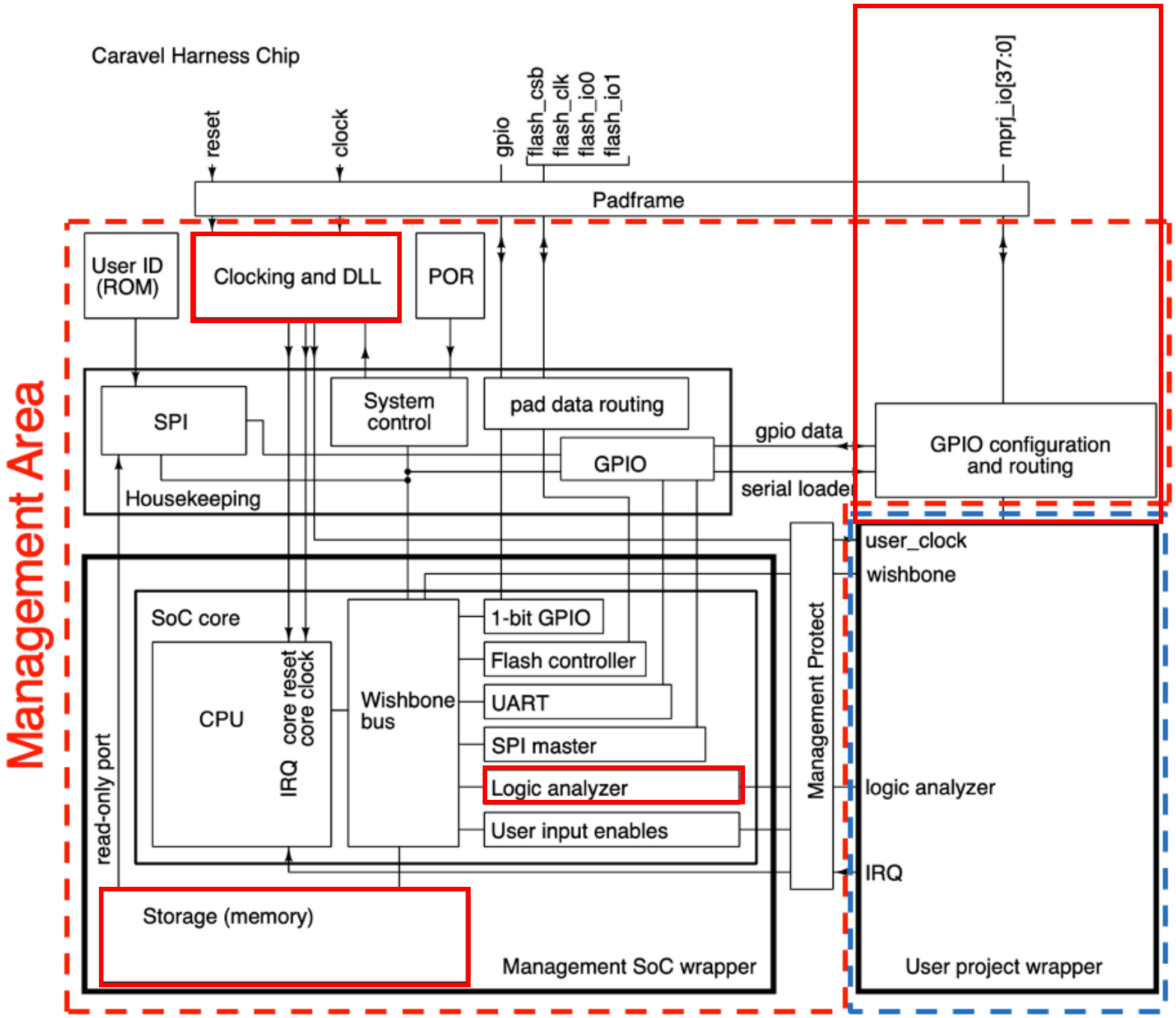


ADC Layout



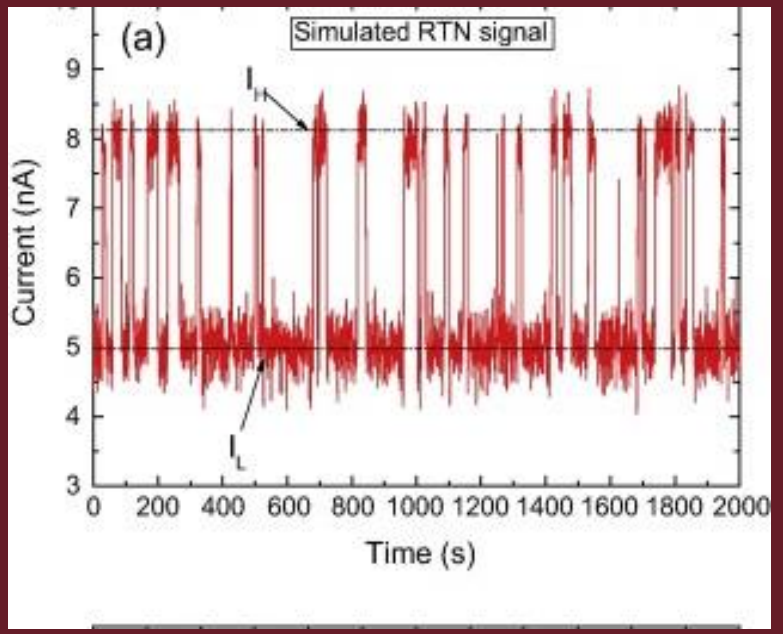
System on Chip

- The SoC includes multiple useful components for our application:
  - Riscv instruction set
    - Built in C compiler
  - Logic Analyzer
  - On chip memory
  - GPIO from the user space to off chip
  - Built counter/timer



Noise breakdown

- There are 4 sources of noise present in our device:
  - Thermal noise, shot noise, and flicker noise are not significant enough to effect our design
    - Skywater has clear temperature ranges for device operations
  - Random Telegraph Noise (aka burst noise)
    - The sky130nm technology uses halfnium-oxide memristors
      - Memristors like hafnium-oxide are more susceptible to RTN
  - Best way to effectively characterize noise in our device is to test the physical devices acquiring characterizations for it in the process.



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Risk Mitigation

- Memristor and CMOS Modeling Issues
  - Risk: Inaccurate device models caused by the use of binning models and BSIM4
  - Mitigation: Explore open-source SPICE models, document current issues, propose future solutions.
- Fabrication Errors
  - Risk: Fabrication defects that aren't attributed to our design
  - Mitigation: Detailed bring-up plan with testing methods, acknowledge limitations in preventing fabrication errors.

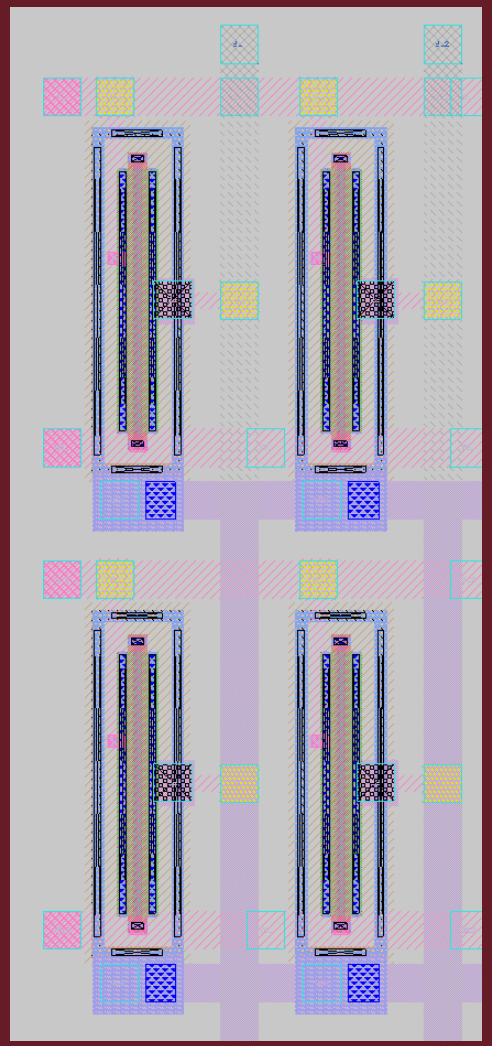
Conclusion

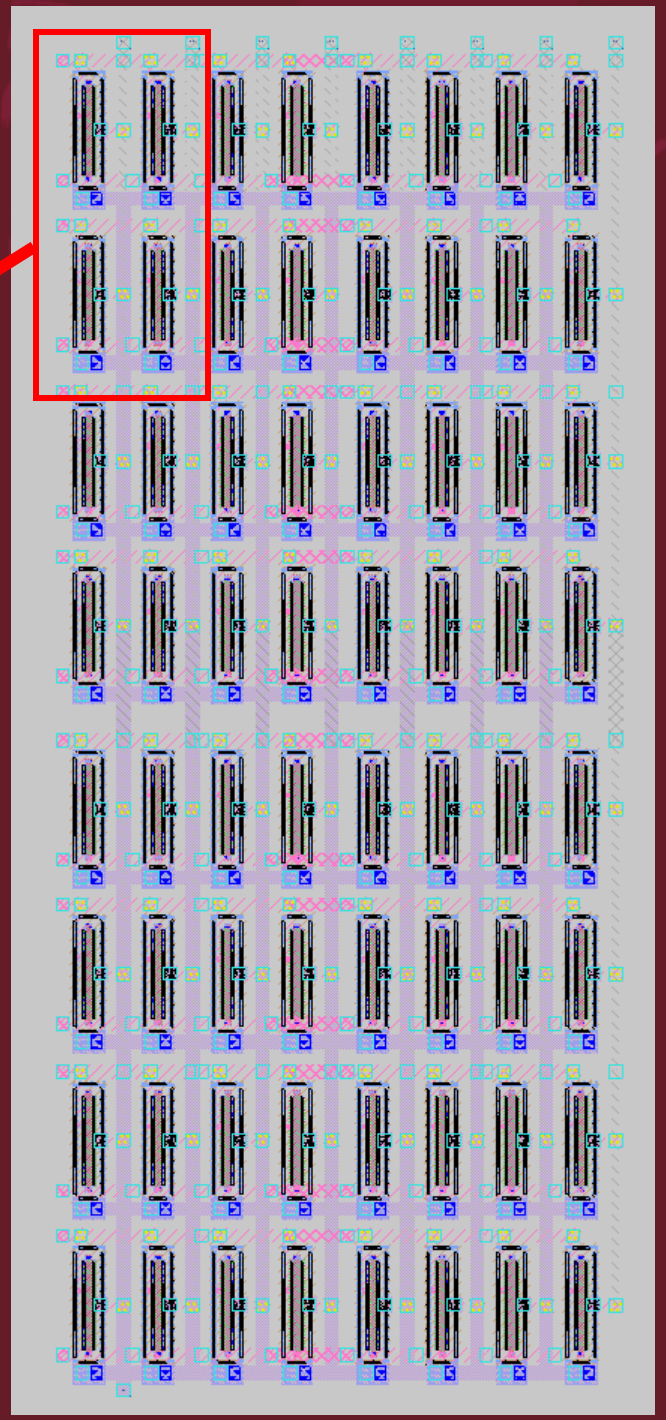
- 8x8 crossbar was designed and tested as well as being verified to pass precheck
- Created appropriate periphery devices to interface with the crossbar
- Created documentation on our design as well as solutions to any common issues to help reduce future teams struggles

Questions?

Supplementary Slides

8x8 Layout

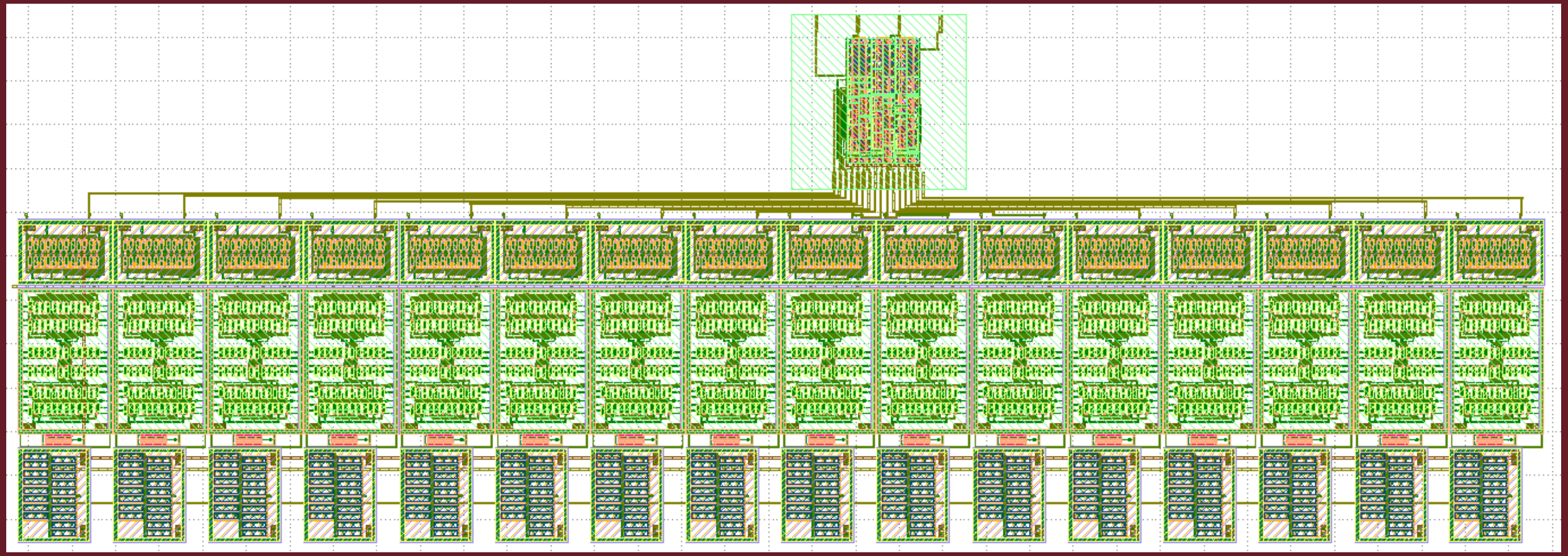




ReRAM Simulation Issues

- ReRAM is unable to be simulated correctly
- Due to transistor models inherently being hard coded as one directional
- See section 5.7.1 in the design document

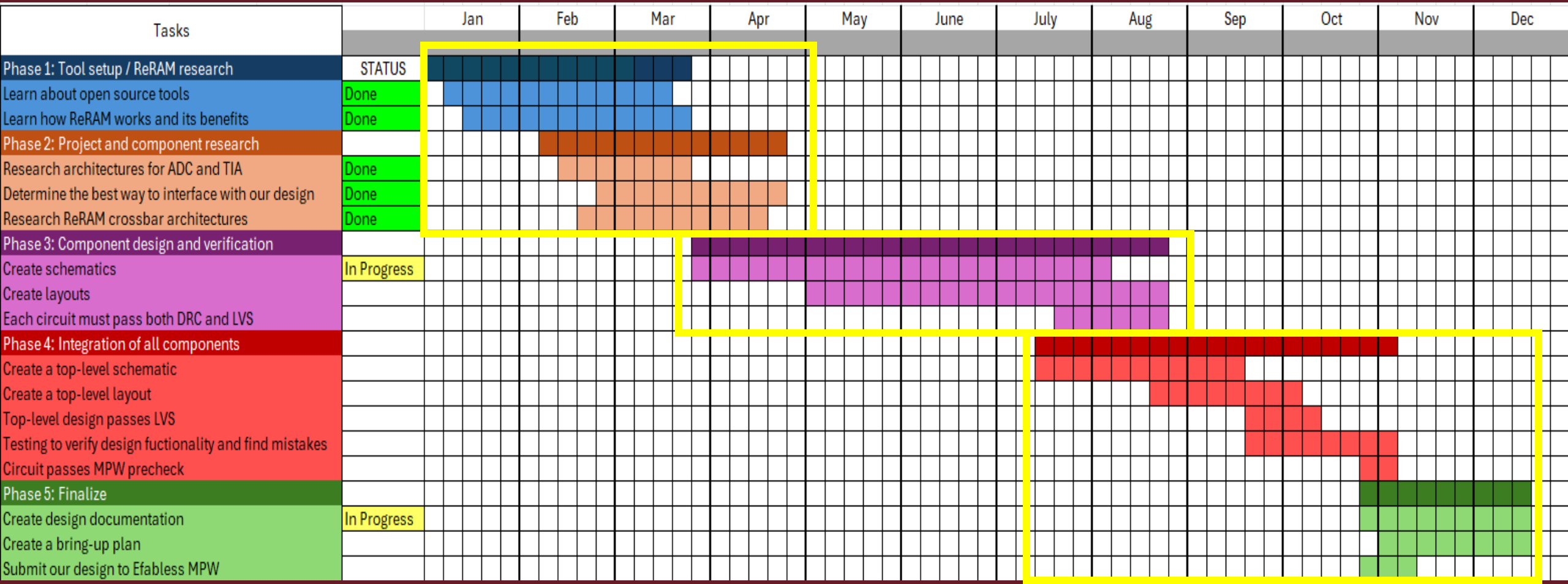
ADC layout



Definitions

- DRC : Design Rule Check
- LVS: Layout vs Schematic
- MPW: Multi-Project Wafer
- Efabless: Chip design company
- ReRAM: Resistive Random Access Memory
- ASIC: Application Specific Integrated Circuit
- ADC: Analogue to Digital Converter
- DAC: Digital to Analogue Converter
- TIA: Transimpedance Amplifier

Timeline


Tasks
Jan
Feb
Mar
Apr
May
June
July
Aug
Sep
Oct
Nov
Dec
Phase 1: Tool setup / ReRAM research
STATUS
Learn about open source tools
Done
Learn how ReRAM works and its benefits
Done
Phase 2: Project and component research
Research architectures for ADC and TIA
Done
Determine the best way to interface with our design
Done
Research ReRAM crossbar architectures
Done
Phase 3: Component design and verification
Create schematics
In Progress
Create layouts
Each circuit must pass both DRC and LVS
Phase 4: Integration of all components
Create a top-level schematic
Create a top-level layout
Top-level design passes LVS
Testing to verify design fuctionality and find mistakes
Circuit passes MPW precheck
Phase 5: Finalize
Create design documentation
In Progress
Create a bring-up plan
Submit our design to Efabless MPW

Contributions – Gage Moorman

- ADC design and test
- TIA design and test

Contributions – Konnor Kivimagi

- Fixed ReRAM precheck issues
- Analog tool setup
- Designed and simulation of the ReRAM crossbar

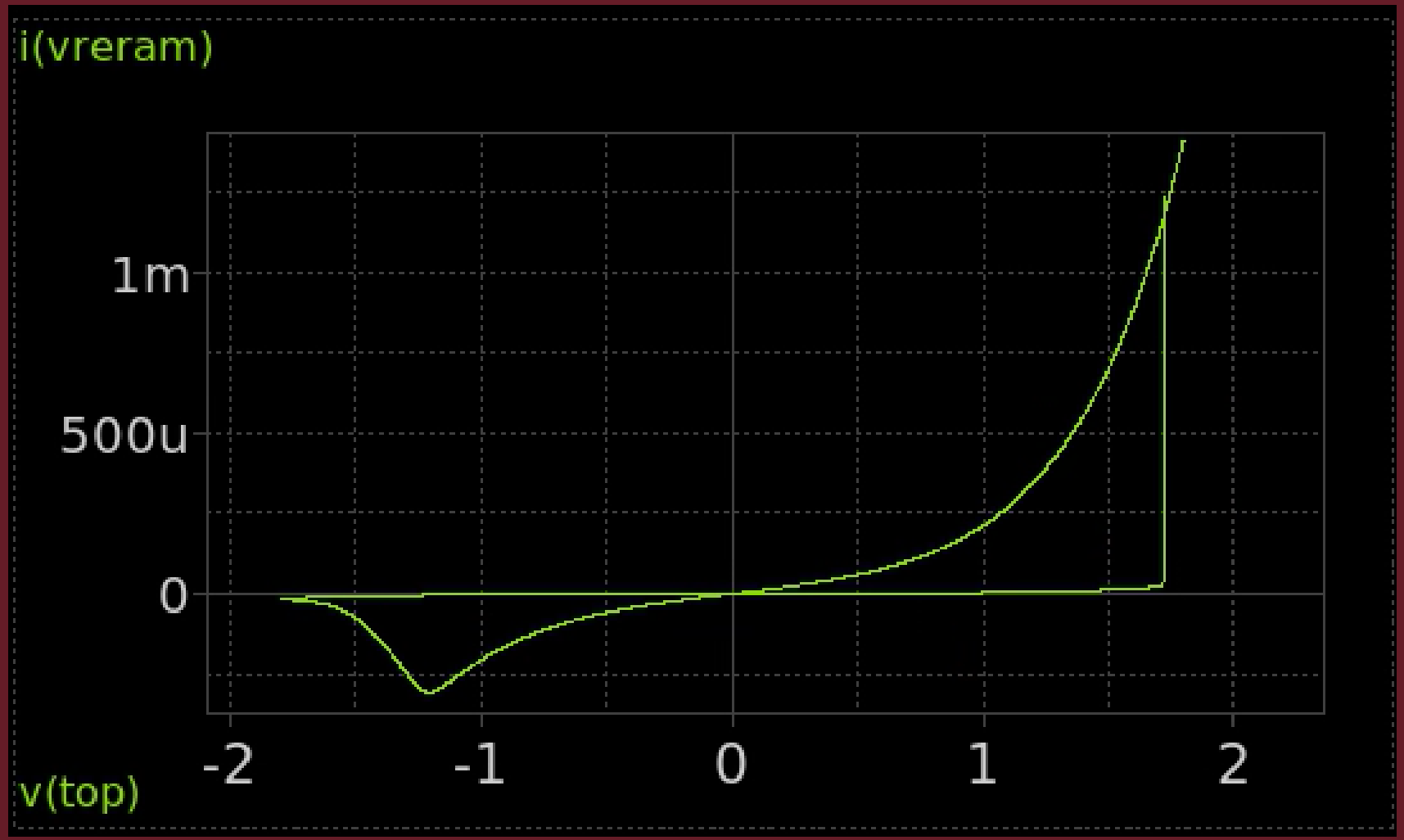
Contributions – Nathan Cook

- Noise analysis
- SoC integration
- Embedded Code development

Contributions – Jason Xie

- Analog layout
- Digital tool setup

ReRAM IV Curve



Sources

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3) http://opencircuitdesign.com/magic/
4) https://semiwiki.com/semiconductor-manufacturers/tsmc/287672-in-memory-computing-for-low-power-neural-network-inference/
5) Tony Chan Carusone, D. Johns, and K. W. Martin, *Analog integrated circuit design*. Hoboken, Nj Wiley, 2012.
6) B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 7, no. 2, pp. 12-17, Spring 2015, doi: 10.1109/MSSC.2015.2418155.
7) https://www.sciencedirect.com/science/article/pii/S0038110115002385