SETR 22/23 Mini-project

Resit Period

Prototyping a "smart" I/O module for the Industrial Internet of Things (IIoT) using Zephyr

Introduction

The aim of this short project is to implement simple Input/Output sensor/actuator modules, which are core parts of modern IoT and IIoT applications.

The embedded I/O module is based on the Nordic nRF52840 Devkit used in the lab classes, using the Zephyr RTOS. The firmware shall be structured according to the real-time model.

The "smart" adjective appears in the (nowadays) conventional sense (i.e. programmable/flexible node), not meaning that it incorporates AI/ML/...

In a more realistic situation, the wireless radio of the DevKit would be used, e.g. via the BLE protocol. However, adding BLE is not trivial (it is not "rocket science", but it takes a few 100's of lines of code and a few hours of effort to learn how to use it), so the interface to the I/O module is made via UART. Note that, if the firmware is properly implemented (i.e. following a modular architecture), moving from the UART interface to BLE would be straightforward.

Specification

The smart I/O module comprises the following inputs and outputs:

- 4 analog inputs. It is used the internal ADC and mux. A 10 kOhm potentiometer is connected to each one of the AN inputs AN{1,2,4,5}, simulating an analog sensor
- 1 analog output. It shall be implemented a PWM-based DAC. The PWM output is filtered by a low-pass filter, to obtain the DC component (proportional to the duty-cycle), while removing (or better, attenuating) the PWM fundamental and harmonic frequencies.

> **NOTE**: The devkit supply (VDD) is 3 V. Feeding an input pin with a voltage higher than 3 V can destroy the devkit. Use the internal power supply (VDD and GND at connector P1) to supply the potentiometers. To have visual feedback of the analog output you can use a LED in series with a resistor. Use a small amount of current (e.g. 10 mA).

According to the real-time model, external read and write operations are carried out asynchronously. That is, when the external computing device (a PC) sets an output value or reads an

input value, it accesses a Real-Time Database (RTDB). This RTDB is, concurrently, accessed by internal real-time periodic tasks that keep it synchronized with the I/O interfaces. Refer to Figure 1 for an overview of the overall system architecture.

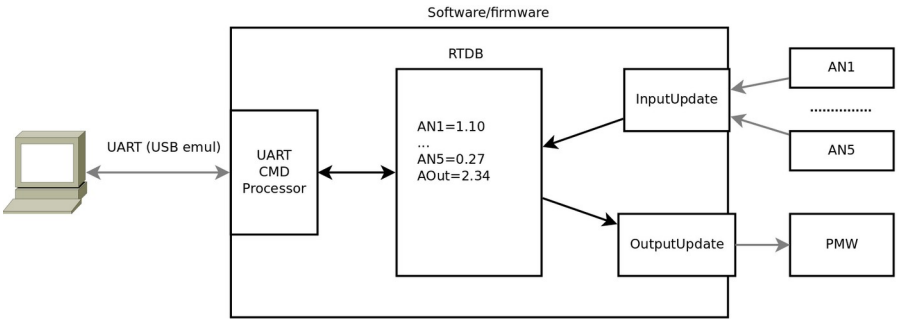

Figure 1: Smart I/O system architecture overview

The UART interface should allow configuring the relevant operational parameters of the I/O's, namely:

- Frequency of update of the analog inputs;
- Frequency of update of the analog output.

As mentioned above, the interface with the "outside world" is made through the UART. A set of commands should be defined to allow configuring the board, set the output value and read the inputs. Analog output and inputs are handled as a voltage comprised between 0.00 V and 3.00 V.

Tasks should have suitable activation modes and use adequate IPC mechanisms.

Note 1: the emphasis of this work is on structuring the software according with the real-time model. A solution using one loop with all functionality inside it will be evaluated with 0 (zero), even if "it works".

Note 2: the global quality of the solution is relevant. This includes e.g. documenting the code, using unit testing (at least for key parts), using suitable activation methods and synchronization protocols for tasks and developing a robust protocol for the UART communications, to name just a few.

Deliverables

- A two to three pages report, pdf format, submitted via eLearning, with:
  - Page 1:
    - Identification of the course and assignment
    - Link to GitHub project repository containing the project code

- Pages 2/3:
  - Brief description (diagrams and text) of the tasks, its execution patterns and relevant events
  - Real-time characterization of the tasks and a discussion of the system schedulability

Schedule

- The report must be submitted by email (pbrp@ua.pt), no later than the beginning of the theoretical exam.
- The application will be presented and demonstrated immediately after the theoretical exam.
- Technical questions about all aspects of the work can be asked during the presentation/demonstration, and the corresponding answers are part of the assessment.