14. MIPS Datapath Quiz

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Sample AI Tool Declaration
I used [AI tool name, e.g., GPT-4.1] to [describe specific uses: e.g., generate ideas, format paragraphs, improve expression, analyse effectiveness, create images and illustrations, produce drafts, refine, and/or finalise my assignment]. I am responsible for the content and quality of the submitted work.

- Due 15 Sep at 23:59
- Points 15
- Questions 15
- Available after 9 Sep at 18:00
- Time limit None
- Allowed attempts 3

Instructions

This quiz covers the L11 and L11a Datapath lecture videos. Lecture 11a can be found in the same PPTX/PDF file as Lecture 11.

Take the quiz again

Attempt history

	Attempt	Time	Score
KEPT	**Attempt 2**	20 minutes	12.93 out of 15
LATEST	**Attempt 2**	20 minutes	12.93 out of 15
	Attempt 1	99 minutes	11.31 out of 15

Correct answers are hidden.

Course chat

Score for this attempt: 12.93 out of 15
Submitted 9 Sep at 23:30
This attempt took 20 minutes.

Question 1
1 / 1 pts

For the following questions, fill in the stages of instruction execution with

(fetch, decode, alu, memory, register write)

A. register write : The instructions writes the result to the register i

j remain idle as they have nothing to be written into the registers.

B. alu : This is also called the execution stage where the

calculation, etc.) is done.

C. decode : The opcode, register numbers and other fields a

data in these registers are also read and passed to the next stage.

D. fetch : The instruction is taken from Instruction memory using PC and placed inside the

instruction register.

E. memory : Using the memory address calculated from the previous stage the data memory is read or

written. Only load/store instruction performs this stage, whereas other instructions remain idle in this stage.

Answer 1:
register write
Answer 2:
alu
Answer 3:
decode
Answer 4:
fetch
Answer 5:
memory

Question 2
1 / 1 pts

What is the output of each stage of execution?

Fetch

32-bit instruction in binary

Decode

Operand 1 and Operand 2 for

ALU

The result computed by the A

Memory

The data read from memory. I

RegWrite

No output, only the data from

Question 3

1 / 1 pts

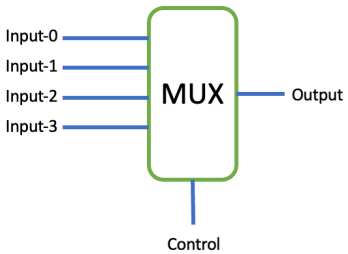
The 6-bit opcode is responsible for generating the control signals in various stages. You will learn how the control signals are generated from opcode in your control path lecture.

- True
- False

Question 4

1 / 1 pts

Say TRUE or FALSE:



The control signal for this multiplexer needs to be represented by 2-bits as there are 4 inputs. Example: 00 will choose the input-0 as output, 01 will choose the input-1 as output, etc.

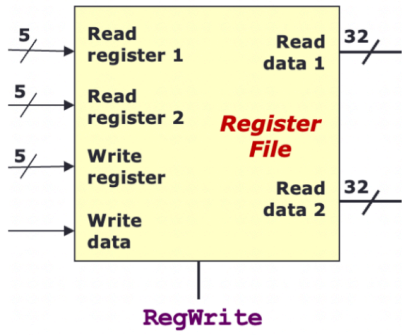
- True

False

Question 5

1 / 1 pts

Answers the following questions with respect to the register file and the values of the registers as shown below:



Register Name	Values in Decimal
$8	100
$9	200
$10	300
$11	400

A. When the 5-bits to Read Reg1=01000, Read Reg2=01001, Write Reg=01010, then the output of Read Data1 and Read Data2 are 100 and 200 respectively.

B. When the Write Data line is 1234 and RegWrite= 1 , then the contents of the register $10 is set to 1234.

Answer 1:

100

Answer 2:

200

Answer 3:

1234

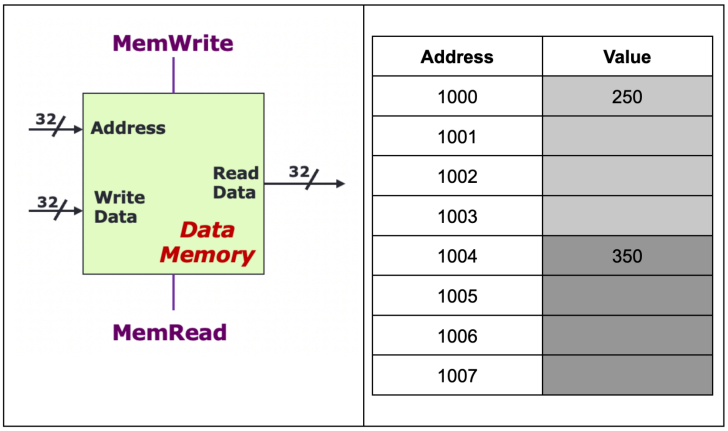
Answer 4:

1

Question 6

1 / 1 pts

What is the output of the following in Data Memory?



Address	Value
1000	250
1001	
1002	
1003	
1004	350
1005	
1006	
1007	

If we want to write the data 54321 into the memory whose address is 1000, then list down the values for the following signals to your Data Memory:

Address = 1000

MemRead = 0

MemWrite = 1

WriteData = 54321

If we want to read the data at the memory whose address is 1004, then write down the values for the following signals in your Data Memory:

Address = 1004

MemRead = 1

MemWrite = 0

WriteData = N.A.

Answer 1:
1000
Answer 2:
0
Answer 3:
1
Answer 4:
54321

Answer 5:
1004
Answer 6:
1
Answer 7:
0

Question 7
1 / 1 pts
Choose the options that are TRUE for PCSrc control signal:

- [x] It chooses between the (PC+4) and (PC+4)+(Immedx4) value, which is then updated into the PC register.
- [x] When 0, the (PC+4) is chosen in the output.
- [x] When 1, the (PC+4)+(Immedx4) is chosen in the output.
- [x] The value of this control signal depends on isZero output from the ALU for branch instructions.
- [ ] The branch target address is calculated by the ALU.

Question 8
1 / 1 pts
The ALUControl signal is used to specify what operation does the ALU need to do whereas the ALUSrc control signal is used to choose the second operand for the ALU.

- (•) True
- ( ) False

Question 9
1 / 1 pts
Your C program is first converted into MIPS assembly code by the compiler. The assembler converts the MIPS assembly code into binary machine code. The binary machine codes are then executed in the MIPS processor.

- (•) True
- ( ) False

Partial

Question 10
0.93 / 1 pts

Trace and list out the datapath for the beq instruction in the following code when register $9 is 0. The beq instruction is stored in the address 0x1080. You may need to use the datapath circuit diagram for this question.

```
Loop:   beq  $9, $0, End
        add  $8, $8, $10
        addi $9, $9, -1
        addi $10,$10, 1
        j    Loop
End:
```

List out the values (in decimal, unless specified) for the following datapath elements:

Instruction Register (in Hexadecimal, E.g., 0x1234ABCD): 0x11200100

Read Register 1 = 9

Read Register 2 = 0

Read Data 1 = 0

Read Data 2 = 0

Register Write= 0

ALUSrc = 0

Operand 1 for ALU = 0

Operand 2 for ALU = 0

isZero = 1

PCSrc = 1

MemRead = 0

MemWrite = 0

PC value after the execution is 0x1094, Say True or False: True

Answer 1:
0x11200100
Answer 2:
9
Answer 3:
0
Answer 4:
0
Answer 5:
0
Answer 6:
0
Answer 7:
0
Answer 8:
0
Answer 9:
0
Answer 10:
1
Answer 11:
1
Answer 12:
0
Answer 13:
0
Answer 14:
True

Question 11
1 / 1 pts
True or False: In a load/store architecture, the only instructions that access memory are load and store.

- (●) True
- ( ) False

Partial

Question 12

0.5 / 1 pts

What are the primary advantages of fixed-sized opcodes? (Choose all that apply)

- [x] Instruction decode is more effcient
- [ ] Leads to overall smaller assembly code
- [x] Faster overall processing time
- [x] Easier to design the hardware

Partial

Question 13

0.5 / 1 pts

What are the different ways in which a memory address is obtained/computed as part of a MIPS instruction? (Choose all that apply)

- [x] Register read
- [x] Sum of PC+4 and an offset
- [ ] Immediate instruction
- [x] Sum of a base and an offset
- [x] Label

Question 14

1 / 1 pts

MIPS is a family of RISC ISAs. What does MIPS stand for?

- ( ) Millions of Instructions per Second
- ( ) Microprocessor Including Pipelined Stages
- (•) Microprocessor without Interlocked Pipelined Stages
- ( ) Microprocessor with Interlocked Pipelined Stages
- ( ) Microprocessor Instruction Pipelined System

Incorrect

Question 15

0 / 1 pts

The hexadecimal value 0x03054021 translates to the following line of MIPS code

addu $8 $24 $5

Quiz score: 12.93 out of 15