GROUP 28

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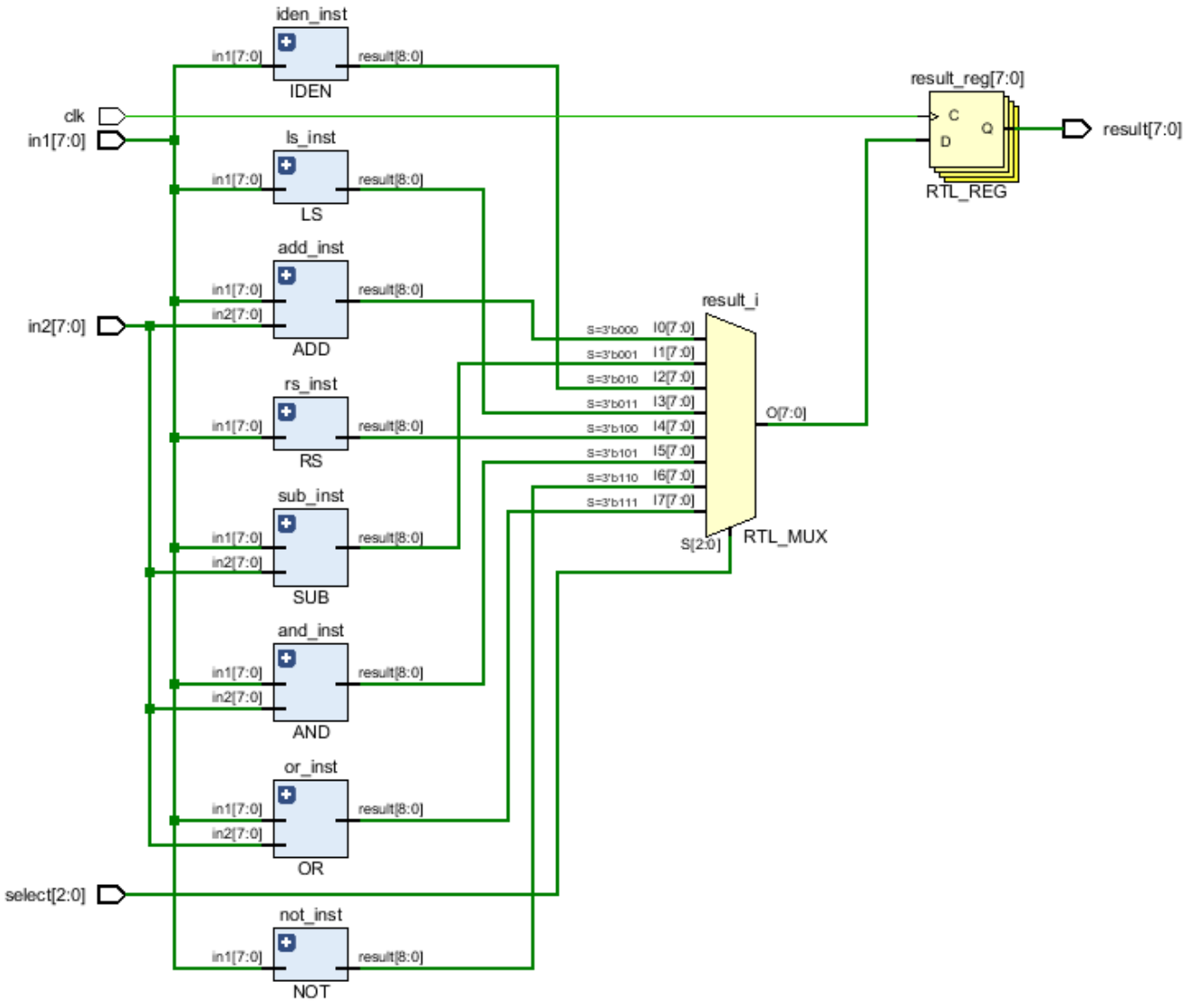
Circuit Diagram:



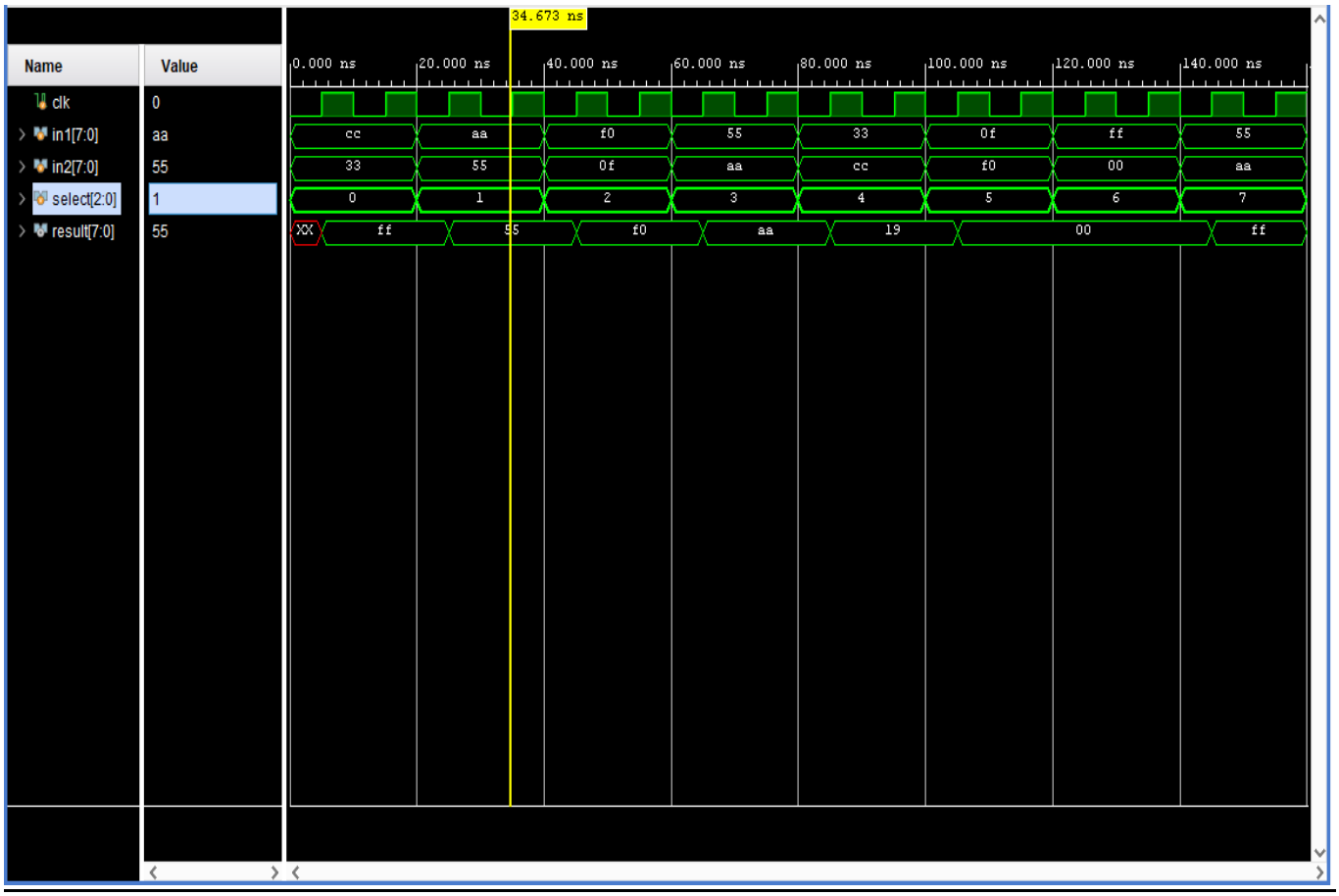
Description:

- We built this ALU circuit using ALU module.
- For each operation we have made different modules:
  ADD – addition
  SUB – subtraction

IDEN – identity
LS – left shift
RS – Right shift
AND – and
NOT – not
OR – or

- We have used the idea of MUX to select one among these 8 operations.
- Each of this operation have a unique 3-bit code which is passed as SELECT to the MUX.
- After evaluating this module give the output as RESULT.
- CLK – clock is used to change the result for each test case.

Simulation:



Terminal Output:

```
# run 1000ns
output for ADD with 204,  51: 255
output for SUB with 170,  85:  85
output for IDEN with 240: 240
output for LS with  85: 170
output for RS with  51:  25
output for AND with  15, 240:   0
output for NOT with 255,   0:   0
output for OR with  85, 170: 255
$finish called at time : 160 ns : File "D:/COA_LAB/project_3/project_3.srcs/sim_1/new/Q1_Grp_28_tb.v" Line 75
INFO: [USF-XSim-96] XSim completed. Design snapshot 'ALU_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:09 . Memory (MB): peak = 2247.727 ; gain = 0.000
```