Group 28

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Control signals used:

- readIn: controls reading of next instruction
  1 - read next instruction
  0 - don’t read
- MuxAlu1: select between regA and PC instruction
  1 - select regA
  0 - select PC
- MuxAlu2: select between regB and immediate value
  1 - select regB
  0 - select imm
- writeDM: write to Data Memory
  1 - write to Data Memory
  0 - don’t write
- readDM: read from Data Memory
  1 - read from Data Memory
  0 - don’t read
- muxWB: select between AluOut and value from LMD
  1 - select AluOut
  0 - select value from LMD
- writeReg: controls write action in register bank
  1 - write to register
  0 - don’t write
- rst: resets all the values
  1 - reset all
  0 - no need to reset
- branch: used to select type of branching (BR / BMI / BPL / BZ)
  000 - No branching

001 - BR
010 - BMI
011 - BPL
100 - BZ

- aluFunc: used to select the arithmetic operation that to be performed.
  0000 - ADD
  0001 - SUB
  0010 - NOT
  0011 - AND
  0100 - OR
  0101 - XOR
  0110 - SLL
  0111 - SRL
  1000 - SRA

Control Signal Table:

	readIn	MuxAlu1	MuxAlu2	writeDM	readDM	muxWB	writeReg	rst	branch	aluFunc
ADD	1	1	1	0	0	1	1	0	000	0000
SUB	1	1	1	0	0	1	1	0	000	0001
NOT	1	1	1	0	0	1	1	0	000	0010
AND	1	1	1	0	0	1	1	0	000	0011
OR	1	1	1	0	0	1	1	0	000	0100
XOR	1	1	1	0	0	1	1	0	000	0101
SLL	1	1	1	0	0	1	1	0	000	0110
SRL	1	1	1	0	0	1	1	0	000	0111
SRA	1	1	1	0	0	1	1	0	000	1000
ADDI	1	1	0	0	0	1	1	0	000	0000
SUBI	1	1	0	0	0	1	1	0	000	0001

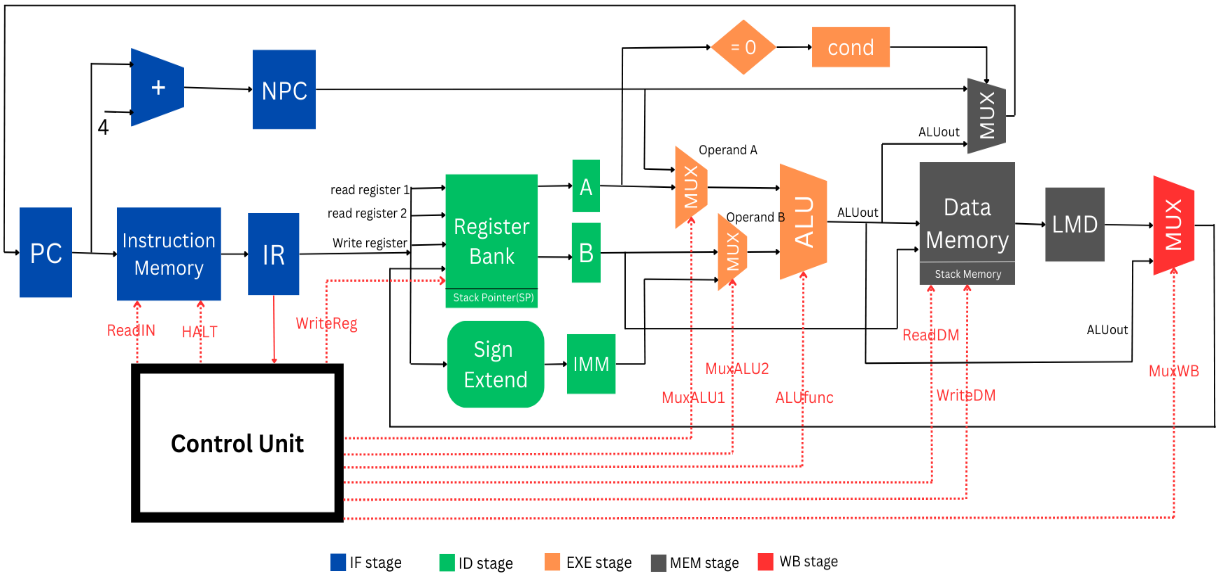
NOTI	1	1	0	0	0	1	1	0	000	0010
ANDI	1	1	0	0	0	1	1	0	000	0011
ORI	1	1	0	0	0	1	1	0	000	0100
XORI	1	1	0	0	0	1	1	0	000	0101
SLLI	1	1	0	0	0	1	1	0	000	0110
SRLI	1	1	0	0	0	1	1	0	000	0111
LD	1	1	0	0	1	0	1	0	000	0000
ST	1	1	0	1	0	0	0	0	000	0000
LDSP	1	1	0	0	1	0	1	0	000	0000
STSP	1	1	0	1	0	0	0	0	000	0000
BR	1	0	0	0	0	0	0	0	001	0000
BMi	1	0	0	0	0	0	0	0	010	0000
BPL	1	0	0	0	0	0	0	0	011	0000
BZ	1	0	0	0	0	0	0	0	100	0000
PUSH	1	1	0	1	0	0	1	0	000	0001
POP	1	1	0	0	1	0	1	0	000	0000
CALL	1	1	0	1	0	0	1	0	000	0001
RET	1	1	0	0	1	0	1	0	000	0000
MOVE	1	1	0	0	0	1	1	0	000	0000
NOP	1	0	0	0	0	0	0	0	000	0000
HALT	0	0	0	0	0	0	0	1	000	0000

RTL instruction Table:

Instruction	RTL micro operations	Control Signals
ADD	- Source and Destination registers obtained from 32 bit Instruction.	- - MuxAlu1,MuxAlu2

	- Select the reg1 and reg2 as operands - Perform addition using aluFunc signal. - Select AluOut to write back. - Write back in register bank	- aluFunc - muxWB - writeReg
ADDI	- Source and Destination registers and immediate value obtained from 32 bit Instruction. - Select the reg1 and imm as operands - Perform addition using aluFunc signal. - Select AluOut to write back. - Write back in register bank	- - MuxAlu1,MuxAlu2 - aluFunc - muxWB - writeReg
LD	- Obtain source and Destination register from 32-bit instruction. - Read from data memory - Load from LMD for write back - Perform write back in register bank.	- - readDM - muxWB - writeReg
ST	- Obtain source and destination register from 32-bit instruction. - write to data memory	- writeDM
BMI	- Source register and offset are obtained from instruction. - Branch if less than zero is selected using branch - Update PC according to the condition.	- branch
MOVE	- Dest and src registers are obtained from instruction. - Perform add operation with one operand as src register and zero register. - Select aluOut for write back. - Perform write back.	- MuxAlu1,MuxAlu2 - aluFunc - muxWB - writeReg
CALL	- Immediate value from instruction. - Perform add operation to the PC and 4. - Store it in stack mem - Perform addition of PC and offset - Update this as next PC.	- writeDm
RET	- Perform read from stack mem. - Update this to PC.	- readDM

Data Path:


cond
= 0
+
NPC
4
MUX
ALUout
Operand A
read register 1
read register 2
Write register
Register Bank
Stack Pointer(SP)
A
B
MUX
Operand B
MUX
ALU
ALUout
Data Memory
Stack Memory
LMD
MUX
PC
Instruction Memory
IR
ReadIN
HALT
WriteReg
Sign Extend
IMM
ReadDM
ALUout
MuxALU2
MuxALU1
ALUfunc
WriteDM
MuxWB
Control Unit
🟦 IF stage
🟩 ID stage
🟧 EXE stage
⬛ MEM stage
🟥 WB stage