Experiment 6: **Sequential Circuit - 2**

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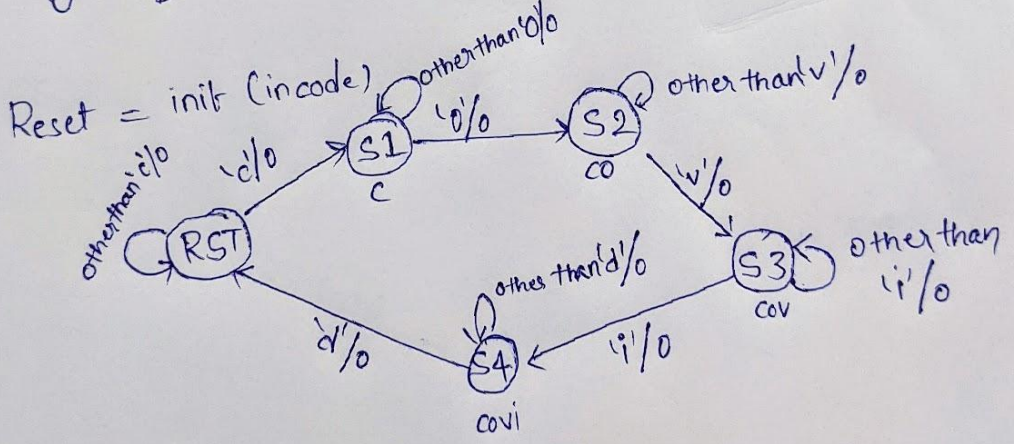
Overview of the experiment:

In two to three paragraphs, summarize
•The purpose of this experiment is to make us familiar with string recognizer and about mealy machine
• I first made a state transition table of how it recognizes the string and then implemented it using a behavioural model.
• I have written in the following order: approach,code,rtl view,simulation screen shots and finally observations.

Approach to the experiment:

State transition table

Reset	Input	Present state	Next state	output
1	X	XXX	RESET	0
0	'C'	RESET	S1	0
0	'O'	S1	S2	0
0	'V'	S2	S3	0
0	'I'	S3	S4	0
0	'D'	S4	RESET	1



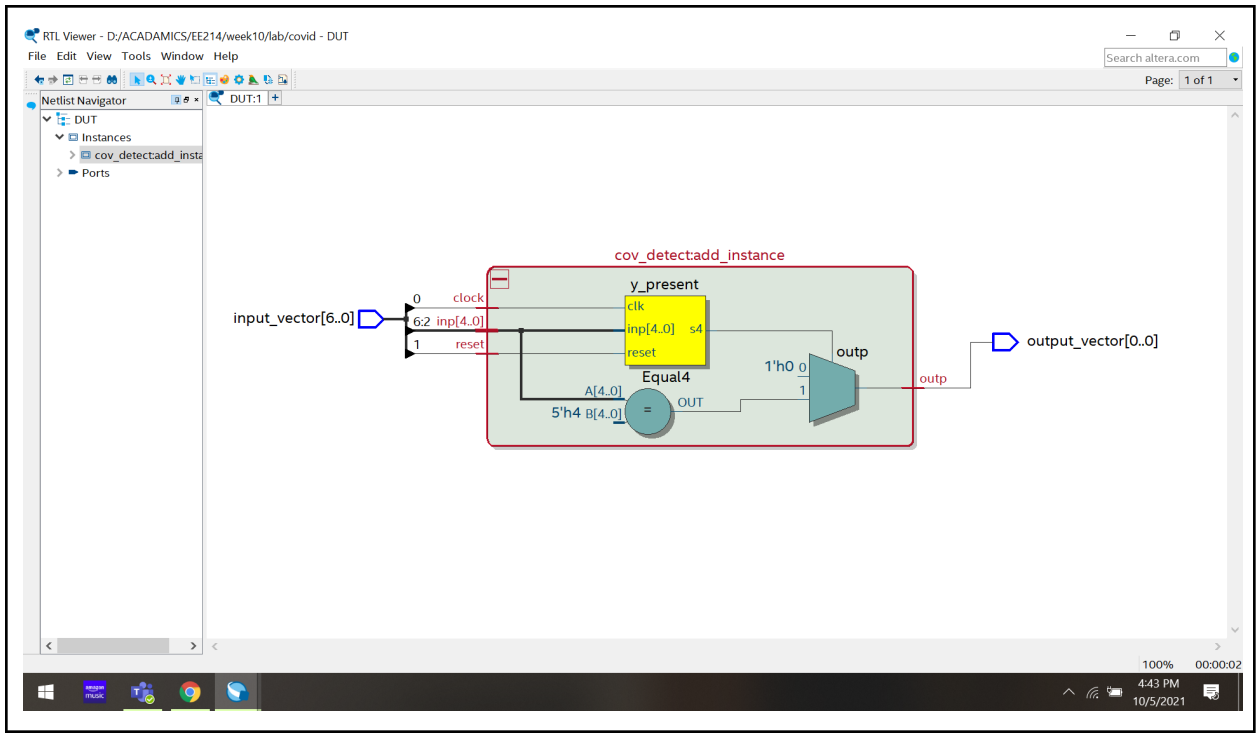
State diagram for detecting word 'covid' in the given string of alphabets

Design document and VHDL code if relevant:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity cov_detect is
port(inp:in std_logic_vector(4 downto 0);
        reset,clock:in std_logic;
        outp: out std_logic);
end cov_detect;

architecture rch of cov_detect is

---------------Define state type here-----------------------------
type state is (init,s1,s2,s3,s4); -- Fill the code
---------------Define signals of state type-----------------------
signal y_present,y_next: state:=init;

begin
clock_proc:process(clock,reset)
begin
    if(clock='1' and clock' event) then
        if(reset='1') then
            y_present<=init;
        else
                            y_present<=y_next;

        end if;
    end if;

end process;

state_transition_proc:process(inp,y_present)
begin
    case y_present is
        when init=>
            if(unsigned(inp)=3) then    --c
                y_next<=s1;
                                                    outp<='0';
                                                    else
                                                    outp<='0';
                                                                y_next<=init;


                                                        end if;
                        when s1=>
            if(unsigned(inp)=15) then    --o
                y_next<=s2;
                                                    outp<='0';
                                                    else
```

```
                                        outp<='0';
                                                y_next<=s1;


                                        end if;
                when s2=>
        if(unsigned(inp)=22) then    --v
           y_next<=s3;
                                        outp<='0';
                                        else
                                        outp<='0';
                                                y_next<=s2;


                                        end if;
                when s3=>
        if(unsigned(inp)=9) then    --i
           y_next<=s4;
                                        outp<='0';
                                        else
                                        outp<='0';
                                                y_next<=s3;

                                        end if;
                when s4=>
        if(unsigned(inp)=4) then    --d
           y_next<=init;
                                        outp<='1';
                                        else
                                        outp<='0';
                                                y_next<=s4;

                                        end if;
                end case;



end process;
end rch;
```

RTL View:



DUT Input/Output Format:

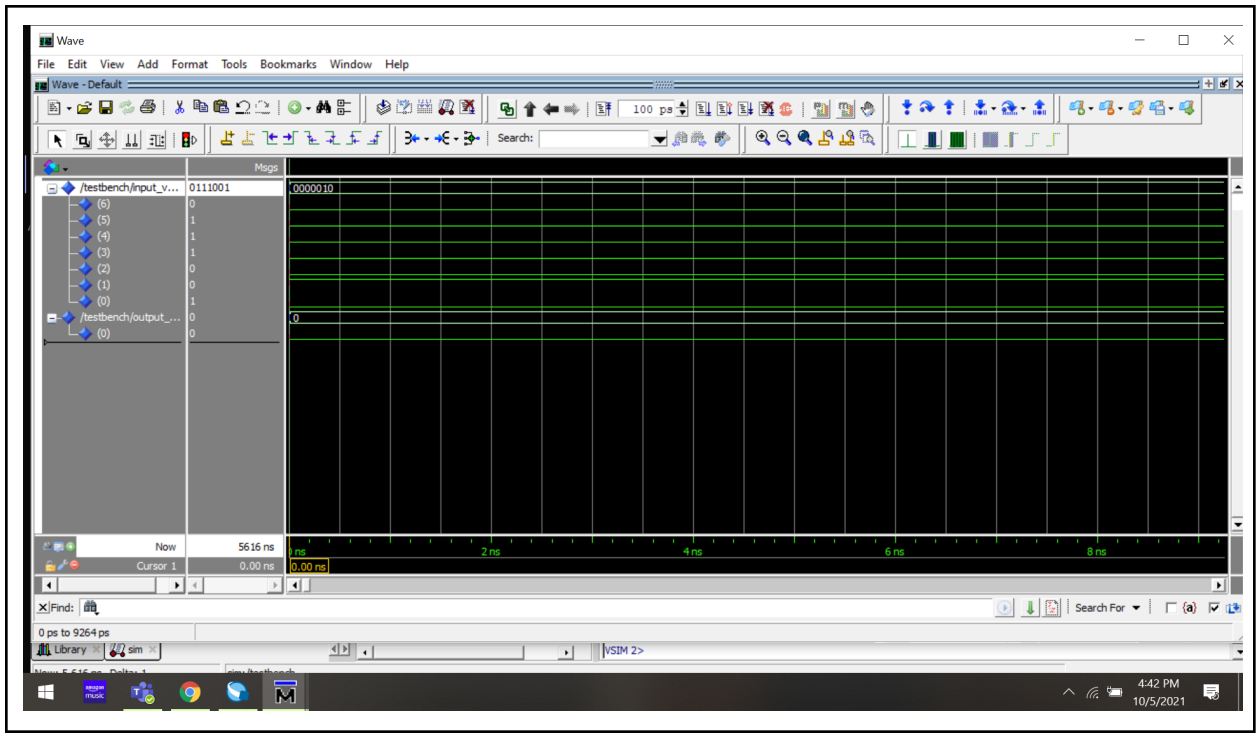
input/output :

```
inp(4)   => input_vector(6),
inp(3)   => input_vector(5),
inp(2)   => input_vector(4),
inp(1)   => input_vector(3),
inp(0)   => input_vector(2),
reset    => input_vector(1),
clock    => input_vector(0),
outp     => output_vector(0)
```

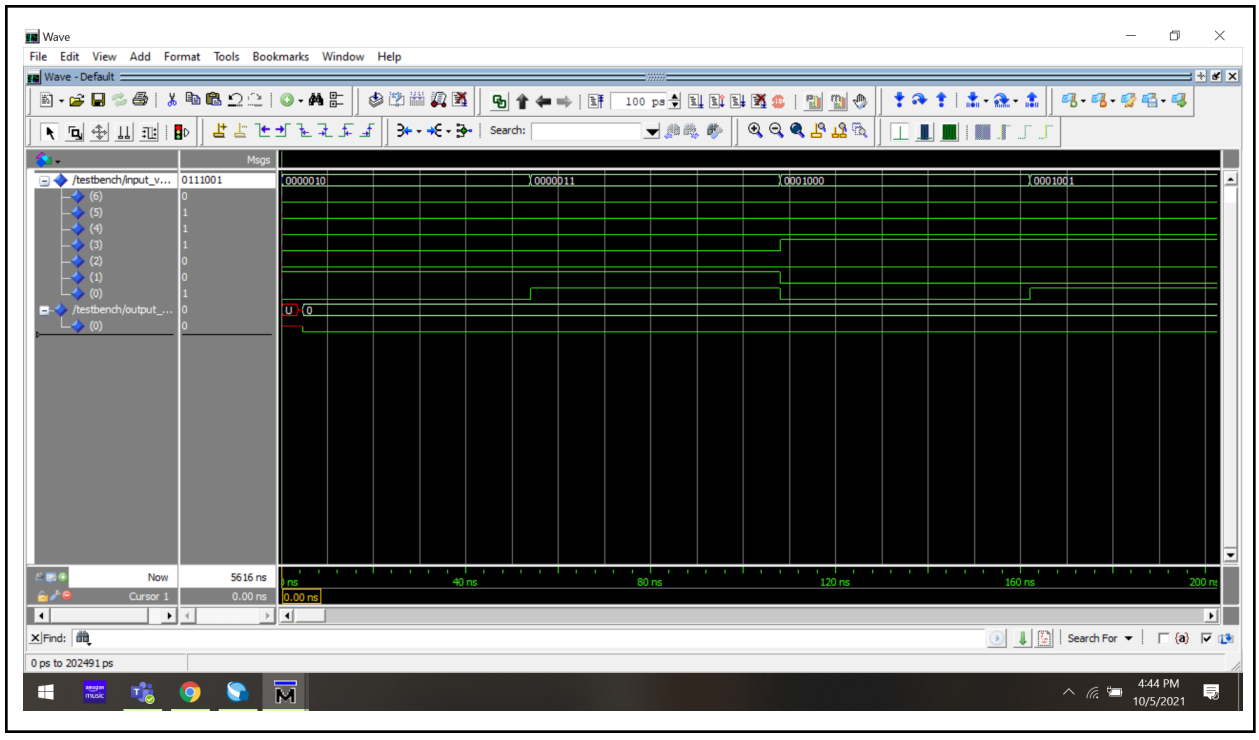
Sample trace file:

```
0000010 0 0
0000011 0 0
0001000 0 1
0001001 0 1
0001000 0 1
0001001 0 1
0001000 0 1
```

RTL Simulation:



Gate-level Simulation:



Observations:

All the test cases have passed the scan chain result :