Lab 5

Using an FPro SoC with Custom Hardware Accelerators: Fast Sorting

Design, implement and verify an FPro system and a corresponding application in C/C++ capable of performing sorting in software and hardware.

Your solution should support sorting of N w-bit unsigned integers for at least the following values of k, $N=2^k$, and w:

k	N	w
4	16	8
6	64	8
9	512	16
10	1024	16
11	2048	16
12	4096	16
13	8192	16

Switches SW3...SW0 should be used to enter $k=\log_2(N)$, i.e., $\log_2$ of the number of elements to sort.
Here are the suggested values of k, and the corresponding values of N and w, to be used for different phases of your project:

1. Debugging: k=4 (N=16 elements of the width w=8 bits)
2. Demo: k=4 and k=6 (N=16 and N=64 elements of the width w=8 bits)
3. Timing measurements: k=9..13 (from N=512 to N=8192 elements of the width w=16 bits).

The application should support the following functionality:

After power-up, the system should wait for the first press of BTNR. All remaining buttons should be ignored.

Task 1: Pseudorandom Initialization

Each time BTNR is pressed, two arrays, sw_data[ ] and hw_data[ ], stored in the Processor's RAM, should be initialized with the same N pseudorandom values generated in software using a Pseudorandom Number Generator based on the C functions rand() and srand().

Task 2: Display Mode

In the Display Mode, for N=16 and N=64, a user should be able to browse the contents of the arrays sw_data[ ] and hw_data[ ] using the following user interface:

SW15=0 : browsing sw_data[ ]
SW15=1 : browsing hw_data[ ].

The circuit should display

- Current Address (using Seven-Segment Displays 3 and 2)
- Value in sw_data[ ] (when SW15=0) or hw_data[ ] (when SW15=1) at the position given by the Current Address (using Seven-Segment Displays 1 and 0).

BTNU should increment the Current Address in a wrap-around fashion (e.g., for N=16, "0F" should be followed by "00").
BTND should decrement the Current Address in a wrap-around fashion (e.g., for N=16, "00" should be followed by "0F").

For values of N > 256, browsing should be disabled, and the Seven-Segment Displays should show values of k and w, respectively, expressed in the decimal notation.

Task 3: Sorting

Pressing BTNC should initiate sorting. Sorting should be performed in software and hardware. Sorting in software should be performed on the array sw_data[ ] stored in the Processor memory. Sorting in hardware should involve transferring input data from the array hw_data[ ] to the Sorting core, performing sorting, and transferring results back to the array hw_data[ ]. The processed numbers should be treated as unsigned integers and should be sorted in ascending order.

The total number of clock cycles required for software and hardware sorting should be measured and stored.

During sorting, “----“ should be displayed on the seven-segment displays.

After sorting is completed, the seven-segment displays should show the number of mismatches between the results of sorting in software and the results of sorting in hardware. Thus, 0000 will represent a perfect match. For N=16 (0x0010), 0010 will mean that none of the corresponding locations in each array matches.

After another press of BTNC, the system should come back to the Display Mode.

Task 4: Cycle Count Mode

After sorting is completed, pressing BTNL should allow toggling between the Display Mode and the Cycle Count Mode.
In the Cycle Count Mode, the total number of clock cycles used for sorting should be displayed on the seven-segment displays.

The position of the switch SW14 should indicate whether the least significant 16 bits of the Cycle Counter (for SW14=0), or the most significant 16 bits of the Cycle Counter (for SW14=1) are displayed in the hexadecimal notation.

The position of the switch SW15 should indicate whether the number of clock cycles used for sorting in software (for SW15=0), or the number of clock cycles used for sorting in hardware (for SW15=1) is displayed.

Task 5: Debug Mode

During sorting and timing measurements, no information should be transmitted using UART (and thus displayed on the console).

During the remaining phases of the operation of your application, you can use functions of the uart driver, such as disp(), to help you with debugging the operation of your application and sorting core.
However, please note that the primary mode of debugging the sorting core is through the use of a VHDL testbench and functional simulation using the Vivado Simulator or ModelSim.

Deliverables:

1. New or revised VHDL Code [other than the original code of the Sampler FPro system]
2. New or revised C/C++ Code [drivers, test programs, applications]
3. Video demonstrating the operation of your application.
4. Written report

Note: Make sure to create a separate directory for each deliverable mentioned above. Do not submit any other files of the Vivado project!

Report File:

1. List of fully completed tasks
2. List of partially completed tasks, including the description of any incorrect functionality
3. Tables and graphs showing for each value of N between 2^9 and 2^{13} (powers of 2 only)
    a. Execution time in software and execution time in hardware (in clock cycles, using logarithmic scale for graphs)
    b. Ratio of the execution time in software vs. execution time hardware
    c. Resource utilization (#Slices, #LUTs, #FFs, #BRAMs)
4. Conclusions

Bonus Task: Contest for the Fastest Implementation of Sorting:

Bonus points will be awarded to students who perform sorting (correctly) using the smallest number of clock cycles in hardware and/or software.
Possible optimizations:

- Faster sorting algorithms in software
- Efficient C/C++ implementation
- Faster sorting algorithms in hardware
- Efficient VHDL implementation.

Deadlines:

	Tuesday Section	Wednesday Section	Friday Section
Deliverables Due for Schedule A	**Saturday, April 17, 11:59pm**		
Deliverables Due for Schedule B	**Saturday, May 1, 11:59pm**		