**Lab 5 Report**

**1)List of fully completed tasks**

All the tasks are completed.

**2) List of partially completed tasks, including the description of any incorrect functionality**

There is no uncompleted or partially completed task

**3) Tables and graphs showing for each value of N between 2^9 and 2 ^13 (powers of 2 only)**

a)

|  |  |  |
| --- | --- | --- |
|  | Clk cycle duration for SW | Clk cycle duration for HW |
| 512-bit |  |  |
| 1024-bit |  |  |
| 2048-bit |  |  |
| 4096-bit |  |  |
| 8192-bit |  |  |

b)

**c)** LUT : 1956

FF : 1919

BRAM : 36

DSP : 1

**4) Conclusion**

During the lab various sorting algorithms are analyzed. But to reduce the design time simplest sw and hw implementations (buble sort) algorithm is chosen. It completely works. SW times are greater than the HW times although the HW times include the data transfers to the HW sort\_core.