**LAB 4 Report**

**A. List of fully completed tasks**

**-** Determining the memory map of the LFSR wrapper (address 0 is used to read, address 1 is used to initialize the LFSR with a hardcoded initial value)

- Drawing the block diagram for LFSR and its wrapper.

**-** Writing the VHDL code for LFSR and its wrapper.

- Writing a test bench to verify the LFSR. The output data obtained from the simulation is compared with the data obtained from python code using a library (pylfsr) with the same polynomial.

- Modifying the mmio\_sys\_sampler\_basys3.vhd inorder to add the lfsr wrapper using the reserved slot4.

- Syhntesizing, implementing and generating bitstream

- Exporting the design to Vitis platform

- Using Vitis building the source files and generating the elf file.

- Using Vivado with the associated elf file modifying the bitstream.

- Programming the board with bitstream.

- Demonstrating the video on the FPGA board.

- Writing the C++ and header files for the LFSR core.

- Writing the main function that uses buttons, switches, LFSR, seven segment displays and timer.

**B. List of tasks attempted but not completed**

There is no uncompleted task.

**C. List of any deviations from the original specification**

There is no deviation from the original specification.

**D. Resource utilization after placing and routing**

SLICE : 735

LUT : 1911

FF : 1884

BRAM : 32

**E. Resource utilization after placing and routing and lessons learned.**

Mostly, I encountered the difficulties on the animation part related with the seven segment display.

In this lab, I’ve learned the LFSR structures which is commonly used for pseudo-random number generation. Also, I’ve learned how to write a driver for a custom hardware and use this driver in the main function.