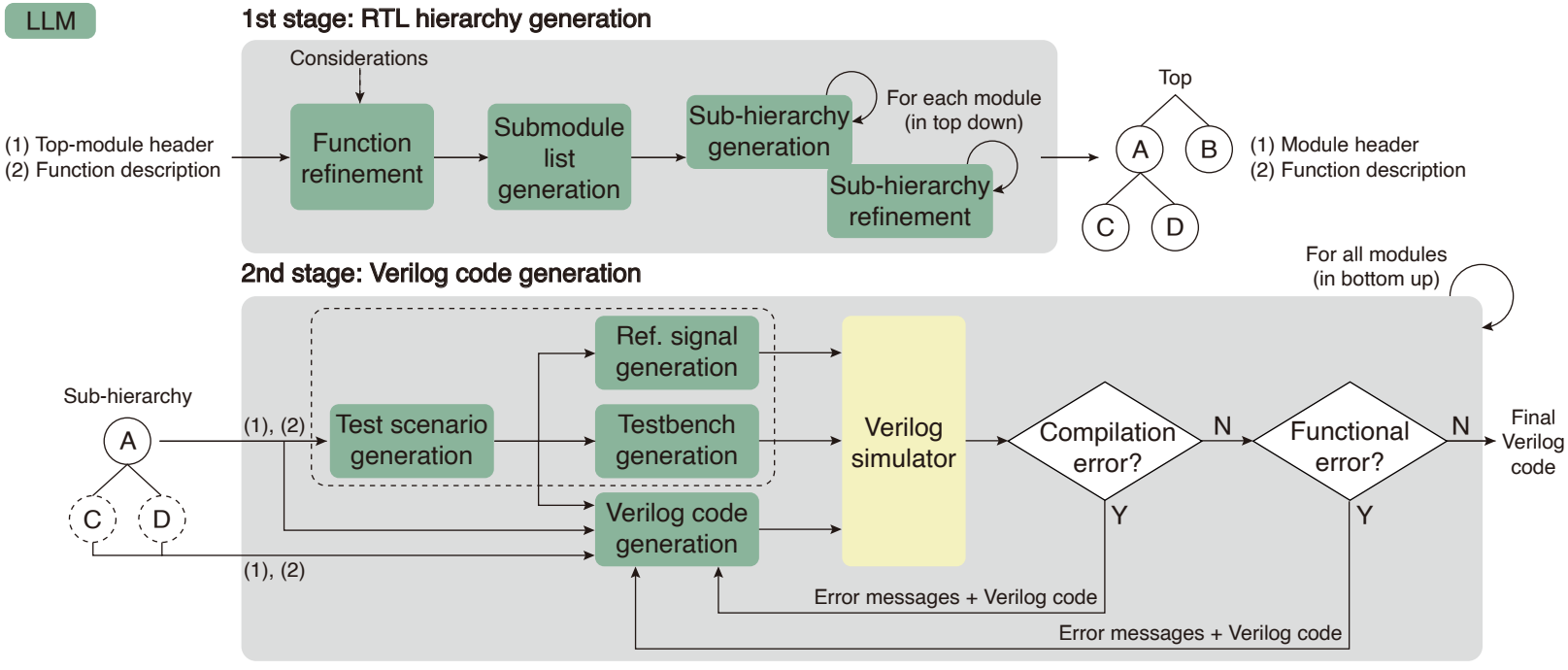
LLM
1st stage: RTL hierarchy generation
Considerations
(1) Top-module header
(2) Function description
Function refinement
Submodule list generation
Sub-hierarchy generation
For each module (in top down)
Sub-hierarchy refinement
Top
A
B
C
D
(1) Module header
(2) Function description
2nd stage: Verilog code generation
For all modules (in bottom up)
Sub-hierarchy
A
C
D
(1), (2)
Test scenario generation
Ref. signal generation
Testbench generation
Verilog code generation
(1), (2)
Verilog simulator
Compilation error?
N
Y
Functional error?
N
Y
Final Verilog code
Error messages + Verilog code
Error messages + Verilog code