ECE341 Homework No. 8

Due date: 12/3/2014

Problem No. 1 (10 points)

Describe a structure similar to that in Figure 8.10 (slide-13 of Lecture-16) for a 64M x 128 memory using 16M x 8 memory chips. What is the total number of memory chips needed? How are they organized in rows and columns?

Problem No. 2 (10 points)

(a) **(2 points)** What is the difference between "temporal" and "spatial" locality?

(b) **(4 points)** Consider a program P_1 which contains two different loops, Loop-A and Loop-B. When a user runs P_1 on a processor, Loop-A iterates 10 times and each Loop-A iteration has 5 instructions. In comparison, Loop-B iterates only twice but each Loop-B iteration has 25 instructions. Thus, both Loop-A and Loop-B execute the same total number of instructions (50). Which of the two loops do you expect to have more instruction cache hits? Why?

(c) **(4 points)** The cache block size in many computers is in the range of 32 to 128 bytes. What would be the main advantages and disadvantages of making the size of cache blocks larger or smaller?

Problem No. 3 (5 points)

A computer system uses 46-bit memory addresses. It has a 64K-byte cache organized in a direct-mapped manner, with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Calculate the number of bits in each of the *Tag*, *Block*, and *Word* fields of the memory address.

Problem No. 4 (7 points)

Assume that the computer system of Problem No. 3 uses a 2M-byte 16-way set-associative cache (i.e., 16 blocks per set). The size of each cache block is 64 bytes.

(a) **(2 points)** Calculate the number of sets in the cache.

(b) **(5 points)** Calculate the number of bits in each of the *Tag*, *Set* and *Word* fields of the memory address.

Problem No. 5 (16 points)

A computer has a small direct-mapped cache capable of holding eight cache blocks. Each cache block consists of 16 words. The computer uses 10-bit memory addresses. When a program *P* is executed, the processor reads data sequentially from the following word addresses:

20, 32, 512, 160, 32, 896, 904, 512

All the above addresses are shown in their decimal values. Assume that the cache is initially empty.

(a) **(12 points)** For each of the above addresses, indicate whether the cache access will result in a hit or a miss. Also, compute the hit ratio of the cache.

(b) **(4 points)** Show the tag contents for each of the eight cache blocks at the completion of the program. For blocks that do not contain any valid data, write down "Invalid" in the tag field.

Problem No. 6 (12 points)

Repeat part (a) of Problem No. 5 for a 2-way set-associative cache that uses the LRU replacement algorithm. Assume the same cache capacity (eight cache blocks) and block size (16 words per block), as in Problem No. 5.