ECE 341

Lecture # 2

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Portland State University

Announcements

- Course website reminder:
  http://www.ece.pdx.edu/~zeshan/ece341.htm

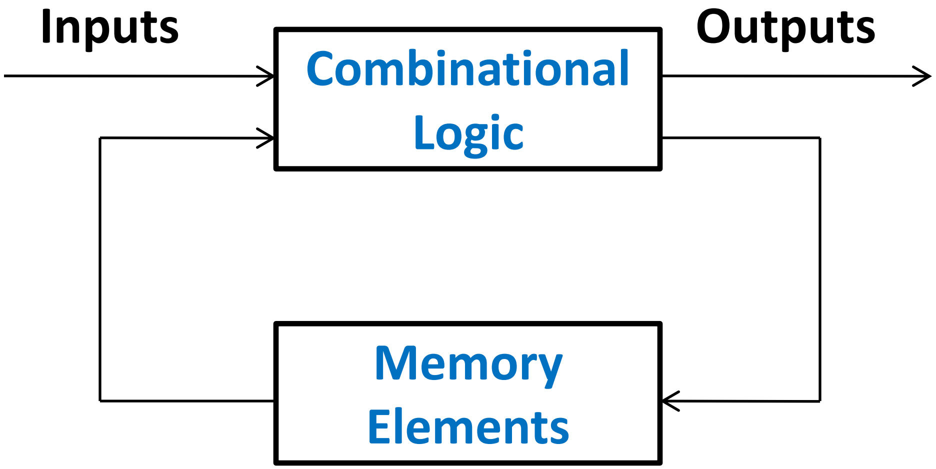
- Homework 1:
  - Will be posted on course website tonight
  - Due date: Wednesday 10/8 in class

Lecture Topics

- Sequential Logic
  - Latches
    - SR Latch
    - Gated SR Latch
    - Gated D Latch
  - Flip flops
    - D flip-flop
    - T flip-flop
    - JK flip-flop

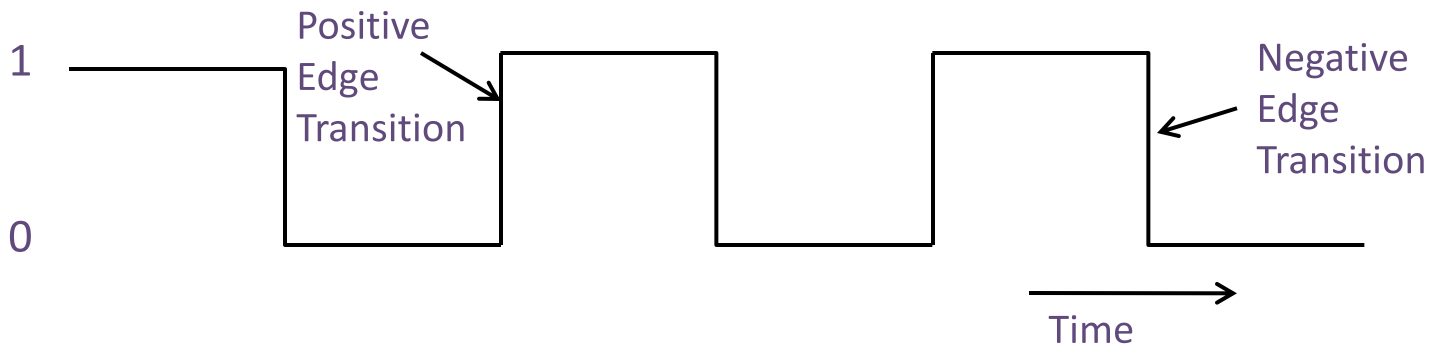
- Reference: Appendix A (pages 492-502), including section A.6

Sequential Logic



- Combinational logic:
  - outputs are uniquely defined for each input combination
- Sequential Logic:
  - output depends not only on current inputs but also on previous state

Clock Signal

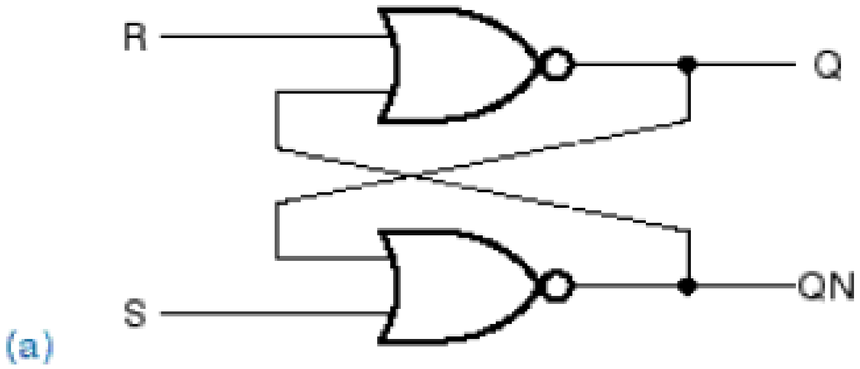


- Sequential circuits often use a clock signal as a reference for when output state changes take place
- **Level triggering:** State changes can take place at any time as long as clock signal is at a particular level (e.g., during the "1" clock phase)
- **Edge triggering:** State changes take place only on clock transitions
  - 0 => 1 transition (positive edge-triggered)
  - 1 => 0 transition (negative edge-triggered)

Latches and Flip Flops

- Latches and flip flops are the most basic memory elements used in sequential circuits
- **Flip flop**
  - Samples its inputs and changes its output only at the *edge* of a controlling clock signal (edge-triggered)
- **Latch**
  - Watches its inputs continuously and changes its output *at any time* irrespective of clock edge transitions
  - May or may not be level-triggered

SR Latch

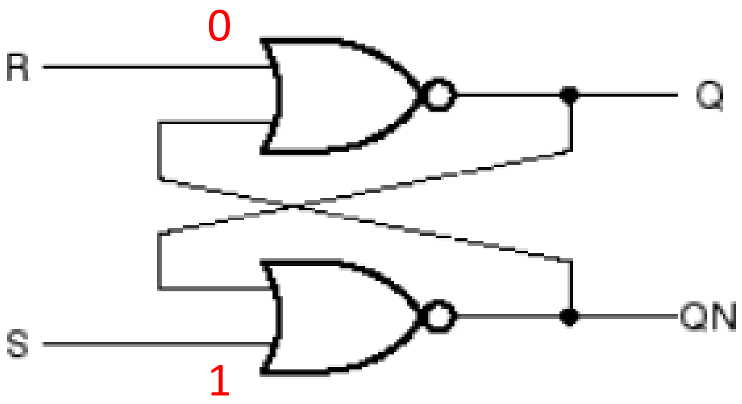


S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

(b)

An SR latch has a set input (S), a reset input (R) and two outputs (Q and QN) that are normally complements of each other

SR Latch



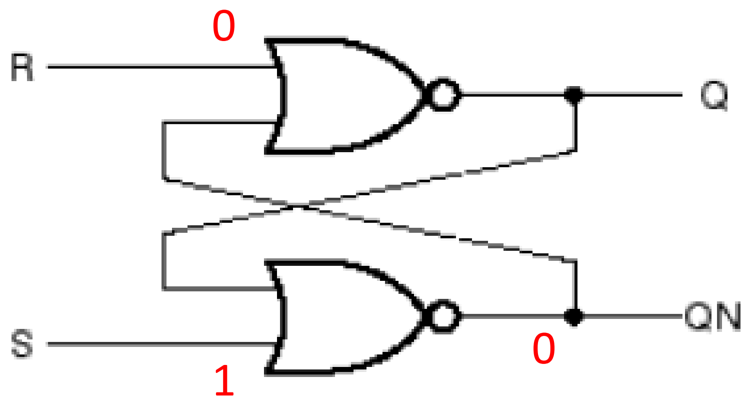
(a)

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

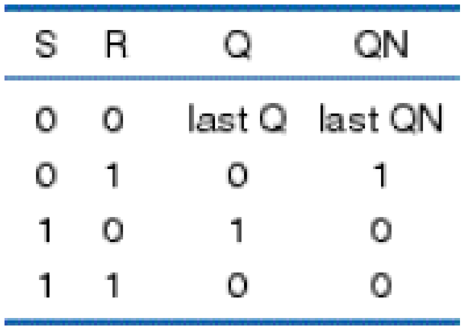
(b)

SR Latch

(a)



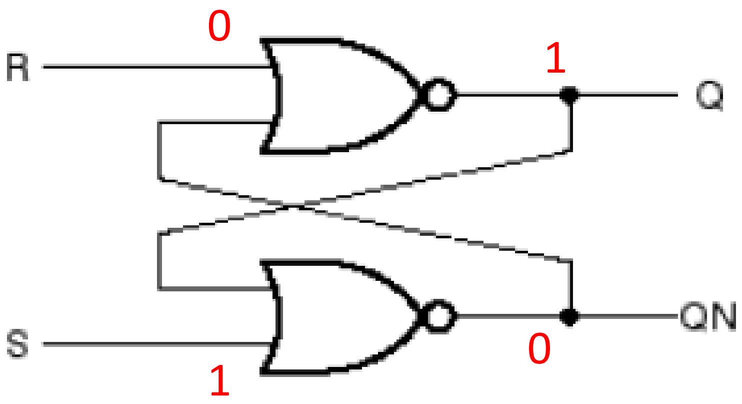
(b)



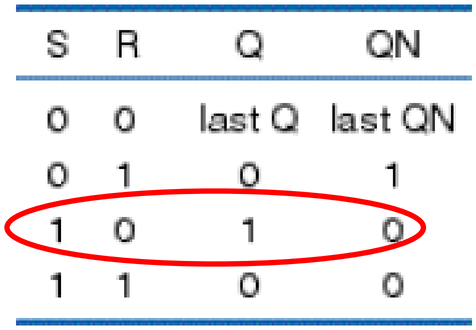
S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

x NOR 1 = 0 for x = 0, 1

SR Latch



(a)

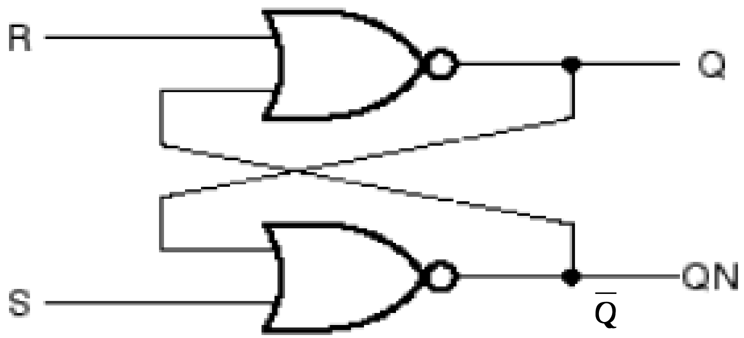


S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

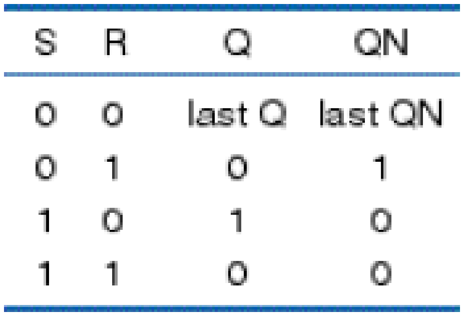
(b)

0 NOR 0 = 1

SR Latch



(a)



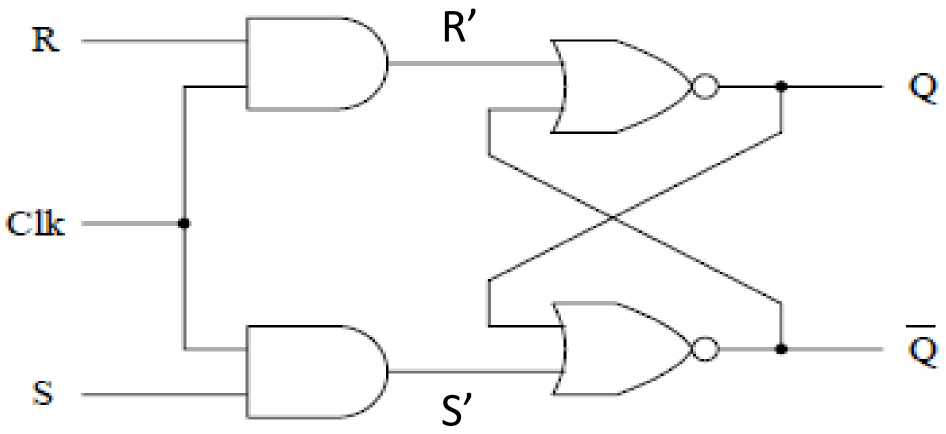
S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

(b)

- Asserting S *sets* the latch (Q = 1, QN = 0)
- Asserting R *resets* the latch (Q = 0, QN = 1)
- If both S and R are 0, the latch acts as a memory element (retains its previous state)
- Input combination R = S = 1 is normally not used
  - QN is often represented as $\overline{Q}$ (NOT of Q)

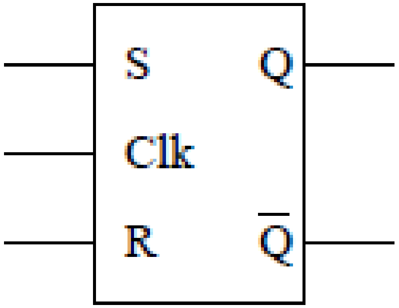
Gated SR Latch

Circuit



Clk	S	R	Q(t+1)
0	x	x	Q(t)
1	0	0	Q(t)
1	0	1	0
1	1	0	1
1	1	1	x

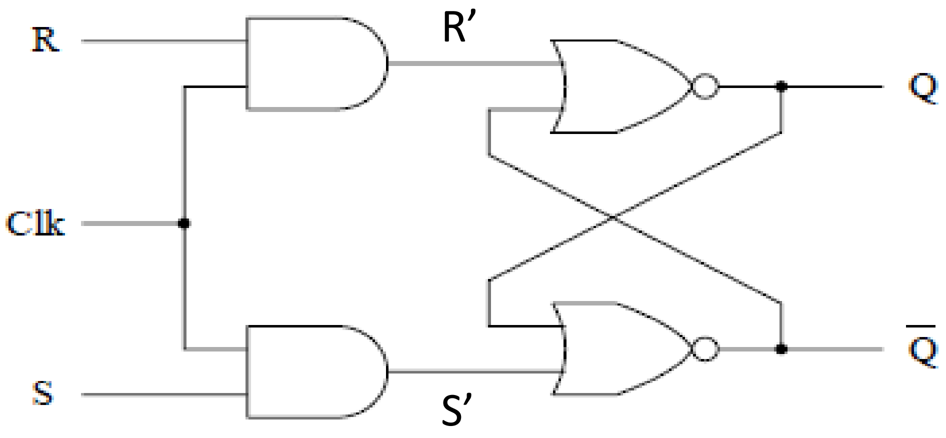
Truth Table



Graphical Symbol

Gated SR Latch

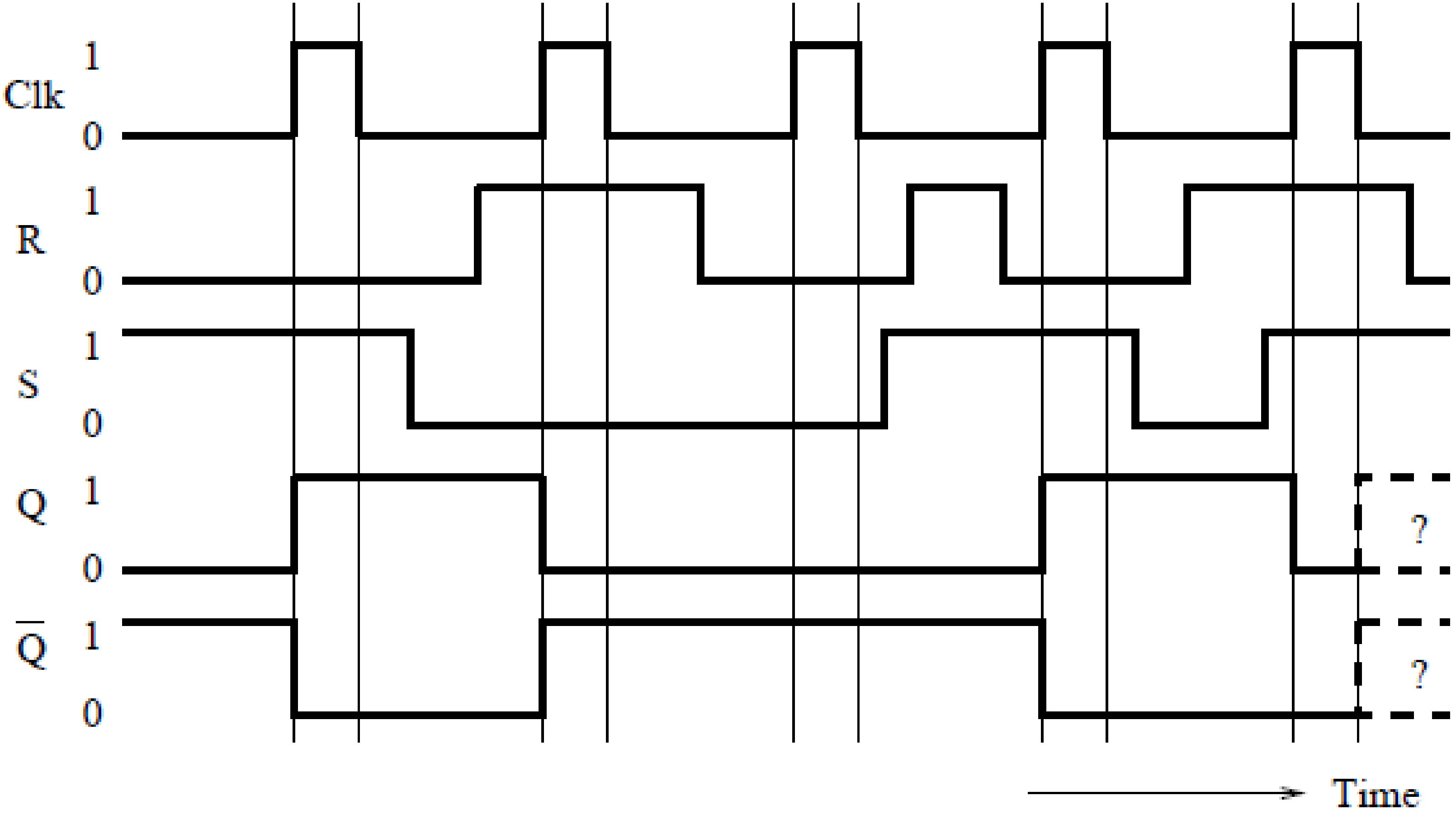
Circuit



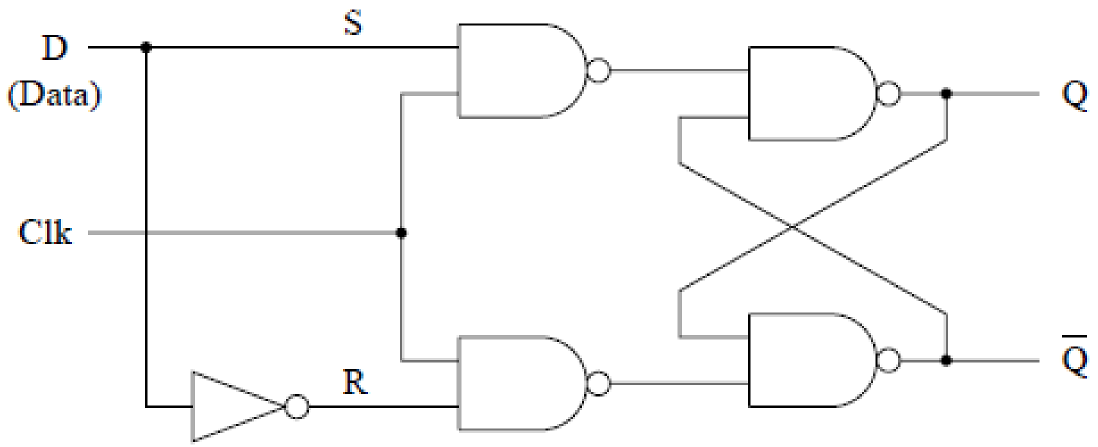
Clock input controls the time at which the latch is set or reset

- When clk = 1
  - R’ = R and S’ = S, behaves like a regular SR latch set/reset by S/R inputs)
- When clk = 0
  - R’ = S’ = 0, latch cannot be set or reset by R and S inputs

Timing Diagram for Gated SR Latch



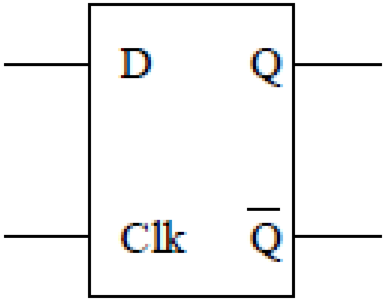
Gated D Latch



Circuit

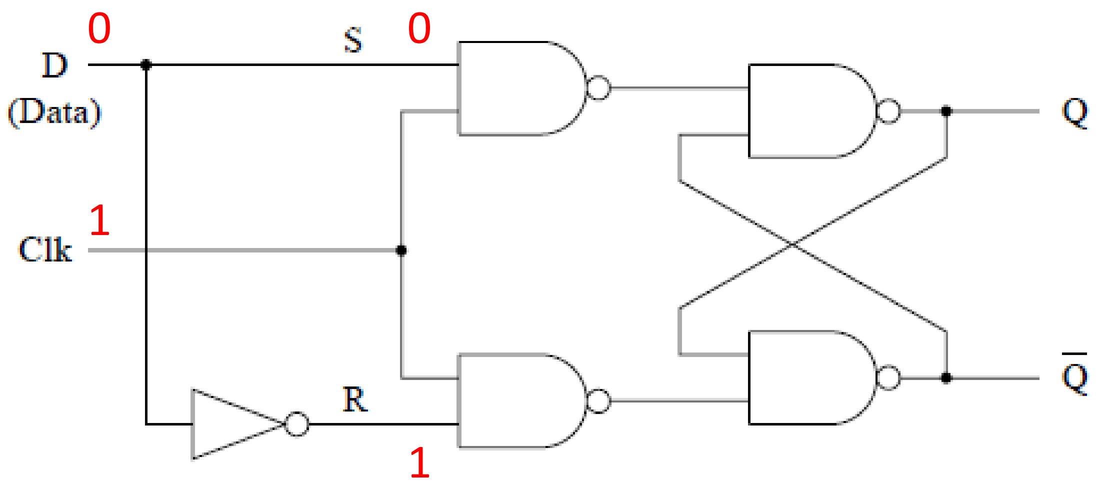
Clk	D	Q(t+1)
0	x	Q(t)
1	0	0
1	1	1

Truth Table



Graphical Symbol

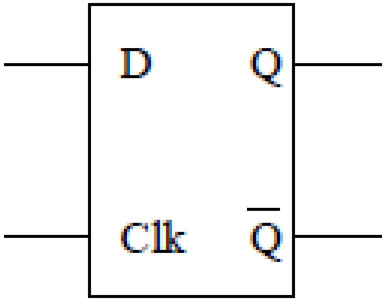
Gated D Latch



Circuit

Clk	D	Q(t+1)
0	x	Q(t)
1	0	0
1	1	1

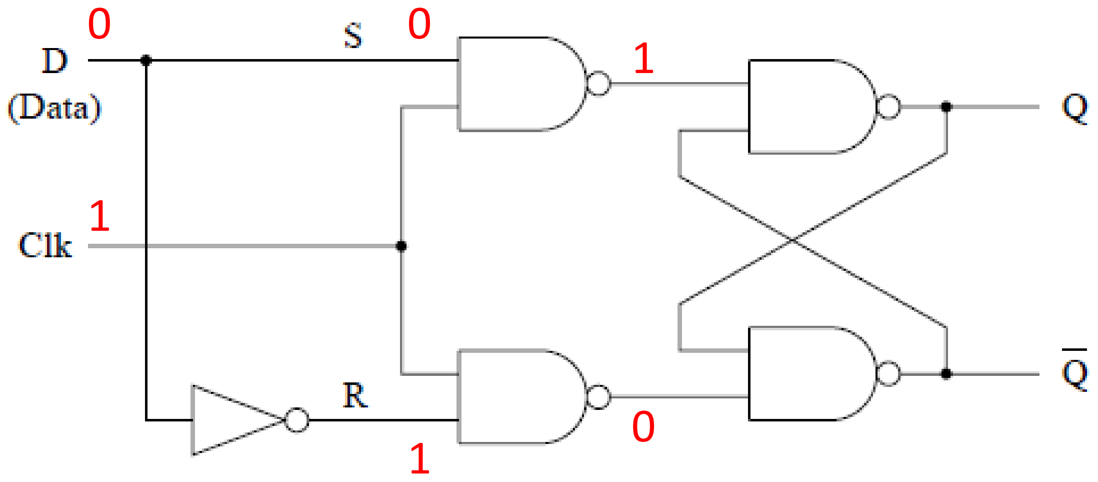
Truth Table



Graphical Symbol

Gated D Latch

Circuit

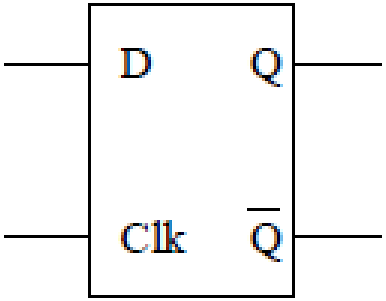


0 NAND 1 = 1

1 NAND 1 = 0

Clk	D	Q(t+1)
0	x	Q(t)
1	0	0
1	1	1

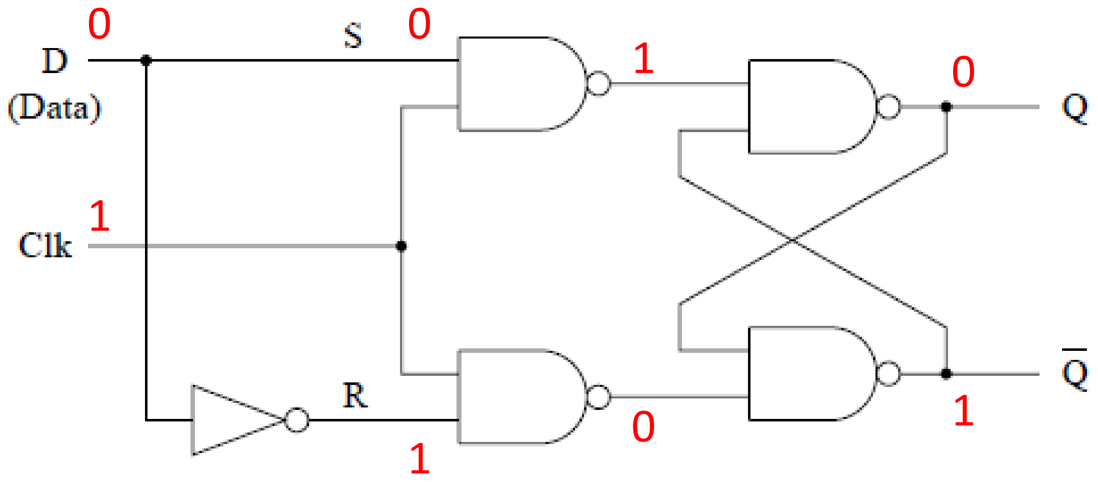
Truth Table



Graphical Symbol

Gated D Latch

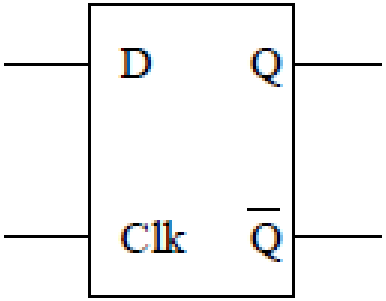
Circuit



Q NAND 0 = 1
1 NAND 1 = 0

Clk	D	Q(t+1)
0	x	Q(t)
1	0	0
1	1	1

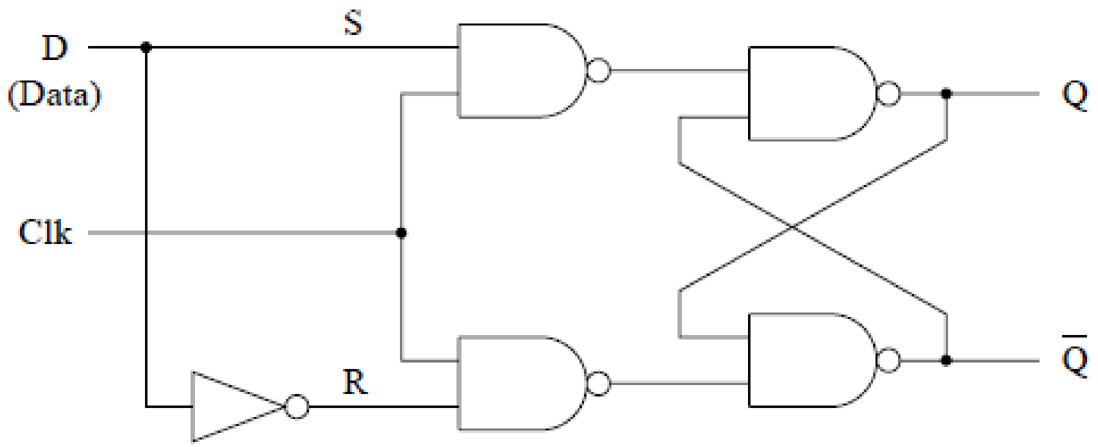
Truth Table



Graphical Symbol

Gated D Latch

Circuit



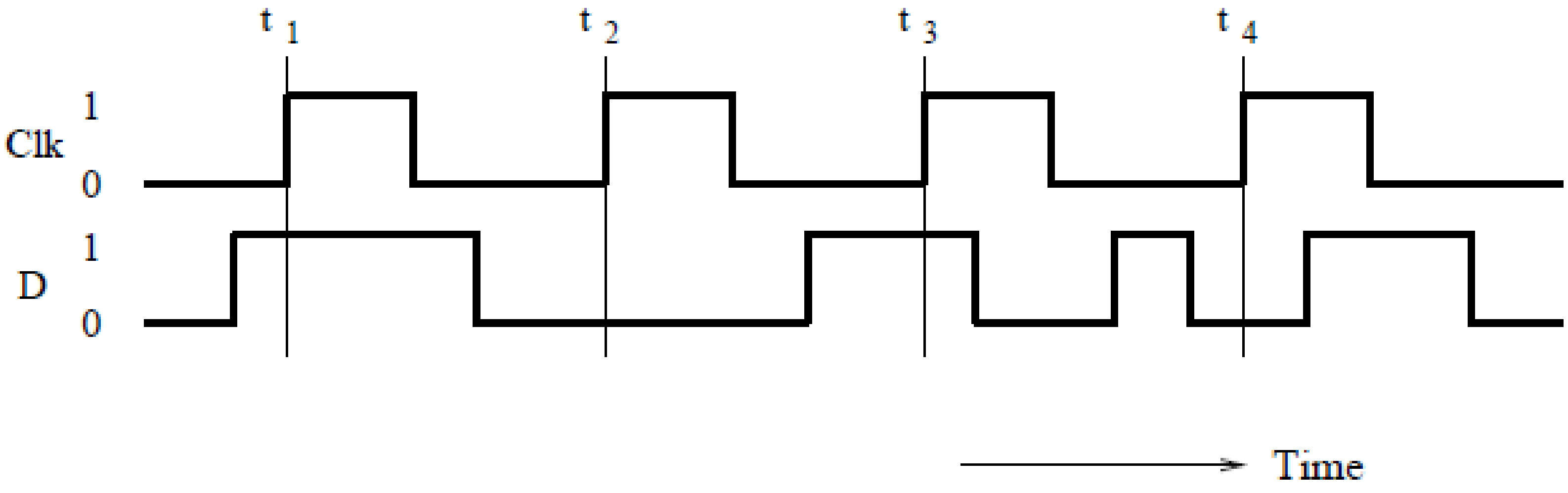
D latch is a special case of SR latch where S and R are derived from single input D

- When clk = 1
  - the Q output is set to the value of D input
- When clk = 0
  - the Q output retains its previous value irrespective of the D input

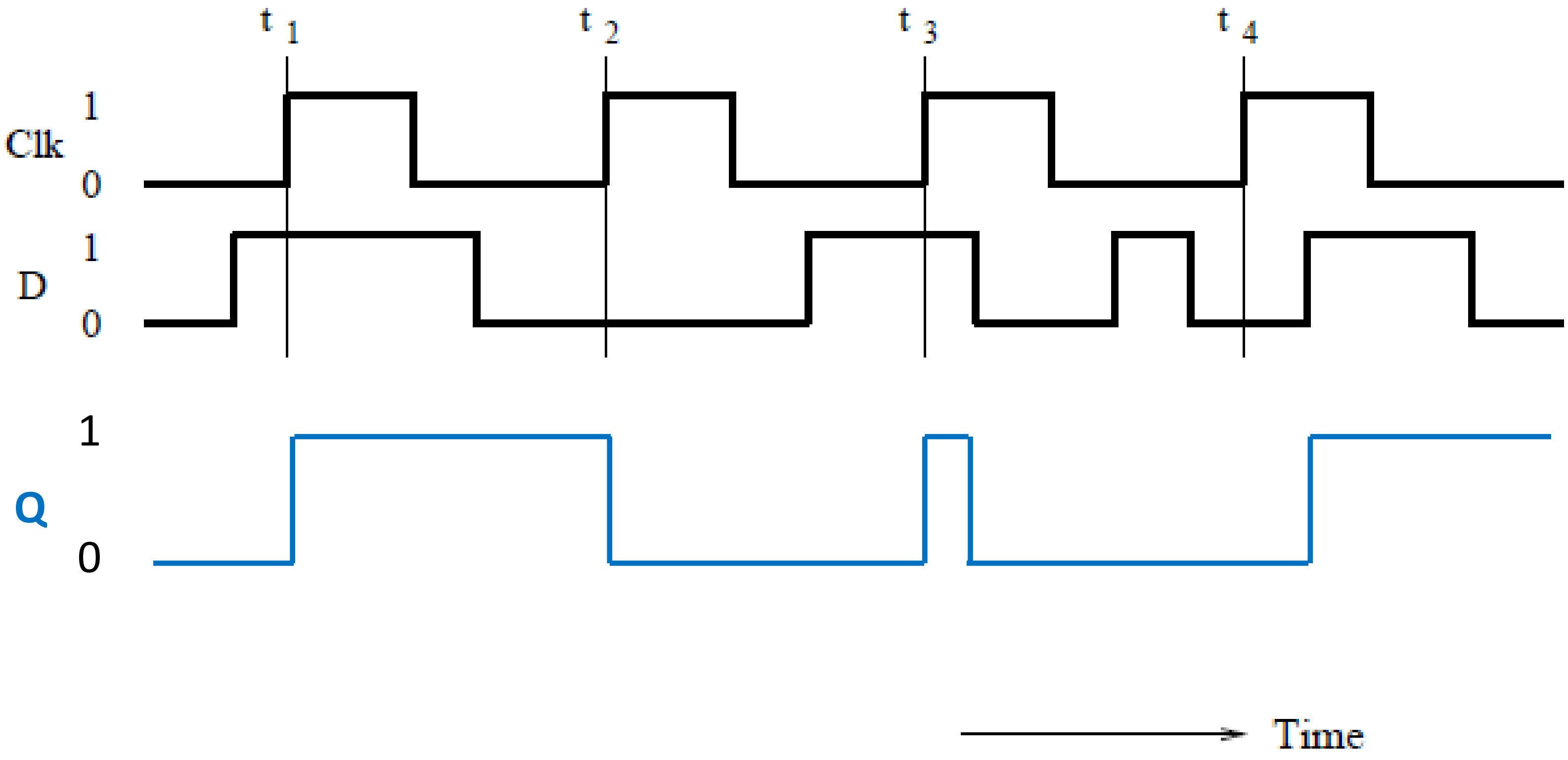
D latch samples input data when clk is high and stores data until next clock pulse

Practice Exercise

The clock and D inputs for a gated D latch are shown below. Plot the Q output as a function of time.



Practice Exercise: Solution

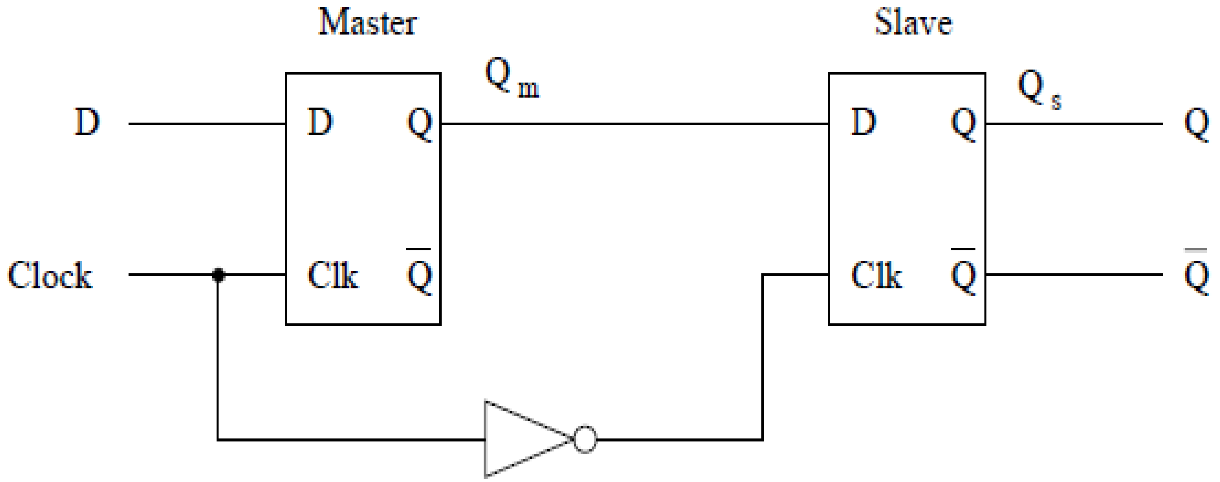


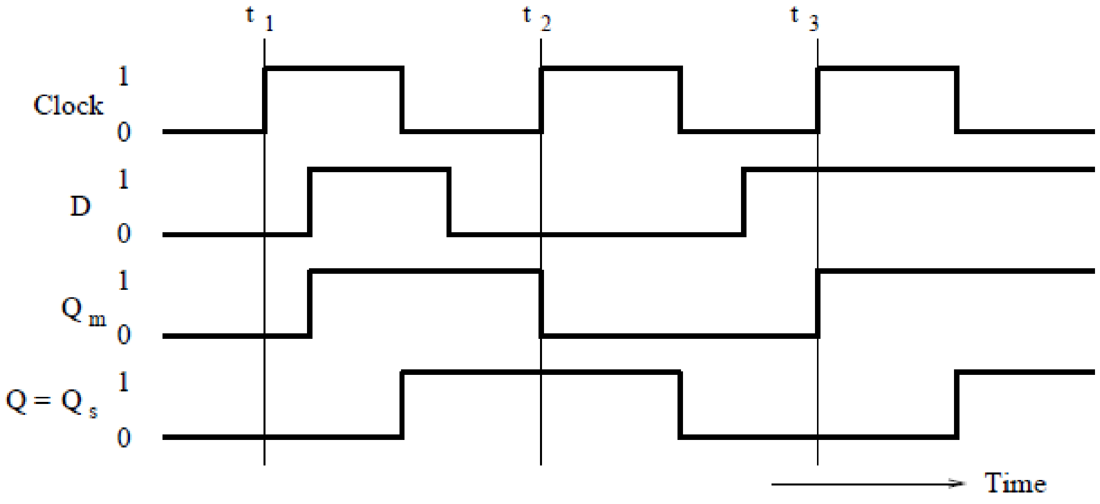
Limitations of Latches

- Latches are sensitive only to clock levels (level-sensitive)
- When clock is high, latch output responds immediately to any changes in inputs
- Undesirable in circuits involving counters and shift registers
  - Immediate propagation of inputs to outputs may lead to incorrect operation
- **Solution: Master-slave flip flop**
  - Sensitive to clock signal transitions (edge-sensitive)
  - Outputs isolated from inputs at all times except at clock transitions
  - Positive edge triggering: data transfer occurs at 0->1 clock transition
  - Negative edge triggering: data transfer occurs at 1->0 clock transition

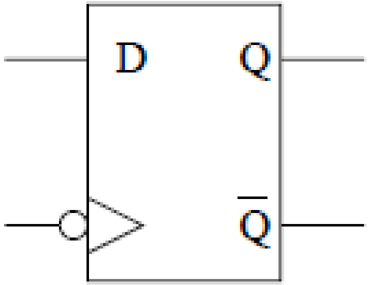
Master-slave D flip-flop

Circuit





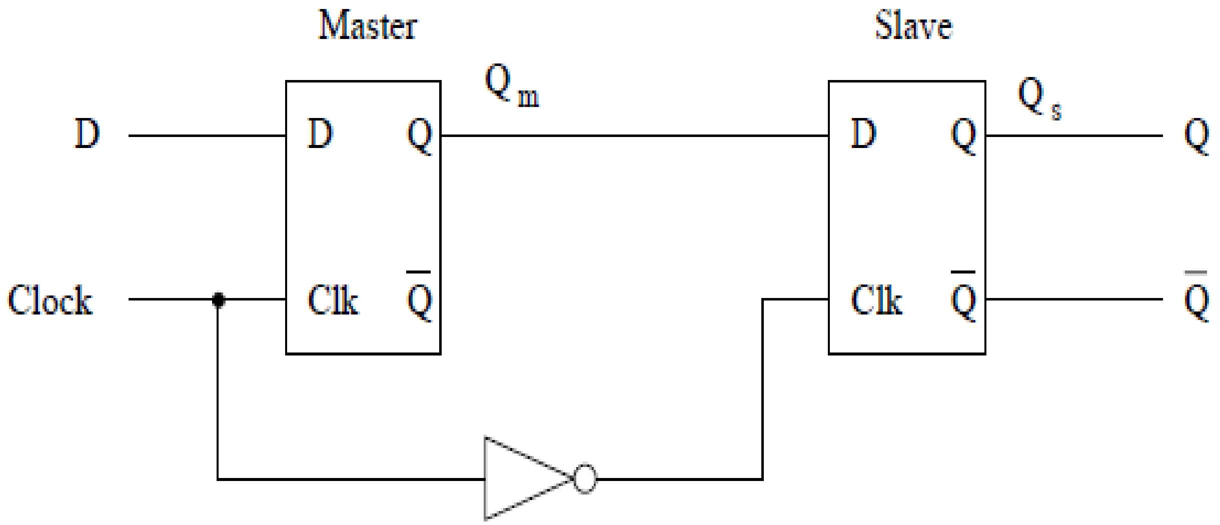
Example Timing Diagram



Graphical Symbol

Master-slave D flip-flop

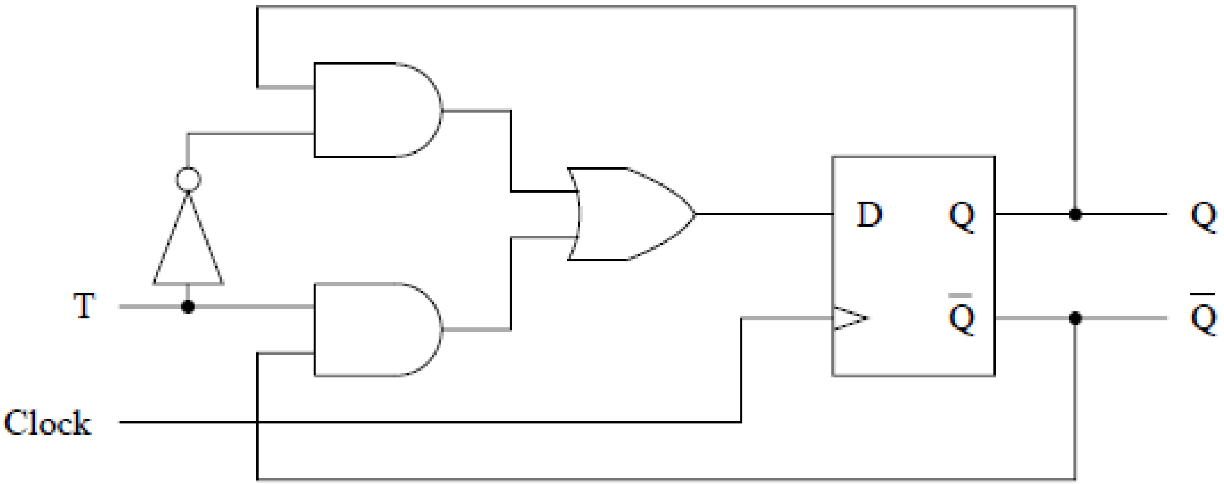
Circuit



- Two gated D-latches (master and slave) together form a master-slave flip-flop
- When clk = 1:
  - D input is transferred to master's output, slave's output is unchanged
- When clock transitions from 1 to 0:
  - Master's contents (Qm) transferred to slave's output (Q), master's output isolated from D-input
- D flip-flop is commonly used for temporary storage of data

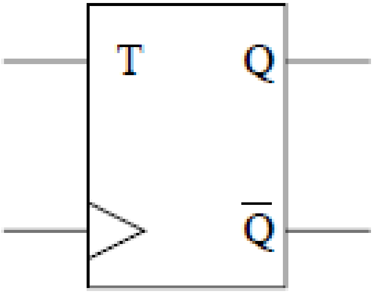
T flip-flop

Circuit



T	Q(t+1)
0	Q(t)
1	$\overline{Q}$(t)

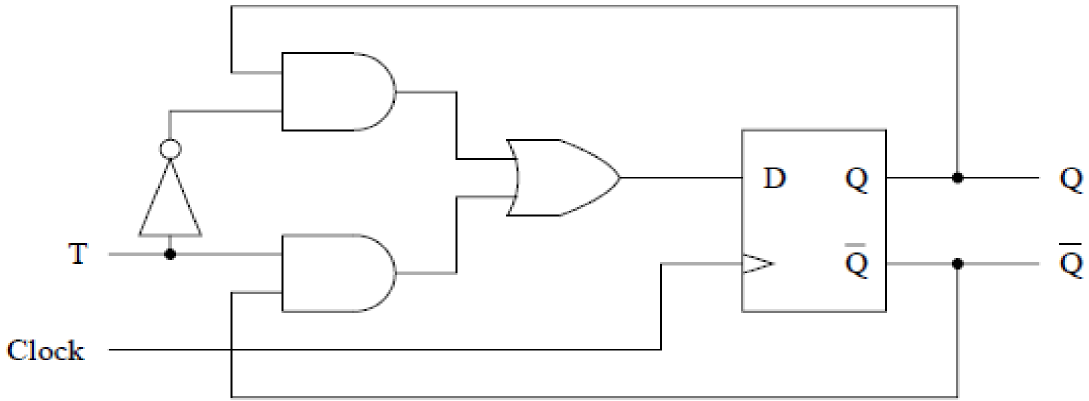
Truth Table



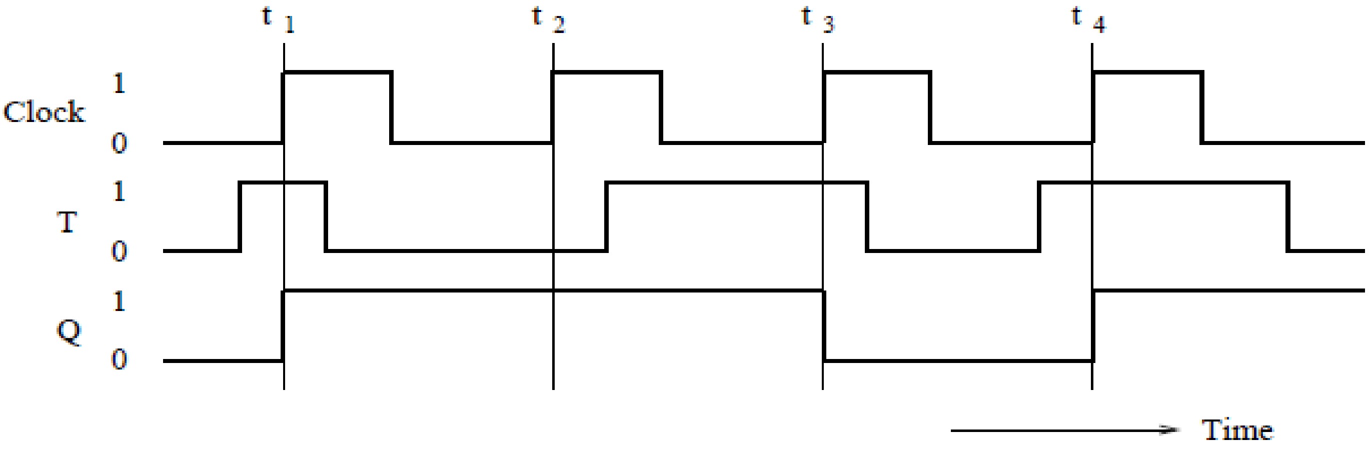
Graphical Symbol

T flip-flop

Circuit



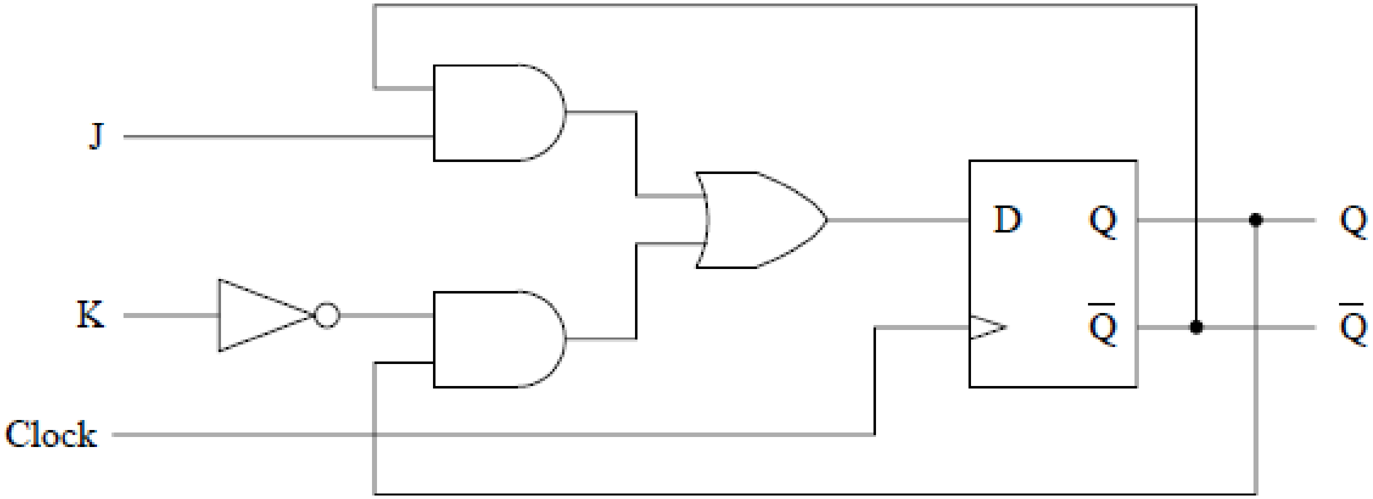
Example Timing Diagram



- T flip-flop toggles its state every cycle if its input T is equal to 1
- Useful in building counters

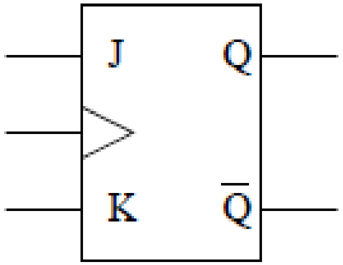
JK flip-flop

Circui



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q}$(t)

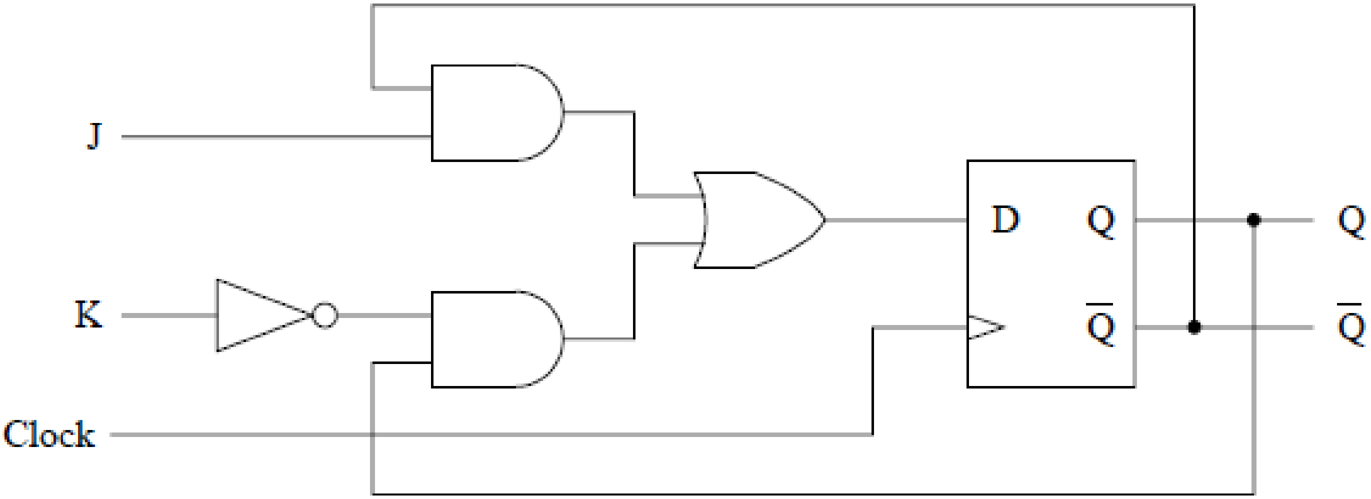
Truth Table



Graphical Symbol

JK flip-flop

Circui



- JK flip-flop combines the behavior of SR and T flip-flops
- When J = K = 1, it functions as a toggle (T flip-flop)
- For other input combinations, it acts as a SR flip-flop with J = S and K = R
- JF flip-flop is versatile; can be used both for data storage and building counters