# ECE 341 Midterm Exam

Name: _____

Time allowed: 90 minutes
Total Points: 70

## Problem No. 1 (9 points)

For each of the following statements, indicate whether the statement is TRUE or FALSE:

(a) Associative rule applies to both the AND and NAND operators.
(b) Any logic function expressed in a sum-of-products form can be implemented with NAND gates.
(c) CISC architectures are simpler to implement in hardware as compared to RISC architectures.
(d) For multiplying large numbers such as 64-bit or 128-bit numbers, an array multiplier requires fewer logic gates than a sequential multiplier.
(e) Subtracting a positive integer from another positive integer in 2's complement binary arithmetic cannot cause an overflow.
(f) If two 32-bit numbers are multiplied by using bit-pair recording of the multiplier, the number of summands is always less than 16.

## Problem No. 2 (21 points)

You are required to design a 2-bit synchronous counter by using a finite state machine. The counter has two external input signals $r$ and $x$, which dictate the operation of the counter as follows: (i) If $\boldsymbol{r = 0}$, the counter counts *up*, irrespective of the value of $x$, (ii) If $\boldsymbol{r = 1}$, $\boldsymbol{x = 0}$, the counter stops counting and retains its present value, (iii) If $\boldsymbol{r = 1}$, $\boldsymbol{x = 1}$, the counter is reset to a value of "0". The counter also has an output signal $z$, which is equal to 1 only if the present value of the counter is "3".

(a) **(6 points)** Draw the state diagram for this state machine.
(b) **(5 points)** Assume that D-flip flops are used to store the two state variables $y_2$ and $y_1$ and the state variable assignment is done in such a way that the number $y_2y_1$ represents the count value. Show the state-assigned state table.
(c) **(5 points)** Derive the *minimal* logic expression to implement the next state value $Y_1$ for the state variable $y_1$. You do not need to show the logic circuit implementation.
(d) **(5 points)** Implement the logic function derived in part (c) by using a 4-input multiplexer.

## Problem No. 3 (20 points)

(a) **(4 points)** A 4-bit carry-looakhead adder (CLA) is used to add two numbers X = 0101 and Y = 1001 with an external carry-in $c_0 = 1$. Compute the values of all the Generate ($G_0$, $G_1$, $G_2$ and $G_3$) and Propagate ($P_0$, $P_1$, $P_2$ and $P_3$) functions.
(b) **(10 points)** A multiplier circuit employing Booth algorithm is used to multiply two signed numbers +16 (multiplicand) and -7 (multiplier) expressed in 2's complement binary notation. Show the Booth recording for the multiplier and calculate the product by using Booth algorithm.

(c) **(6 points)** A processor P1 with a clock period of 0.4 nanoseconds is used to execute a program, whose instruction statistics are as follows:

| Type of Instruction | Percentage of Total Instructions | Cycles per Instruction |
|---|---|---|
| Branch | 10% | 3 |
| Load | 25% | 5 |
| Store | 15% | 4 |
| Arithmetic | 50% | 4 |

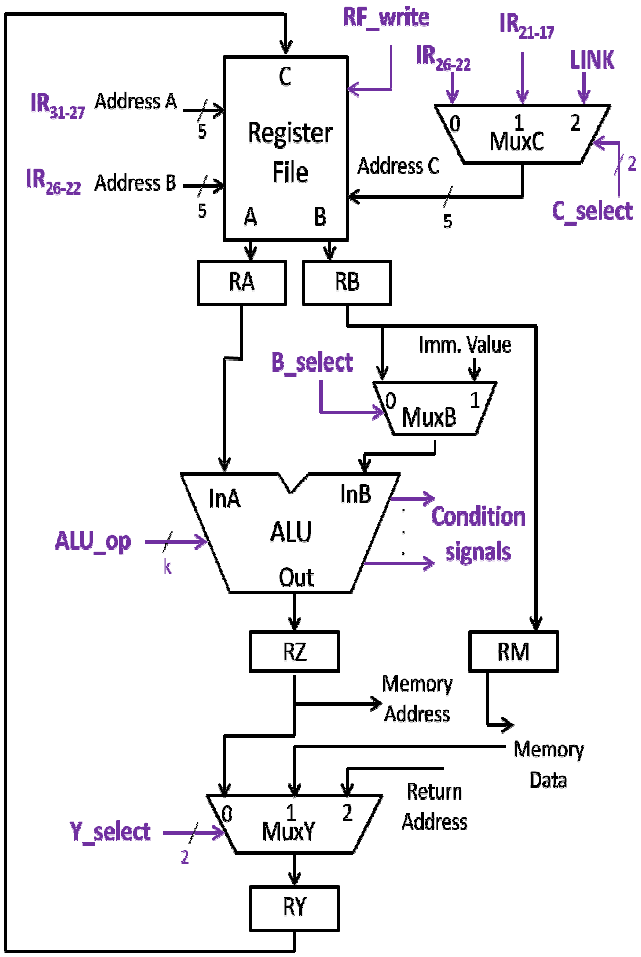
Compute the number of instructions completed by the processor in one millisecond.

## Problem No. 4 (20 points)

(a) **(7 points)** The 5-stage RISC processor discussed in class is used to execute the following sequence of instructions, one after the other:

Instruction 1: Load R4, #100(R2)
Instruction 2: Subtract R5, R3, R4
Instruction 3: Call #5000

The processor data path with all the control signals is shown in the following figure:



Write down the values of the following control signals:

(i) ***B_select*** during stage 3 of instruction processing (for instructions 1 and 2 only).

(ii) ***Y_select*** during stage-4 of instruction processing (for instructions 1 and 2 only).

(iii) ***C_select*** during stage-5 of instruction processing (for each of the three instructions).

(b) **(6 points)** Before the execution of the instruction sequence mentioned in part (a), the initial state of the processor is as follows: (i) Registers R2, R3 and R4 contain 6000, 300 and 500, respectively, (ii) Program counter (PC) contains 2000, (iii) Contents of memory address 6100 are 100. Write down the contents of inter-stage register *RY* after the completion of stage-4 for each of the three instructions.

(c) **(7 points)** The 5-stage RISC processor is required to support a new instruction called "ldu" (Load-update). This new instruction uses the same format as the "load" instruction discussed in class:

ldu *Rdst*, X(*Rsrc*)

However the semantics of the "ldu" instruction differ from the "load" instruction. Specifically, the "ldu" instruction performs two operations, which are illustrated by the following register-transfer notation:

Rdst ← [[Rsrc] + X]

**Rsrc ← [Rsrc] + X**

Note that the first operation of the "ldu" instruction is the same as the "load" instruction, but the second operation is done only by the "ldu" instruction. What modifications (if any) are needed in the 5-stage processor of part (a) to implement the "ldu" instruction? Your solution must ensure that the "ldu" instruction is completed in 5 cycles.