ECE341 Homework No. 1

Due date: 10/8/2014

Problem No. 1 (5 points)

Implement the XNOR function f = $\overline{x \oplus y}$ in the sum-of-products form.

Problem No. 2 (10 points)

Prove the following identities by using algebraic manipulation AND also by using truth tables:

(a) $x + w\bar{x} = x + w$

(b) $x \oplus (\overline{y \oplus z}) = x.y.\bar{z} + x.\bar{y}.z + \bar{x}.y.z + \bar{x}.\bar{y}.\bar{z}$

Problem No. 3 (15 points)

(a) Derive minimal sum-of-products form for the function *F* in the following truth table:

x_1	x_2	x_3	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(b) Show a logic circuit implementation for function *F*. **You will receive an extra credit of 5 pts,** if your implementation uses at most one NOT gate, one 2-input OR gate and one 2-input AND gate.

Problem No. 4 (5 points)

Prove that the associative rule does not apply to the NOR operator: (x ↓ y) ↓ z ≠ x ↓ (y ↓ z)

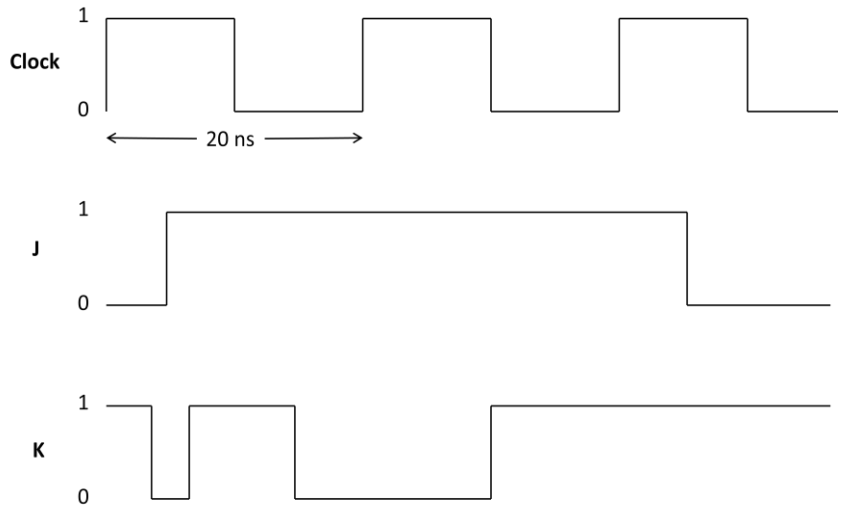
Problem No. 5 (10 points)

Implement the following function by using only NAND gates. Complemented input variables are not available and the use of NOT gates is not allowed.

$$f = xy + \bar{u}\bar{v}$$

Problem No. 6 (10 points)

The input waveforms for a positive edge-triggered JK flip flop are shown in the following figure. Assume that each waveform starts at time = 0 and output Q of the flip-flop has a logic value of "0" at time = 0. What is the logic value of output Q at the following points of time: (i) 8 ns, (ii) 18 ns, (iii) 28 ns, (iv) 38 ns, (v) 48 ns?



Problem No. 7 (10 points)

Derive the truth table for the NAND gate circuit shown in the following figure. Compare it with the truth table of the SR latch discussed in class (slide 7 of Lecture No. 2 or Figure A.23b in the textbook). What similarities or differences do you find between the two truth tables?