ECE 341 Midterm Exam

Name: _____

Time allowed: 90 minutes
Total Points: 75
Points Scored: _____

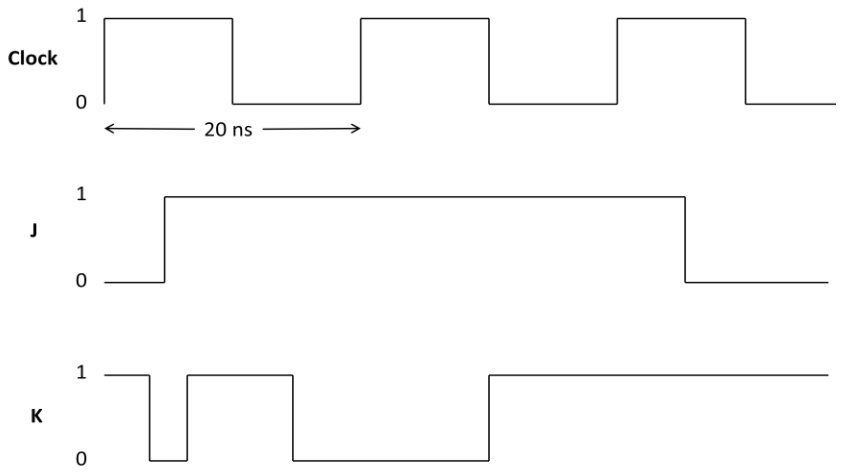
Problem No. 1 (10 points)

For each of the following statements, indicate whether the statement is TRUE or FALSE:

(a) It is undesirable to use latches for building circuits that involve counters and shift registers.
(b) Booth algorithm is most efficient when the multiplier has an alternating sequence of 1s and 0s.
(c) An array multiplier typically requires less hardware than a sequential multiplier.
(d) Subtracting a positive integer from a negative integer in 2's complement binary arithmetic can cause an overflow.
(e) A programmable device (such as an FPGA) usually achieves better performance than a customized device (such as ASIC) for a particular task.

Problem No. 2 (12 points)

(a) **(6 points)** The input waveforms for a positive edge-triggered JK flip flop are shown in the following figure. Assume that each waveform starts at time = 0 and output Q of the flip-flop has a logic value of "0" at time = 0. What is the logic value of output Q at the following points of time: (i) 18 ns, (ii) 35 ns, (iii) 50 ns?



(b) **(6 points)** Implement an XNOR function ($z = \overline{x \oplus y}$) by using a 2-input multiplexer and a NOT gate.

Problem No. 3 (18 points)

You are required to design a 2-bit synchronous counter by using a finite state machine. The counter has one external input signal *x*, which dictate the operation of the counter as follows:

(i) If *x* = 0, the counter counts *up* in the following sequence ……,0,1,2,3,0,1,2,3,0,1,2,…..

(ii) If *x* = 1, the counter acts as a *saturating down* counter: It counts *down* until it reaches 0 and then stops there.

The circuit also has an output signal *z*, which is equal to "1" *only* if the present value of the count is less than 3.

(a) **(6 points)** Draw the state diagram for this state machine.

(b) **(6 points)** Assume that D-flip flops are used to store the two state variables y_2 and y_1 and the state variable assignment is done in such a way that the number y_2y_1 represents the count value. Show the state-assigned state table.

(c) **(6 points)** Derive the *minimal* logic expression to implement the output z and the next state value Y_2. You do not need to show the logic circuit implementation.

Problem No. 4 (20 points)

(a) **(4 points)** A 4-bit carry-lookahead adder (CLA) is used to add two numbers $X(x_3x_2x_1x_0) = 1101$ and $Y(Y_3Y_2Y_1Y_0) = 1010$ with an external carry-in $c_0 = 1$. Use the CLA carry-out equation to compute the value of carry-out c_3.

(b) **(8 points)** A multiplier circuit employing Booth algorithm is used to multiply two numbers +8 (multiplicand) and -5 (multiplier) expressed in 2's complement binary notation. Show the Booth recording for the multiplier and calculate the product by using Booth algorithm.

(c) **(8 points)** A company is designing a processor P1 to execute a program, whose instruction statistics are as follows:

Type of Instruction	Percentage of Total Instructions	Cycles per Instruction
Branch	10%	3
Load	30%	5
Store	20%	4
Arithmetic	40%	4

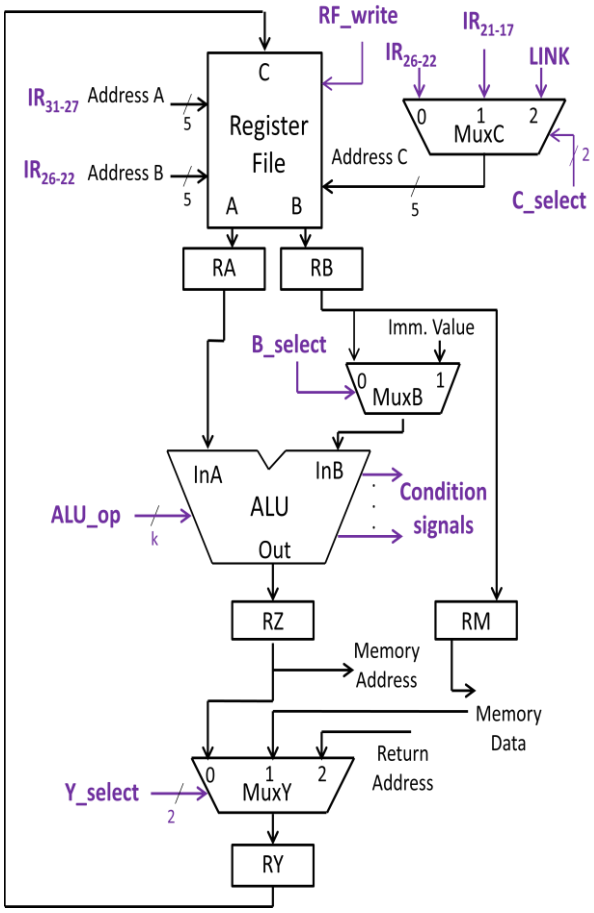
The chief architect for the processor sets a target that the processor must be able to execute 500 million instructions per second. What is the minimum clock speed that the processor must run at to achieve this target?

Problem No. 5 (15 points)

The 5-stage RISC processor discussed in class is used to execute the following sequence of instructions, one after the other:

Instruction 1: Load R4, 200(R3)
Instruction 2: Add R5, R2, R4
Instruction 3: Store R5, 400(R3)

The processor data path with all the control signals is shown in the following figure:



Assume that the initial contents of registers R2, R3, R4 and R5 are 200, 28000, 800 and 70 respectively. The contents of memory locations at addresses 28000, 28200 and 28400 are 400, 500 and 600, respectively.

(a) **(9 points)** For **each** of the three instructions in the program, answer the following questions:
(i) Which of the two inputs ("0" or "1") is selected by MuxB?

(ii) What are the contents of register RY after the completion of stage-4 (“memory access” stage)?

(iii) Write down the value of control signal RF_write during stage-5 of instruction processing.

(b) **(6 points)** After the completion of the above code sequence, what are the final contents of memory locations at addresses 28200 and 28400?