ECE341 Homework No. 4

Due date: 11/3/2014

Problem No. 1 (15 points)

(a) **(5 points)** Using manual methods, perform the operation *A*B* (*A* multiplied by *B*) on the 5-bit **unsigned** numbers *A* = 10111 and *B* = 11001.

(b) **(10 points)** Show how the multiplication operation in part (a) would be performed by a sequential circuit multiplier by constructing a chart similar to the one in Figure 9.7 of the textbook (slides 6 - 10 of lecture 7). Assume that *A* is the multiplicand and *B* is the multiplier.

Problem No. 2 (10 points)

Multiply each of the following pairs of **signed** 2's-complement numbers using the Booth algorithm. In each case, assume that *A* is the multiplicand and *B* is the multiplier.

(a) A = 110011 and B = 011100

(b) A = 010111 and B = 100111

(Hint: You can validate your result by converting the numbers to decimal representation, multiplying the two decimal numbers and then converting the product back to binary representation)

Problem No. 3 (10 points)

Repeat Problem No. 2 (a & b) by using bit-pair recording of the multipliers.

Problem No. 4 (20 points)

(a) A program is executed on two different processors P1 and P2. Both the processors have identical clock speeds of 2 GHz and use the same instruction-set architecture. The program consists of a total of 700 instructions, including a 200-instruction loop that is executed 5 times. The main difference between P1 and P2 is that P2 has an on-chip cache while P1 does not have a cache. Fetching and executing an instruction that is in the main memory requires 80 cycles. If the instruction is found in the cache, fetching and executing it requires only 4 cycles. Ignoring operand data accesses, calculate the speedup of P2 over P1. Assume that the cache is initially empty, that it is large enough to hold the loop, and that the program starts with all instructions in the main memory.

(b) Generalize part (a) by replacing the constants 700, 200, 5, 80, and 4 with the variables *w, x, y, m,* and *c*. Develop an expression for speedup in terms of these five variables.

(c) If the loop is executed 40 times (*y* = 40), with all the other parameters (*w, x, m,* and *c*) retaining the same values as in part (a), what is the new speedup of P2 over P1?

(d) Consider the form of the expression for speedup developed in part(b). What is the upper limit on speedup as the number of loop iterations, *y*, becomes larger and larger?

Problem No. 5 (13 points)

(a) **(5 points)** Consider a program running on a CISC processor P3 with a clock rate of 3 GHz. The instructions in the program can be categorized into two types:

(i) Type-1 (multiply-add instructions): Each of these instructions takes 4 cycles to execute on the processor P3.

(ii) Type-2: Each of these instructions takes 1 cycle to execute on P3.

Assume that 30% of the total instructions in the program are of Type-1, while the remaining instructions are of Type-2. Also assume that the program has a total of 1 million instructions. How long will it take processor P3 to execute the program completely?

(b) **(8 points)** A RISC processor P4 with a clock rate of 4 GHz is used to execute the program of part 3(a). P4 can execute each Type-2 instructions in 1 cycle, just like P3. However, P4 lacks the capability to execute Type-1 instructions as such. To mitigate this limitation, the compiler transforms each of the Type-1 instructions in the program into two instructions; a "multiply" instruction and an "add" instruction. Each "multiply" instruction takes 4 cycles to execute on P4 while each "add" instruction takes 1 cycle. Does P4 improve the performance of program in comparison to P3? If yes, what is the speedup of P4 over P3?

Problem No. 6 (10 points)

Consider a RISC processor "R_1" that uses the five-step sequence discussed in class and shown in Fig. 5.7 of the textbook.

(a) **(5 points)** Assume that the delays required by each of the processor operations are as follows: (i) Instruction fetch requires 1 ns, (ii) Decoding an instruction requires 0.4 ns, (iii) Accessing the register file requires 0.8 ns, (iv) Each ALU operation requires 0.5 ns, and (v) Reading or writing data to the memory requires 0.1 ns. Ignoring the delays incurred by multiplexers and inter-stage registers, what is the minimum clock period needed by R_1 to guarantee correct operation?

(b) **(5 points)** Consider a program "P_1" running on the processor R_1. Assume that the "Load" and "Store" instructions constitute 40% of the dynamic instruction count in P_1. What is the frequency of memory accesses (i.e., number of memory accesses per second)? (Hint: You should account for memory accesses due to both instruction fetches and data reads/writes).

Problem No. 7 (12 points)

Consider the following instruction executed on the 5-stage RISC processor:

Load R6, 40(R9)

(a) **(3 points)** Write down the register transfer notation (RTN) expression for the above instruction.

(b) **(5 points)** List the steps performed by the processor in each of the five processing stages (fetch, decode, execute, memory access and writeback) for this instruction.

(c) **(4 points)** At the time the above instruction is fetched, R6 and R9 contain the values 100 and 85320, respectively. The contents of memory locations 85320, 85340 and 85360 are 200, 400 and 600, respectively. What are the contents of R6 and R9 after this instruction has been executed by the processor?