ECE341 Homework No. 7

Due date: 11/26/2014

Problem No. 1 (12 points)

Consider a branch instruction which is executed 10 times in a program. The actual outcomes of the branch are T, T, T, NT, NT, T, T, T, NT, NT where T = Taken and NT = Not taken. Dynamic branch prediction is used to predict the branch outcomes. Show the predictions made for each instance of the branch and calculate the branch prediction accuracy in case of the following two predictors:

(a) A 1-bit branch predictor which starts in the *LNT* state
(b) A 2-bit branch predictor which starts in the *SNT* state

Refer to class notes and Figure 6.12 in the textbook for the state machine diagrams of the two predictors.

Problem No. 2 (8 points)

A 5-stage pipelined RISC processor R_1 running at 2.8 GHz is used to execute a program P_1. Processor R_1 uses operand forwarding to mitigate data hazards. Assume that *load* instructions constitute 35% of dynamic instruction count in P_1 and 40% of *load* instructions are immediately followed by a dependent instruction. Also assume that data hazards caused by *load* instructions are the only source of pipeline stalls. Calculate the instruction throughput of processor R_1.

Problem No. 3 (12 points)

Two 5-stage pipelined RISC processors R_2 and R_3 are used to execute a program P_2. 20% of the dynamic instructions in P_2 are branch instructions and 70% of all the branches are taken. Both processors R_2 and R_3 have the same clock rate. R_2 uses a static branch predictor with a "always-not-taken" prediction. R_3 uses a dynamic branch predictor with a branch target buffer, as illustrated in Section 6.6.4 of the textbook. Assume that branch penalty is the only source of pipeline stalls in both R_2 and R_3.

(a) What is the minimum branch prediction accuracy for R_3 to perform at least as well as R_2?
(b) If the branch prediction accuracy for R_3 is actually 90%, what is the speedup for R_3 relative to R_2? You can assume that the computation of branch outcomes in both R_2 and R_3 is carried out in the "Compute" stage (stage-3).

Problem No. 4 (8 points)

A 5-stage pipelined RISC processor R_4 running at 3 GHz is used to execute a program P_3. Assume that 20% of the dynamic instructions in P_3 are branch instructions. R_4 does not use any branch prediction and instead relies on the branch delay slot optimization. The compiler is able to fill 80% of the branch delay slots in the program P_3 with useful instructions. The remaining delay slots are filled with NOP

instructions. Calculate the instruction throughput of processor R_4. You can assume that the computation of branch outcomes is done in the "Decode" stage and branch penalty is the only source of pipeline stalls.

Problem No. 5 (15 points)

A 5-stage pipelined RISC processor R_5 running at 2.4 GHz is used to execute a program P_4. The instructions statistics for P_4 are as follows:

Branch: 20%

Load: 20%

Store: 10%

Arithmetic Instructions: 50%

Assume that there are no data dependencies in the program. Also assume that 1% of all instruction fetch operations and 2% of all data accesses incur a cache miss. The penalty to access the main memory for a cache miss is 10 cycles. R_5 uses a dynamic branch predictor and a branch target buffer to predict all the branches during the "fetch" stage. The computation of actual branch outcomes is carried out in the "decode" stage.

A customer demands the processor manufacturer that the processor R_5 must achieve an instruction throughput of 2 billion instructions per second. What must be the minimum branch prediction accuracy for the branch predictor used in R_5 to satisfy this demand?