ECE341 Homework No. 5

Due date: 11/12/2014

Problem No. 1 (4 points)

(Problem 5.3 from textbook): Figure 5.12 (also shown on slide 19 of Lecture 10) shows the bit fields assigned to register addresses for different groups of instructions. Why is it important to use the same field locations for all instructions?

Problem No. 2 (12 points)

The following instruction is stored in location 0x24A014 in the memory:

OR R2, R2, R6

At the time this instruction is fetched, registers R2 and R6 contain the values 0x24B4 and 0xA742, respectively. Give the values in registers PC, RA, RM, RZ, and RY of Figures 5.8 and 5.10 (slides 10 and 17 of Lecture 10) in each clock cycle as this instruction is executed, and also in the first clock cycle of the next instruction. You do not need to show the contents of *every* register in *every* cycle, but only need to show those register values that change during a particular cycle.

Notes: (i) 0x represents hexadecimal or base-16 representation, (ii) The "OR" instructions performs a bitwise OR operation over the contents of the two source registers and stores the result in the destination register.

Problem No. 3 (10 points)

The MIPS instruction set includes a move-if-zero (Movz) instruction, whose syntax is as follows:

Movz Rdst, Rsrc1, Rsrc2

The Movz instruction copies the contents of register Rsrc2 into register Rdst, *if* the contents of register Rsrc1 are equal to zero. You are required to implement this instruction on the five-stage RISC hardware discussed in class.

(a) **(6 points)** What modifications (if any) are needed in the datapath of Figure 5.8 to implement this instruction?

(b) **(4 points)** Give the sequence of actions needed in each of the five stages of processor hardware to execute this instruction.

Problem No. 4 (12 points)

A RISC processor that uses the five-step hardware discussed in class is driven by a 2.5 GHz clock. Instruction statistics in a large program are as follows:

Branch	15%
Load	25%
Store	15%
Computational Instructions	45%

Estimate the rate of instruction execution (number of instructions completed per second) in each of the following cases:

(a) **(5 points)** Access to the memory is always completed in 1 clock cycle

(b) **(7 points)** 95% of instruction fetch operations are completed in one clock cycle and 5% are completed in 10 clock cycles. Access to the data operands of a Load/Store instruction is completed in 2 clock cycles, on average.

Problem No. 5 (17 points)

The 5-stage RISC processor discussed in class is used to execute the following sequence of instructions, one after the other:

Instruction-1: LOAD R4, #200(R2)
Instruction-2: AND R5, R3, R4
Instruction-3: CALL_REGISTER R5

Refer to the processor datapath and control signals discussed in class (shown on slide 13 of Lecture 11) and answer the following questions:

(a) **(8 points)** Fill the following table to indicate the values of control signals for each of the three instructions:

	B-select in stage-3	*Y-select* in stage-4	*RF_write* in stage-5	*C_select* in stage-5
LOAD				
AND				
CALL_REGISTER				

(b) **(9 points)** Assume that the initial contents of program counter (PC), R2, R3 and R4 are 40, 2000, 60 and 100, respectively. Also assume that the initial contents of memory addresses 2000 and 2200 are 10 and 26, respectively.

i. Write down the contents of inter-stage register ***RZ*** after the completion of stage-3 for instructions 1 and 2.

ii. Write down the contents of inter-stage register ***RY*** after the completion of stage-4 for each of the three instructions.

iii. Write down the final contents of the PC after the completion of the above instruction sequence.