ECE 341 Midterm Exam

Name: _____

Time allowed: 75 minutes
Total Points: 75
Points Scored: _____

Problem No. 1 (8 points)

For each of the following statements, indicate whether the statement is TRUE or FALSE:

(a) A JK flip-flop can provide the same functionality as a T flip-flop.
(b) Associative rule does not apply to the NAND and XOR operators.
(c) Subtracting a negative integer from another negative integer in 2's complement binary arithmetic can cause an overflow.
(d) If two 16-bit numbers are multiplied by using bit-pair recording of the multiplier, the number of summands is always less than or equal to 8.

Problem No. 2 (12 points)

Multiple possible answers are provided for each of the following questions. Encircle **ALL** the correct answers in each case.

(a) A 16-bit **ripple-carry** adder is used to add two numbers X ($x_{15}x_{14}x_{13}……x_1x_0$) and Y ($y_{15}y_{14}y_{13}….y_1y_0$) to generate a 16-bit sum S ($s_{15}s_{14}s_{13}……s_1s_0$). How many gate delays are required to compute s_{13}, after all the inputs have been applied?
   i. 8
   ii. 25
   iii. 27
   iv. 31

(b) A 16-bit **blocked carry-lookahead adder (CLA)** composed of four 4-bit CLA blocks is used to add the same numbers X and Y, as in part (a). Under which of the following conditions is the carry-out c_{16} equal to 1?
   i. $c_0 = 0$, none of the CLA blocks generates a carry, but all the CLA blocks propagate a carry
   ii. $c_0 = 0$, all the CLA blocks generate a carry, but none of the CLA blocks propagate a carry
   iii. $c_0 = 1$, none of the CLA blocks generates a carry, but all the CLA blocks propagate a carry

(c) A processor running at a clock speed of 2 GHz is able to complete 1 billion instructions in 7 seconds. Assume that the execution time is dominated by the memory access time needed to fetch instructions from memory and read/write data to memory in case of load/store

instructions. Each memory access requires 10 clock cycles. What is the total percentage of load and store instructions in the program?

i. 35%
ii. 40%
iii. 50%
iv. 60%

Problem No. 3 (20 points)

You are required to design a 2-bit synchronous counter by using a finite state machine. The counter has two external input signals *u* and *v*, which dictate the operation of the counter as follows: (i) If $u = 0$, $v = 0$ **OR** $u = 1$, $v = 1$, the counter is reset to a value of "0", (ii) If $u = 0$, $v = 1$, the counter counts *up*, (iii) If $u = 1$, $v = 0$, the counter counts *down*. The outputs of the counter are the flip flop values themselves.

(a) Draw the state diagram for this state machine.

(b) Assume that D-flip flops are used to store the two state variables y_2 and y_1 and the state variable assignment is done in such a way that the number y_2y_1 represents the count value. Show the state-assigned state table.

(c) Derive the *minimal* logic expression to implement the next state value Y_1 for the state variable y_1. You do not need to show the logic circuit implementation.

(d) Implement the logic function derived in part (c) by using a 4-input multiplexer.

Problem No. 4 (10 points)

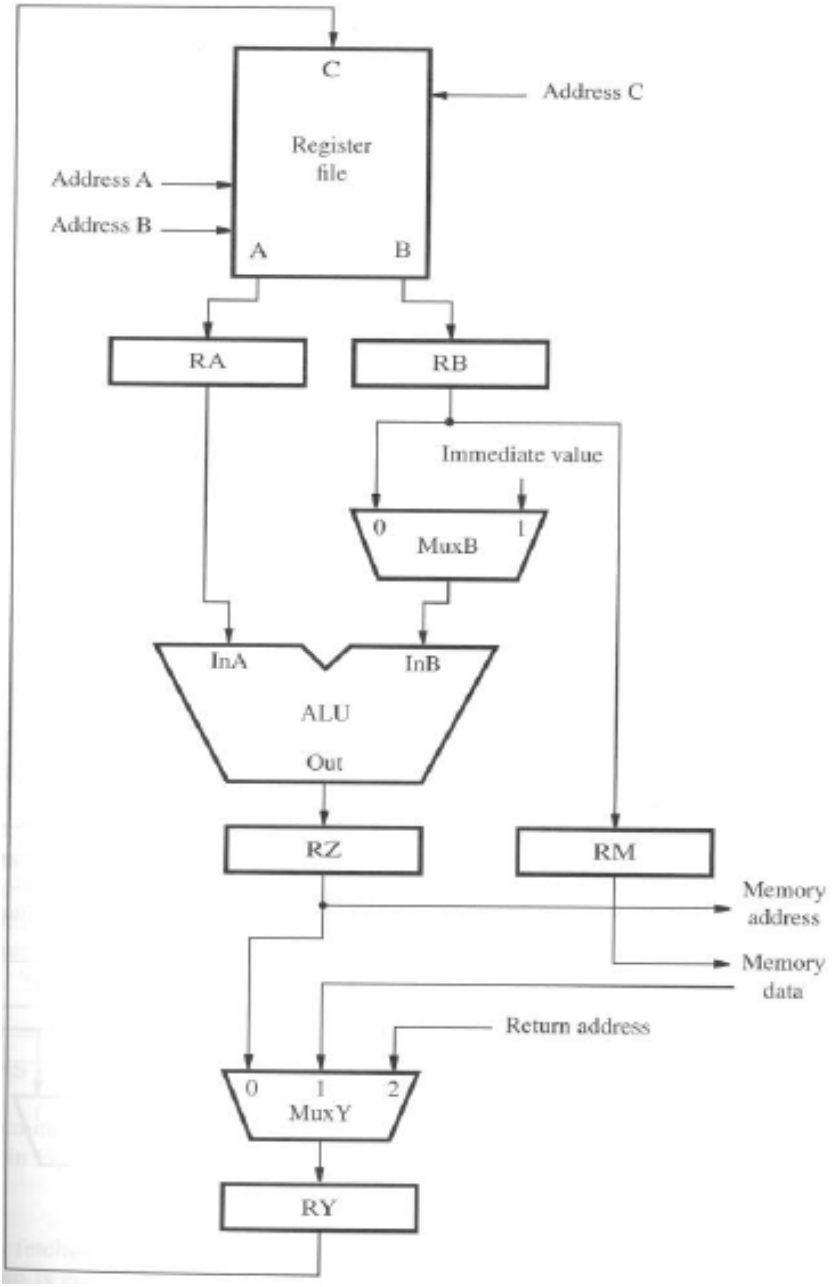
A multiplier circuit employing Booth algorithm is used to multiply two signed numbers +14 (multiplicand) and -9 (multiplier) expressed in 2's complement binary notation. Show the Booth recording for the multiplier and calculate the product by using Booth algorithm.

Problem No. 5 (15 points)

A 5-stage RISC processor is used to execute the following sequence of instructions, one after the other:

Instruction 1: Add R3, R2, #100
Instruction 2: Load R4, 100 (R3)
Instruction 3: Add R6, R4, R5

Assume that the initial contents of registers R2, R3, R4 and R5 are 86000, 87000, 88000 and 70 respectively. The contents of memory locations at addresses 86200, 87100 and 88000 are 50, 70 and 90, respectively. The processor data path discussed in class is shown in the following figure:



For **each** of the three instructions in the program, answer the following questions:

(a) Which of the two inputs (“0” or “1”) is selected by MuxB?
(b) Which of the three inputs (“0”, “1”, or “2”) is selected by MuxY?
(c) What are the contents of register RA at the end of “instruction decode” stage?
(d) What are the contents of register RY at the end of “memory access” stage?

Problem No. 6 (10 points)

A processor P1 running at a clock speed of 2 GHz is used to execute a matrix multiplication program, whose instruction statistics are as follows:

Type of Instruction	Percentage of Total Instructions	Cycles per Instruction
Branch	10%	2
Load	30%	4
Store	20%	4
Arithmetic	40%	3

A circuit designer proposes an optimization to the processor ALU, which enables all the arithmetic instructions to complete in one fewer cycle. However, this change requires the clock period for P1 to be lengthened by 15%. Will this change increase or decrease the execution time of the matrix multiplication program? Please show all the calculations.