# ECE341 Homework No. 2

**Due date:** 10/15/2014

## Problem No. 1 (8 points)

In the class, we studied a 4-bit shift register network (Lecture # 3, slide #4) that shifts the data to the right one place at a time under the control of a clock signal. Modify this register to make it capable of operating in the following two modes under the control of the clock signal and an additional control input shr/rot, as follows: (i) If shr/rot = 1, the register should act as a standard shift right register (External data input written to F1, F1's contents move to F2, F2's contents move to F3 and F3's contents move to F4 on each +ve clock edge) (ii) If shr/rot = 0, the register should act as a rotator (F1's contents move to F2, F2's contents move to F3, F3's contents move to F4 and F4's contents written to F1 on each +ve clock edge). Show your modifications in a figure.

## Problem No. 2 (10 points)

A logic function to be implemented is described by the expression:

$$f(x1, x2, x3, x4) = x2.x3.x4 + x1.x2.\overline{x3} + \overline{x2}.x3$$

(a) Show an implementation of *f* in terms of an eight-input multiplexer circuit.

(b) **(Extra Credit: 5 points)** Can *f* be realized with a four-input multiplexer circuit? If so, show how. Note: Apart from the 4-input multiplexer, you cannot use any additional logic gates (such as AND, OR, NOT) in your implementation.

## Problem No. 3 (12 points)

(a) Using positive edge-triggered T flip-flops, design a 3-bit asynchronous counter which counts in the following sequence: 0, 3, 4, 7, 0, 3, 4, 7 , 0, 3, 4, 7, 0, 3, …….

(b) Repeat Problem 3(a) for the following sequence: 0, 1, 4, 5, 2, 3, 6, 7, 0, 1, 4, 5, 2, 3, …..

## Problem No. 4 (10 points)

Complete the design of the mod-4 up/down counter discussed in class (Figure A.46 in textbook) by using a different state assignment S0 = 10, S1 = 00, S2=11, and S3=01. Derive the new state-assigned state table and logic expressions to implement the counter. You do not need to show the logic circuit implementation.

## Problem No. 5 (25 points)

You are required to design a 2-bit synchronous counter by using a finite state machine. The counter has two external input signals *r* and *x*, which dictate the operation of the counter as follows: (i) If ***r* = 0**, the

counter counts *up*, irrespective of the value of *x*, (ii) If ***r* = 1**, ***x* = 0**, the counter stops counting and retains its present value, (iii) If ***r* = *1*, *x* = *1*,** the counter is reset to a value of "0". The counter also has an output signal *z*, which is equal to 1 only if the present value of the counter is an odd number.

(a) Draw the state diagram for this state machine.

(b) Assume that D-flip flops are used to store the two state variables $y_2$ and $y_1$ and the state variable assignment is done in such a way that the number $y_2y_1$ represents the count value. Show the state-assigned state table.

(c) Derive the *minimal* logic expression to implement the next state values $Y_1$ and $Y_2$ for the state variable $y_1$ and $y_2$, respectively.

(d) Show the logic circuit implementation of the counter.