ECE341 Homework No. 3

Due date: 10/22/2014

Problem No. 1 (12 points)

(a) What range of signed integers can be specified by using **10-bit** 2's complement representation?

(b) Convert the following pairs of decimal numbers to **5-bit** 2's complement numbers, and then add them. State whether or not overflow occurs in each case.

(i) -4 and 12
(ii) 6 and 10
(iii) 9 and -8

Problem No. 2 (9 points)

Repeat Problem No. 1(b) for the subtraction operation, where the second number of each pair is to be subtracted from the first number. State whether or not overflow occurs in each case.

Problem No. 3 (6 points)

A 16-bit ripple carry adder is used to add two numbers X and Y. How many gate delays are required to compute the following outputs: (i) c_7, (ii) s_{13}, (iii) c_{16}?

Problem No. 4 (12 points)

A 4-bit carry-lookahead adder (CLA) is used to add two numbers X = 0010 and Y = 1011 with an external carry-in $c_0 = 1$.

(a) Compute the values of all the Generate (G_0, G_1, G_2 and G_3) and Propagate (P_0, P_1, P_2 and P_3) functions.
(b) Use the CLA carry-out equation to compute the values of c_3 and c_4.

Problem No. 5 (12 points)

(a) How many logic gates are needed to build a 4-bit CLA (shown in slide 20 of lecture 5)? What is the maximum fan-in for the logic gates used to build this adder?
(b) Repeat Problem 5(a) for a 4-bit ripple-carry adder.

Problem No. 6 (14 points)

Consider the 16-bit blocked CLA with first-level propagates and generates discussed in class (slides 6 and 7 in lecture 6, also shown in Figure 9.5 in the textbook).

(a) Derive the logic expression for c_{12} in terms of c_0 and the first-level propagate and generate functions.

(b) Calculate the number of gate delays for the following outputs: (i) c_7, (ii) s_{13}.
Compare the delays for the same outputs (c_7, s_{13}), when using the 16-bit ripple carry adder discussed in Problem No. 3.